Analogue-to-digital converters support multicarrier systems

A lack of suitable analogue-to-digital converters is a problem for systems designers. Heinz-Peter Beckemeyer of Texas Instruments explains.

Advanced wireless telecommunications equipment, such as UMTS multicarrier receivers and power amplifier (PA) linearization systems, require analogue-to-digital converters (ADCs) capable of high-speed operation and high resolution. A lack of suitable ADCs has been a stumbling block for systems designers and this has led US-based Texas Instruments (TI) to develop the ADS5500 14-bit ADC.

The device operates at 125 mega-samples per second (MSPS) and represents an important step forward in the design of high-speed ADCs. It offers the unique combination of 14-bit resolution, high conversion speed and very-low power consumption. Designed with a complementary metal-oxide semiconductor process using a pipeline architecture, the ADS5500 only consumes about 750 mW of power, which is about 50% of the power dissipated by today's 100 MSPS ADCs.

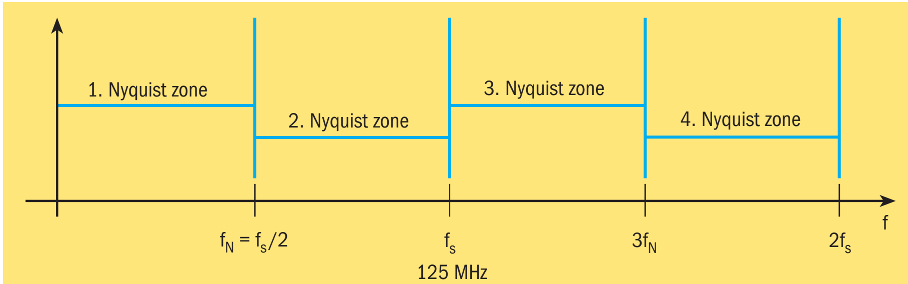

Fig. 1. Texas Instruments' ADC, the ADS5500, has Nyquist zones that are defined by its 125 MSPS sampling rate.

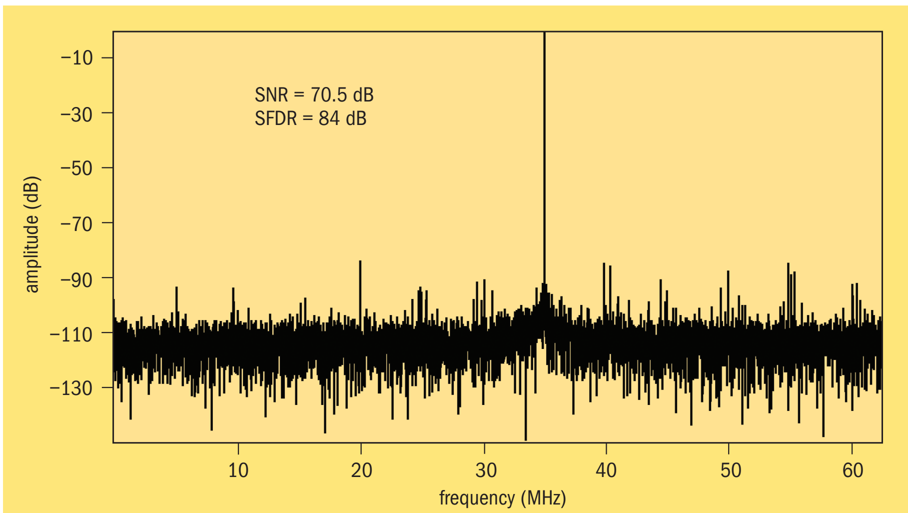

Fig. 2. A fast Fourier transform of a 90 MHz input signal digitized by the ADS5500 sampling at 125 MSPS.

Dynamic performance

The ADS5500 was designed specifically to fulfil the dynamic-range requirements of UMTS multicarrier receivers, which must operate at 122.88 MSPS. The sample-and-hold stage of the ADC has a bandwidth of 750 MHz, which ensures a stable dynamic performance even at high input frequencies in the 200 MHz range. This makes the ADC attractive for high intermediate-frequency (IF) sampling architectures.

An ADC operating in high-IF sampling mode can be used in place of a mixer stage. This reduces the overall cost of the receiver because a mixer stage requires a phase-locked loop (PLL), a voltage-controlled oscillator (VCO) and a filter.

Traditionally, receivers for UMTS base stations used dual-conversion architectures, which involve two mixer stages. The first stage converts the radio-frequency (RF) signal at 1.9 GHz down to the first IF of about 200 MHz. A second mixer stage then reduces the frequency further to 40–60 MHz.

Dual-conversion was required because the dynamic performance of an ADC is only suitable in the first and second Nyquist zones. A Nyquist zone defines the frequency range of a signal that can be sampled by an ADC operating at a specific sampling rate. Many first-generation UMTS receivers use ADCs operating at 61.44 MSPS. These devices have their first Nyquist zone at 0–30.72 MHz and the second zone at 30.72–61.44 MHz.

With 125 MSPS as the maximum sampling rate, the ADS5500 was designed for high-IF sampling architectures and provides a wide Nyquist bandwidth (see figure 1). The signal-to-noise ratio (SNR) of the ADC in the first Nyquist zone (0–62.5 MHz) at 125 MSPS is in the 72 dB range. The SNR remains very stable in the 70–71.5 dB range in the second zone (62–125 MHz). It stays at 70 dB up to an input frequency of more than 150 MHz, dropping to 69 dB at 220 MHz. The spurious free dynamic range (SFDR) is still in the range of 80–85 dBc for frequencies in the 70–150 MHz range and 75 dB at 220 MHz.

The clock-signal and aperture jitter of an ADC's sample-and-hold stage are important in the SNR, especially at high IFs. The device offers a low aperture jitter of 300 fs.

Figure 2 shows a fast Fourier transform (FFT) plot for an input frequency of 90 MHz at a sample rate of 125 MHz. The FFT displays the Nyquist frequency range from 0 to 62.5 MHz. The input frequency is shown at 35 MHz because the ADC is operated in IF- or under-sampling mode. The frequency of

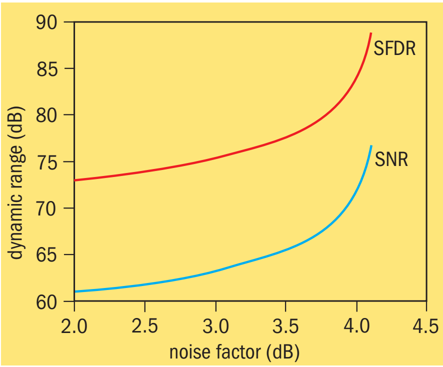

Fig. 3. A plot of the required dynamic performance versus noise factor of a ADS5500-based W-CDMA receiver.

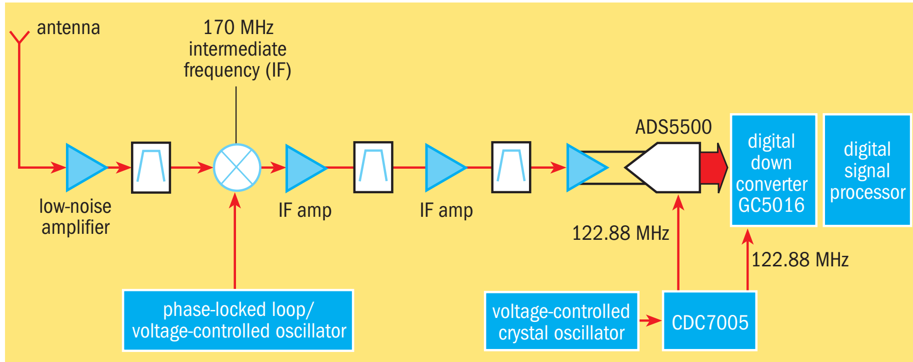

Fig. 4. The ADS5500 can be used to create a multicarrier UMTS receiver architecture with only one mixer stage. This is a cost-effective design because it eliminates the need for several discrete components in a second mixer stage.

90 MHz is therefore displayed as 125 MHz minus 90 MHz, which is 35 MHz.

The ADS5500 has a high sampling rate and therefore has a high Nyquist bandwidth, which equals the sampling rate divided by two. This leads to over-sampling in most applications, which is defined by the ratio of the Nyquist bandwidth to the bandwidth of the signal of interest. Over-sampling spreads the quantization noise over a wider band, resulting in a processing gain that is proportional to the logarithm of the over-sampling ratio. The use of the ADC in a UMTS receiver with a sampling rate of 122.88 MSPS and a signal bandwidth of 3.84 MHz results in a processing gain of 12 dB.

A high Nyquist bandwidth is also an important criterion for ADCs used in digital pre-distortion (DPD) systems. These systems are used to linearize base-station PAs and their application can lead to significant cost savings in terms of hardware requirements and energy consumption.

DPD involves measuring the PA intermodulation and then pre-distorting it up to the fifth-order component. To achieve this, the PA signal is usually down-converted to an IF. An ADC then digitizes the signal and the intermodulation components. In a dual-carrier transmitter with 10 MHz bandwidth, the DPD system needs five times more bandwidth than the UMTS carrier, which is 50 MHz.

The UMTS base-station receiver specification defines a range of parameters, including the ADC's dynamic range. Also specified is the maximum bit-error-rate (BER) in the presence of an interfering signal in the same frequency channel. The specifications relating to blocker signals for a multicarrier receiver are also important. Where an adjacent-channel signal exists at a level of –52 dBm, the receiver must be able to detect the desired signal at a level of –115 dBm reference sensitivity with specified BER. The separation between the adjacent channel and the actual carrier is 5 MHz.

Increasing sensitivity

The receiver must display the same characteristics for a blocker signal with an offset of 10 MHz and a level of –40 dBm. The receiver's reference sensitivity is –121 dBm at a data rate of 12.2 kbit/s without a blocker in the adjacent or alternate channel. Base-station manufacturers usually try to better this sensitivity value to make their equipment more competitive.

In a multicarrier design, the ADC must be able to convert an entire frequency block. This corresponds to a bandwidth of 15 MHz in the case of three adjacent carriers and 20 MHz for four. A blocker level of –40 dBm has to be taken into account in the calculation of the dynamic performance of the ADC.

The SNR and SFDR are the most important criteria for a UMTS receiver. The SFDR can be viewed as the difference between the blocker and the reference sensitivity levels. Figure 3 shows an example of the SNR calculation for a three- or four-carrier system. The calculation was carried out using a reference sensitivity of –121 dBm in the presence of a blocker signal, which is 6 dB better than the –115 dBm limit set by the UMTS standard. A peak-to-average ratio of 4 dB for a W-CDMA blocker signal with one user code is used, and ADC had a processing gain of 12 dB. A de-spreading gain of 25 dB was taken into account (3.84 MCPS/12.2 kbit/s) and an Eb/No signal-to-noise ratio of 5 dB.

Figure 3 also shows that the SFDR greatly depends on the noise factor (NF) of the receiver chain, excluding the ADC. An NF of 3.8 dB, which includes a margin for the non-linearity impairments of the RF chain, results in an ADC SNR of around 68 dB for a four-carrier system. Figure 3 shows that the ADS5500 can provide enough dynamic range at high IF for a UMTS multicarrier receiver, even at a high input frequency of more than 150 MHz.

Figure 4 shows how the ADS550 can be used in a cost-efficient receiver architecture for a multicarrier system. The design has one mixer stage with an IF frequency of about 170 MHz and also employs TI's GC5016 digital down converter (DDC). The DDC selects the desired carrier and generates an I/Q baseband signal from the complementary signal. The design also employs TI's CDC7005 clock synchronizer device.
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