EVM User's Guide: TPS65214EVM **TPS65214 Evaluation Module**



Description

The TPS65214EVM is designed to provide a quick setup to evaluate the TPS65214 power management IC (PMIC) and gain familiarity with the PMIC at a register level. The EVM has built-in configurability using headers and jumpers. A USB-C port allows for easy communication with the device through the onboard MSP432, along with an onboard USB-to-I²C adapter.

Get Started

- 1. Order the TPS65214EVM
- 2. Follow the provided link to access the GUI for online use in a browser or direct download of the desktop version: TPS65214-GUI
- 3. Connect the EVM hardware to the host computer using the USB-A to USB-C[®] cable included in the

EVM kit and apply input power to the board to enable I2C communication.

Features

- GUI support to read and write to device registers along with being able to view and export register data
- USB-A to USB-C connection for I2C communication

Applications

- Low power industrial MPUs such as AM62L
- Appliances, building security, EV charging infrastructure, fire safety systems, HMI, HVAC, industrial PCs, optical modules, patient monitoring and diagnostics, PLC, smart meters, test and measurement, video surveillance



TPS65214EVM

1

1 Evaluation Module Overview

1.1 Introduction

This user's guide describes the characteristics, operation, and use of the TPS65214 evaluation module (EVM). The TPS65214EVM is a fully assembly platform for evaluating the performance and functionality of the TPS65214 power management IC (PMIC). The EVM includes an onboard USB-to-I²C adapter, power terminals, and jumpers for all DC regulator inputs and outputs, as well as test points for common measurements.

1.2 Kit Contents

- TPS65214EVM Board
- USB-A to USB-C Cable

1.3 Specification



Copyright © 2023, Texas Instruments Incorporated

Figure 1-1. TPS65214 Functional Block Diagram



1.4 Device Information

The TPS65214 is a Power Management IC (PMIC) designed to supply a wide range of SoCs in both portable and stationary applications. The device is characterized across an ambient temperature range of -40°C to +105°C, making the PMIC an excellent choice for various industrial applications. The device includes three synchronous step-down DC-DC converters and two linear regulators.

2 Caution





3 Hardware

3.1 Requirements

This section lists the minimum hardware requirements needed to operate the EVM.

EVM

TPS65214 evaluation board.

Host Computer

A computer with an available USB port is required to make use of the EVM software. The EVM software runs on the computer and communicates with the EVM via a USB-A to micro-B cable.

Power Supply

An input voltage source capable of supplying 5V.

3.2 TPS65214 Resources Overview

The TPS65214 PMIC has multiple analog and digital resources that can be configured to power different processors, FPGAs and SoCs. Table 3-1 and Table 3-2 summarize some of the key electrical spec specification for the analog rails, the possible supply configurations and programmable features for each regulator. Table 3-1, TPS65214 Power Resources

| | 10010 0 | | 500011000 | |
|----------------------------------|----------------------------|----------------------------|------------------|------------------|
| | Buck1 | Buck 2 and 3 | LDO1 | LDO2 |
| Input voltage range | 2.5V to 5.5V | 2.5V to 5.5V | 1.4V to 5.5V | 1.4V to 5.5V |
| Output voltage range | 0.6V to 3.4V | 0.6V to 3.4V | 0.6V to 3.3V | 0.6V to 3.3V |
| Operating current | Maximum of 2A | Maximum of 1A | 300mA | 500mA |
| Current limiting | 5.7A to 6.9A | 3.9A to 4.7A | 600A to 900mA | 400A to 900mA |
| Status monitoring | UV, NEG_OC, OC, SCG, RV | UV, NEG_OC, OC, SCG, RV | UV, OC, SCG, RV | UV, OC, SCG, RV |
| Rail configuration | Buck converter | Buck converter | LDO; load switch | LDO; load switch |
| Short-Circuit Threshold (SCG) | 220mV to 300mV | 220mV to 300mV | 220mV to 300mV | 220mV to 300mV |

TPS65214 Multifunction Pins

TPS65214 has three multifunctional pins that can be configured depending on functional use. Table 3-2 shows the functions available for each of these pins as well as how these functions are configured and operated.

Note Only one of the following pins, MODE/RESET or MODE/STBY, can be configured as MODE. If both are configured as MODE, then MODE/RESET takes priority and MODE/STBY is be ignored.

| Pin Name | Pin Configuration | Operation |
|-------------|---|--|
| GPIO/VSEI | GPIO Configurable as an input or an output through the GPIO_CONFIG bit in the GENERAL_CONFIG register. | For detailed operation, see GPIO/VSEL configured as <i>GPIO</i> section in the TPS65214 Integrated Power Management IC for ARM Cortex Processors data sheet |
| | VSEL The pin level is used to set the output voltage of Buck1 or Buck3 through the VSEL_RAIL bit in the MFP_1_CONFIG register. | For detailed operation, see GPIO/VSEL configured as 'VSEL' section in the TPS65214 Integrated Power Management IC for ARM Cortex Processors data sheet |
| MODE/STBY | MODE Forces buck converters into PWM or permits auto- entry in PFM-mode | Pin status determines the switching mode of the buck converters. |
| | STBY Low power mode | Disables selected rails. Assert pin low for longer than Both MODE and STBY can be combined. Level sensitive. |
| GPO/nWAKEUP | GPO | |
| | nWAKEUP | |

Table 3-2 TPS65214 Multifunctional Pins

3.3 EVM Configuration

The following sections outline how to configure the TPS65214EVM for general experimentation.

EVM Configuration

The TPS65214EVM can be configured as follows:

- 1. Configure regulator input supply rails for the expected application using the jumpers indicated in the *Supply Voltage Setup*
- 2. Configure the multi-function pins externally using the mode configuration descriptions indicated in *Multi-Function pin setup*. Please note that the default configuration for regulator choice in SD or DDR voltage selection can differ for each individual NVM configuration (polarity is configurable).
- 3. Connect VSYS to a power supply capable of supporting the application and enable the supply. Typical supply for TPS6521401 is 5V.
- 4. If using a version of TPS65214 configured for First Supply Detection (FSD), then the power-up sequence is executed as soon as the 5V supply is connected to VSYS.

3.3.1 Default EVM Configuration

This section describes the default configuration programmed on the TPS6521401 PMIC.

The TPS65214EVM comes with the TPS6521401 PMIC installed, which is one of the orderable part numbers of the TPS65214 device family. Table 3-3 shows the default jumper configuration that can be used to evaluate the PMIC performance. For reference, Figure 3-1 demonstrates the output voltages and jumper location on the EVM. This information is based on the programmed default configuration on the TPS6521401EVM. The EVM can be used to evaluate other TPS65214 variants. External passive components and jumper configuration can be needed to be changed if the PMIC is reconfigured or replaced with a different orderable.

For more information about the settings that can be re configured and the I2C registers associated, refer to the TPS65214 Integrated Power Management IC for ARM Cortex Processors data sheet and TPS6521401 Technical Reference Manual (TRM).

The TPS65214EVM is designed to demonstrate some of the potential uses of the PMIC family. The EVM has more limitations than the TPS65214x device.



| - | Table 3-3. TPS | S65214EVM Default Jum | per Configuration |
|--------------------------|----------------|-------------------------------|---|
| | | Header | Jumper Default Position |
| Supply voltage setup | J6, J7 | PRE_REG/ EXT_SUPPLY/ USB_V | Set up to supply system voltage with an external supply from VSYS input |
| | J25 | PRE-REG VOUT | Set up for pre-regulator to output 3.3V |
| VIO voltage setup | J8 | VIO | Set up to supply VIO with external 3.3V LDO |
| | J30 | EXT_LDO_VIN | Set up to supply the external 3.3V LDO with VSYS |
| Multi-function pin setup | J11 | GPIO_VSEL | High = ON (default EVM config) Low = OFF |
| | J14 | MODE_STBY | High = ACTIVE state (default EVM config) Low = STBY state |



Figure 3-1. TPS65214EVM Default Configuration









* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 3-3. TPS6521401 Power-Down Sequence

7



3.3.2 Configuration Headers

The TPS65214EVM has multiple headers that can be used to change the input supply for some of the power rails. The PCB also includes headers that allows changing specific functions of the PMIC using the multi-function pins. Table 3-4 lists all the headers and the expected configuration for each selection. For reference, the header locations and configuration options are shown in Figure 3-4.

| | Header Name | Description | Configuration |
|-----|--------------------|--------------------------------|---|
| | | VSYS | J6-1, J6-3 VSYS supplied by PRE-REG output (3.3V / 5V) |
| J6 | PRE_REG/EXT_SUPPLY | Input source selection | J6-5 , J6-7 VSYS supplied by external supply at VSYS input (J5) |
| J7 | USB_5V | VSYS Input source selection | J7-1 VSYS supplied by USB input |
| 10 | N/IO | VIO | J8-1 VIO supplied by external 3.3V LDO |
| J8 | VIO | source select | J8-3 VIO supplied by BUCK2 output |
| 111 | | High/Low selection for GPIO/ | J11-1 Sets GPIO/VSEL pin HIGH. Effect is dependent on configuration as GPIO or VSEL |
| JII | GFIO_VSEL | VSEL pin | J11-3 Sets GPIO/VSEL pin LOW. Effect is dependent on configuration as GPIO or VSEL |
| 114 | MODE STRY | High/Low selection for | J14-3 Sets MODE/STBY pin HIGH. Effect is dependent on configuration as MODE, STBY, or both |
| 514 | MODE_STRI | MODE/STBY pin | J14-1 Sets MODE/STBY pin LOW. Effect is dependent on configuration as MODE, STBY, or both |
| J30 | EXT_LDO_VIN | External 3.3V LDO Input | External LDO supplied by VSYS |
| J31 | PMIC_EN | PMIC enable | PMIC enable pin if EN/PB/VSENSE is configured as EN |

| Tahlo | 3_1 | TDS6521/ | Configuration | Hoadore |
|-------|------|----------|---------------|---------|
| rable | J-4. | 12303214 | Configuration | neauers |



Figure 3-4. TPS65214EVM Header Configurations



3.3.3 Test Points

The EVM contains additional headers that can serve as test points for voltage and current sense measurements. Trace assignments to the test points are shown in Table 3-5.

| | Header Name | Associated Trace |
|-----|-------------|--------------------|
| J3 | USB_5V_S | USB Input SENSE |
| | | GND |
| J9 | LDO1_S | LDO1 Output SENSE |
| | | GND |
| J12 | LDO2_S | LDO2 Output SENSE |
| | | GND |
| J15 | BUCK3_S | BUCK3 Output SENSE |
| | | GND |
| J16 | BUCK1_S | Buck1 Output SENSE |
| | | GND |
| J17 | BUCK2_S | BUCK2 Output SENSE |
| | | GND |
| J34 | GND | GND connection |
| J35 | GND | GND connection |
| J36 | GND | GND connection |

Table 3-5. TPS65214 EVM Test Points



4 Software

4.1 Graphical User Interface (GUI)

The TPS65214-GUI can be used in the browser or as a standalone application. This software provides a simple way to communicate with the device via I2C using the built-in USB2ANY utilizing an MSP432. Details on the GUI installation and setup process are provided in this section. Note that the EVM can power up and operate without use of software.

This section covers the usage and capabilities of the TPS65214 Graphical User Interface (GUI) tool from Texas Instruments.

4.1.1 Getting Started

Getting started involves the following steps:

- 1. Find the GUI within the Gallery
- 2. Download the required software
 - a. TI Cloud Agent for running the GUI from a web browser
 - b. An offline copy of the GUI
- 3. Launch the GUI

4.1.1.1 Finding the GUI

The PMIC GUI is based upon GUI Composer which is compatible with either Chrome[™] or Firefox[™]. The Chrome[™] web browser is recommended and used throughout this document for demonstration. The PMIC GUI is also compatible with Microsoft Edge[™]. The GUI is found through the TI Development tools at TI DevTools page. Navigating to the Gallery from the Tools tab, highlighted in blue in Figure 4-1, is one way to enter the Gallery.

| 👂 Ti developer zone | Tools Help | Logini | Register |
|--|--|--|----------|
| TI developer zo Access all the development tools, soft | CCS Cloud Edge AI Cloud Gallery GUI Composer Resource Explorer SysConfig | sily develop, debug and analyze code on your desktop or in the cloud. | |
| Get started select a board or device Common actions Create a new project with Code Composer stud | ♥ UniFlash io~ Cloud IDE | Browse software and examples with Resource Explorer Download the Code Composer Studio* IDE and start development on your desktop | |
| | | ← Show all available tools | |
| About TI | Quick links | Buying Connect with us | |

Figure 4-1. GUI Composer Gallery



In the gallery, locate the TPS65214-GUI panel shown in Figure 4-2 by using the search bar and entering TPS65214-GUI.

| | Gallery | | Login / register |
|-----|---|--|---|
| | | Search | Q |
| | We've found 1 result(s) for "TPS65214-GUI" | | |
| | | | |
| | TPS65214-GUI Version 1.0.3 by PMIC (8roup) | | |
| | Graphical User Interface for the TPS65214 PMIC. | | |
| | (3) (3) ≛ (3) 103 Wees | | |
| | | | |
| | | | |
| Das | alboards, Applications, and Components are distributed with a TSPA license. | | |
| -10 | Texas Instruments | Copyright 1995-2025 Texas Instruments Incorpo Trademarks Privacy Policy Cookie Policy Ter | insted. All rights reserved. ms of Use Terms of Sale |
| | | | |

Figure 4-2. Locating the PMIC GUI in the Gallery

4.1.1.2 Downloading the Required Software

Both the standalone GUI and the GUI Composer Runtime are available from the PMIC panel. Again, the TI Cloud Agent enables the GUI to be run through a web browser but requires an internet connection to be able to run the GUI. By contrast, the standalone GUI is much larger but does not require an internet connection.

The download options are found in the pop-up window, as shown in Figure 4-3, when the cursor is placed on the download icon. The upper three options offer a standalone download for the appropriate operating system, while the lower three are for the GUI Composer Runtime.



Figure 4-3. GUI Software Download Options



4.1.1.3 Launching the GUI

After the appropriate software has been downloaded, the GUI can be launched locally from the PC application or from the TI Cloud using the Gallery. To use the TI Cloud version of the GUI, simply click anywhere in the panel, shown in Figure 4-4, that is not associated with the download or information icons.



Figure 4-4. GUI Panel Within the Gallery

Figure 4-5 shows an example of the PC application.

| est match for apps | |
|--|-------------------------------------|
| P 7PS65214-GUI 1.0.3 App | (=) |
| pps | TPS65214-GUI 1.0.3 |
| TPS65214-GUI-1.0.3.setup-win.exe > | |
| TPS65214-GUI 1.0.3 Release Notes | 🖸 Open |
| uninstall_TPS65214-GUI.exe | Run as administrator |
| ore | ○ Open file location ◇ Pin to Start |
| TPS65214-GUI - Search for apps in the Microsoft Store | 🔗 Pin to taskbar |
| | 间 Uninstall |
| | |
| | |
| | |
| | |
| | |

Figure 4-5. PMIC GUI Desktop Application



4.1.1.4 Connecting to the EVM

The GUI displays the Home page, shown in Figure 4-6. With the buttons displayed on the Home page, users can navigate to the other GUI pages which are described in the subsequent sections. These pages can also be found on the left side of the GUI interface.



Figure 4-6. GUI Home Page

4.1.2 Collateral Page

The Collateral page, shown in Figure 4-7, contains the functional block diagram for the TPS65214 PMIC device.







4.1.3 Register Map Page

The Register Map page (shown in Figure 4-8) lists the different registers available for configuration and is intended for direct reads and writes to the PMIC registers. Reading and writing registers can be done individually or all at once. An Auto Read feature can be enabled by using the drop-down menu next to the **READ ALL REGISTERS** button to select an automatic read timing. Use the search bar at the top of the page to search registers by name or address.

The first three columns under the search bar show the name of each register, followed by the hexadecimal address and data value. The *Bits* column contains the bit values for each register and can be hidden by unchecking the *Show Bits* box at the top of the page, under the *READ ALL REGISTERS* button. Double-clicking a bit in this section changes the bit value.

The Field View section on the right side of the page shows register bits grouped by the respective control blocks. Users can click on the question mark icon next to the bit field label for an expanded view with more detail on the bit field. This function also highlights the corresponding bit boxes in yellow in the *Bits* column. Each field has a name shown by the blue text at the top of each box. These names can be found using the search bar by checking the *Search Bitfields* box to the right of the search bar.

In the *Immediate Write* mode (toggle option located at the top right of the page), write buttons are grayed out since individual registers are written immediately with each change in the Field View, change in bits, or change in hexadecimal value. In *Deferred Write* mode, the writing of a single register or all registers is deferred until the *WRITE REGISTER* or *WRITE ALL REGISTERS* button is selected.

| egister Map | Set Write Mode to 'Defer' Unlock Registers | Registers Locked Off | 🗸 Read Read all | Write Write all |
|----------------------------|--|----------------------|-----------------------|-----------------|
| Search registers by name | | | Search bitfields Fiel | d View |
| | Register Name | Address - Value | _ Bits - DEVIC | CE / TI_DEV_ID |
| DEVICE | | | 7 6 5 4 3 2 1 0 TI_DE | VICE_ID[7:0] () |
| ti dev id | | 0×00 0×14 | 0 0 0 1 0 1 0 0 0 | 0x14 |
| nym id | | 0x00 0x14 | 0 0 0 0 0 0 0 1 | |
| enable ctri | | 0x01 0x01 | 1 1 0 1 1 1 | |
| reg lock | | 0x02 0x07 | | |
| Ido1_vout_stby | | 0x04 0x1A | - 0 0 1 1 0 1 0 | |
| ldo1_vout | | 0x05 0x1A | - 0 0 1 1 0 1 0 | |
| Ido2_vout | | 0x06 0x05 | 0 - 0 0 0 1 0 1 | |
| Ido2_vout_stby | | 0x07 0x05 | - 0 0 0 0 1 0 1 | |
| b3_vout | | 0x08 0x14 | 0 0 0 1 0 1 0 0 | |
| b2_vout | | 0x09 0x24 | 0 0 1 0 0 1 0 0 | |
| b1_vout | | 0x0A 0x86 | 10000110 | |
| Ido1_sequence_slot | | 0x0C 0x22 | - 0 1 0 0 0 1 0 | |
| Ido2_sequence_slot | | 0x0D 0x23 | - 0 1 0 0 0 1 1 | |
| b3_sequence_slot | | 0x0F 0x30 | - 0 1 1 0 0 0 0 | |
| b2_sequence_slot | | 0x10 0x22 | - 0 1 0 0 0 1 0 | |
| b1_sequence_slot | | 0x11 0x42 | - 1 0 0 0 1 0 | |
| nrst_sequence_slot | | 0x12 0x60 | - 1 1 0 0 0 0 0 | |
| gpio_sequence_slot | | 0x13 0x03 | 0 0 0 0 - 0 1 1 | |
| gpo_sequence_slot | | 0x15 0x30 | - 0 1 1 0 0 0 0 | |
| power_up_slot_duration_1 | | 0x16 0x89 | 10001001 | |
| power_up_slot_duration_2 | | 0x17 0x7C | 0 1 1 1 1 1 0 0 | |
| b3_vout_stby | | 0x19 0x00 | 0 0 0 0 0 0 0 | |
| power_down_slot_duration_1 | | 0x1A 0xCC | 1 1 0 0 1 1 0 0 | |
| power_down_slot_duration_2 | | 0x1B 0x00 | 0 0 0 0 0 0 0 | |
| b2_vout_stby | | 0x1C 0x00 | 0 0 0 0 0 0 0 | |
| b1 yout stby | | 0v10 0v00 | 0 0 0 0 0 0 0 | |

Figure 4-8. Register Map Page

Note

Read-only registers are grayed out and locked to prevent write attempts. Reserved register bits are shown as a dash mark.



4.1.4 Device Configuration Page

The Device Configuration page is the main feature of the GUI and highlights the configurability of the PMIC, as shown in Figure 4-9. On this page, register fields are grouped according to use case and are labeled to indicate which part of the PMIC is controlled by each block.

| Buck & LDO Config Digital PIn Config Mask Config Monitor PMIC Status Buck 1 Buck 2 Buck 3 LDO 1 LDO 2 output Voltage 0.750V 0utput Voltage 0.40put Voltage 1.00V 0utput Voltage 0.40put Voltage 0.40put Voltage 1.00V 0utput Voltage 0.40put Voltage 0.40put Voltage 1.00V 0utput Voltage 0.40put Current 400 mA 0.40put Current 600 mA 0.40put Current | Buck & LDO Config Mask Config Monitor PMIC Status Buck 1 Buck 2 Buck 3 LDO 1 LDO 2 0utput Voltage 0.750V 0utput Voltage 0utput Volta | Buck & LDD Config Digital Pin Config Mask Config Monitor PMIC Status Buck 1 Buck 2 Buck 3 LDD 1 LDD 2 output Voltage 0.750V 0utput Voltage 1.800V 0utput Voltage 1.100V 0utput Voltage 0utput Voltage 0utput Voltage 1.800V 0utput Voltage 0utput Voltage 1.800V 0utput Voltage 0utput Vo |
|--|--|--|
| Buck 1 Buck 2 Buck 3 LD0 1 LD0 2 output Voltage 0.750V output Voltage 1.800V output Voltage 1.100V output Voltage 1.800V output Voltage 0.750V Degltch Duration 20us egltch Duration 20us egltch Duration 20us output Voltage 1.800V output Voltage 0.750V Discharge 125 O Discharge 125 O Discharge 125 O output Voltage 1.800V output Voltage 0.750V Nu Ytneshold -5% Output Voltage 0.750V Discharge 250 O output Current 600 mA VU Ytneshold -5% VU Ytneshold -5% VU Ytneshold -5% output Tureshold -5% VU Ytneshold -5% VU Ytneshold -5% VU Ytneshold -5% VU Ytneshold -5% | Buck 1 Buck 2 Buck 3 LD0 1 LD0 2 output Voltage 0.750V output Voltage 1.800V output Voltage 0.750V Diglitch Duration 20us D | Buck 1 Buck 2 Buck 3 LD0 1 LD0 2 Output Voltage 0.0750V Output Voltage 1.800V Output Voltage 1.800V Output Voltage 0.0750V Output Voltage 0.800V Output Voltage 1.800V Output Voltage 0.0750V Output Voltage 0.0750V Output Voltage 1.800V Output Voltage 0.0750V Output Voltage 0.0750V Output Voltage 0.750V Output Voltage 0.0750V Output Volt |
| Output Voltage 0.750V Output Voltage 1.800V Output Voltage 1.100V Output Voltage 1.800V Output Voltage 0.750V Deglitch Duration 20us Deglitch Duration 20us Deglitch Duration 20us Output Voltage 1.100V Output Voltage 1.800V Output Voltage 0.750V Discharge 125 Ω Discharge 125 Ω Discharge 125 Ω Discharge 250 Ω Discharge 200 Ω Bandwidth Bandwidth Bandwidth Bandwidth Bandwidth Bandwidth Configuration LD0 Mode Configuration LD0 Mode Configuration LD0 Mode V// Threshold 5% V/// Threshold 5% V//// Threshold 5% V//// Threshold 5% V/// Threshold 5% <th>Output Voltage 0.750V Output Voltage 1.800V Output Voltage 1.800V Output Voltage 0.800V Output Voltage 0.750V Deglitch Duration 20us Deglitch Duration 20us Output Voltage 1.800V Output Voltage 0.750V Discharge 125 Ω Discharge 125 Ω Discharge 250 Ω Discharge 200 Ω Bandwidth Bandwidth Bandwidth Bandwidth Bandwidth Configuration LD0 Mode Configuration LD0 Mode UV Threshold 5% UV Threshold 5%</th> <th>Output Voltage 0.750V Output Voltage 1.80V Output Voltage 1.10V Output Voltage 1.80V Output Voltage 0.750V Deglitch Duration 20us Deglitch Duration 20us Deglitch Duration 20us Output Voltage 1.80V Output Voltage 0.750V Discharge 125 Ω Discharge 125 Ω Discharge 250 Ω Discharge 200 Ω Bandwidth Initial bandwidth Bandwidth Show UV Threshold 5% UV</th> | Output Voltage 0.750V Output Voltage 1.800V Output Voltage 1.800V Output Voltage 0.800V Output Voltage 0.750V Deglitch Duration 20us Deglitch Duration 20us Output Voltage 1.800V Output Voltage 0.750V Discharge 125 Ω Discharge 125 Ω Discharge 250 Ω Discharge 200 Ω Bandwidth Bandwidth Bandwidth Bandwidth Bandwidth Configuration LD0 Mode Configuration LD0 Mode UV Threshold 5% | Output Voltage 0.750V Output Voltage 1.80V Output Voltage 1.10V Output Voltage 1.80V Output Voltage 0.750V Deglitch Duration 20us Deglitch Duration 20us Deglitch Duration 20us Output Voltage 1.80V Output Voltage 0.750V Discharge 125 Ω Discharge 125 Ω Discharge 250 Ω Discharge 200 Ω Bandwidth Initial bandwidth Bandwidth Show UV Threshold 5% UV |
| Degltch Duration 20us Degltch Duration 20us Degltch Duration 20us Output Current 400 mA Duration Duration Duration 20us Output Current 400 mA Duration Duratio | Deglitch Duration 20us Deglitch Duration 20us Output Current 00mA Output Current 60mA Discharge 125 Ω Discharge 125 Ω Discharge 20 Ω Discharge 20 Ω Bandwidth Bandwidth Bandwidth Bandwidth Bandwidth Configuration LDO Mode Configuration Configuration LDO Mode Configuration LDO Mode V/ Threshold 5% V// Threshold 5% V/// Threshold 5% V/// Threshold 5% V/// Threshold 5% V/// Threshold 5% V//// Threshold 5% V//// Threshold 5% V//// Threshold 5% V//// Threshold 5% V/// Threshold 5% V/// Threshold 5% V/// Threshold 5% V/// Threshold 5% V | Deglitch Duration 20us Deglitch Duration 20us Deglitch Duration 20us output Current 400 mA Output Current 600 mA Discharge 125 Ω Discharge 125 Ω Discharge 125 Ω Discharge 20 Ω Discharge Discharge 20 Ω Discharge 20 Ω Discharge 20 Ω Discharge Discharge 20 Ω Discharge Discharge <td< td=""></td<> |
| Discharge 125 Ω Discharge 125 Ω Discharge 125 Ω Discharge 20 Ω Discharge Discharge 20 Ω Discharge Discharge 20 Ω Discharge Discharge <td>Discharge 125 Ω Discharge 125 Ω Discharge 25 Ω Discharge 20 Ω Bandwidth Nigh bandwidth Bandwidth Bandwidth Bandwidth Bandwidth Configuration LD0 Mode Configuration LD0 Mode Configuration LD0 Mode UV Threshold 5% UV Threshold</td> <td>Discharge 125 \Leftarrow Discharge 125 \Leftarrow Discharge 250 \Leftarrow Discharge 200 \Leftarrow Bandwidth Image Bandwidth Image Bandwidth Image Discharge 200 \Leftarrow Discharge 200 \Leftarrow UV Threshold 5% VV Threshold 5%</td> | Discharge 125 Ω Discharge 125 Ω Discharge 25 Ω Discharge 20 Ω Bandwidth Nigh bandwidth Bandwidth Bandwidth Bandwidth Bandwidth Configuration LD0 Mode Configuration LD0 Mode Configuration LD0 Mode UV Threshold 5% UV Threshold | Discharge 125 \Leftarrow Discharge 125 \Leftarrow Discharge 250 \Leftarrow Discharge 200 \Leftarrow Bandwidth Image Bandwidth Image Bandwidth Image Discharge 200 \Leftarrow Discharge 200 \Leftarrow UV Threshold 5% VV Threshold 5% |
| Bandwidth high bandwidth • Bandwidth Iow bandwidth • Configuration LDO Mode • | Bandwidth high bandwidth Bandwidth high bandwidth Configuration LD Mode Configuration LD Mode UV Threshold S% UV Threshold S% | Bandwidth high bandwidth > Bandwidth Iow bandwidth > Configuration LDO Mode > Configuration LDO Mode UV Threshold -5% > UV Threshold -5%< |
| UV Threshold -5% v UV Threshold -5% v UV Threshold -5% v DVS Transition No DVS transition V DVS Transition No DVS transition v DVS Transition No DVS transition v DVS Transition No DVS transition v DVS Transition No DVS transition v DVS Transition No DVS transition v v DVS Transition v VS Transition v VS Transition v v VS Transition v v VS Transition v | UV Threshold -5% v UV Threshold -5% | UV Threshold -5% v UV Threshold -5% |
| DVS Transition No DVS transition No DVS transition DVS Transition No DVS transition DVS Transition No DVS tran | DVS Transition No DVS transition v DVS transition v DVS transition v DVS transition No DVS transition | |
| | | DVS Transition No DVS transition No DVS transition DVS Transition No DVS t |
| Standby Voltage 0.600V v Standby Voltage 0.600V Standby Voltage 0.600V Standby Voltage 0.750V | Standby Voltage 0.600V v Standby Voltage 0.600 | Standby Voltage 0.600V v Standby Voltage 0.600V v Standby Voltage 0.600V v Standby Voltage 0.750V |
| Standby State Not enabled in STBY Mode v Standby State Enabled in STBY Mode v | Standby State Not enabled in STBY Mode v Standby State Enabled in STBY Mode v State Standby State Enabled in STBY Mode v State | Standby State Not enabled in STBY Mode 🔹 Standby State Enabled in STBY Mode |

Figure 4-9. Device Configuration Page

4.1.4.1 Configuration Fields

Register settings can be changed on the Device Configuration Page and follow the register write mode specified on the Register Map page (Immediate or Deferred).

The *BUCK & LDO Config* tab holds register settings for each power rail of the PMIC. (For more information on the Load Switch and BYPASS modes for the LDOs, refer to the TPS65214 Integrated Power Management IC for ARM Cortex Processors data sheet).

The *Digital Pins Config* tab is used to control settings for the enable configuration and digital I/O pins (For details on multi-function pins, see the TPS65214 Integrated Power Management IC for ARM Cortex Processors data sheet.

The *Mask Config* tab allows you to control fault reporting for PMIC protection features which includes masking for undervoltage, temperature, and interrupt signals.

The *Monitor PMIC Status* tab holds a collection of read-only status registers that show the power rail enables and interrupts, which are displayed as digital LEDs. This section provides fast visual feedback on the PMIC and the operating conditions.

4.1.4.2 Create and Load a Custom Configuration

The NVM Configuration page does not require hardware to develop an NVM configuration. Connection with an actual device is needed only when attempting to upload to a target device.

Once the registers are set to your desired configuration,go to the *File* tab at the top of the screen, to select a format for your configuration file (shown in Figure 4-10). A register configuration can be saved in either a CSV (Comma Separated Values), JSON (Javascript Object) format, or TXT (plain text file format). Next, use the *Save Register Map* option to download your saved configuration in your selected format.

To load an existing configuration into the NVM, use the *Load Register Map* option and browse to the configuration file location. Save an existing register map, or download the Device OTP file from the *OTP Validation* tab for an example of the accepted format of the configuration file.





Figure 4-10. Save and Load Register Options

4.1.5 NVM Programming Page

The NVM Programming page allows re-programming the device NVM memory to change the default register settings. This page includes four main functions that correspond to the buttons shown in Figure 4-11. The first two steps *I2C OFF REQUEST* and *ENABLE I2C COMMUNICATION* are only needed when re-programming the PMIC from the Initialize state (PMIC rails OFF).

- The I2C OFF REQUEST button triggers an OFF request though I2C and sends the PMIC to INITIALIZE state.
- The ENABLE I2C COMMUNICATION button enables I2C communication in INITIALIZE state.
- Once I2C communication is enabled, users can go to the NVM configuration page to select the desired register settings or use the *File* tab options to load a pre-configured JSON or CSV file.
- The NVM PROGRAMMING button programs the selected register settings into the NVM.
- The VALIDATE NVM PROGRAMMING button reads the NVM content and compares with the selected register settings. The result (PASS or FAIL) is stored in register 0x34, field 7 CUST_NVM_VERIFY_ERR.

| ^v rogram Device | | |
|------------------------------|--|---|
| | I2C OFF REQUEST | 0 |
| | ENABLE 12C COMMUNICATION | ٥ |
| o to the 'Device Config' tab | -> Update NVM fields Update NVM fields | |
| | NVM PROGRAMMING | 0 |
| | | |
| ad bit 'CUST_NVM_VERIFY | VALIDATE NYM PROGRAMMING | Ø |
| ead bit 'CUST_NVM_VERIFY | VALIDATE NYM PROGRAMMING | ٥ |

Figure 4-11. NVM Programming Page

4.1.6 Additional Features

In the Options tab at the top of the GUI interface, you can select *Serial Port* to display information about the EVM connection to your computer.

DEXAS INSTRUMEN



4.1.7 Connecting the EVM using USB2ANY

First, take a look at the USB2ANY Interface Adapter User's Guide to make sure that the USB2ANY adapter has the proper firmware and components. Additional information on the adapter pin functions is included in the document.

To connect the EVM to a computer using the USB2ANY adapter, plug the ribbon cable from the USB2ANY into the J2 header on the EVM. The ribbon cable is keyed at both ends to make sure that all the pins are connected correctly. Plug the USB cable extending from the other side of the USB2ANY into a computer. The GUI automatically connects to the computer.



5 Hardware Design Files

5.1 TPS65214EVM Schematic



Figure 5-1. TPS65214EVM, Schematic Page 1





Figure 5-2. TPS65214EVM, Schematic Page 2







Figure 5-3. TPS65214EVM, Schematic Page 3



5.2 TPS65214EVM PCB Layers



Figure 5-4. TPS65214EVM Top Layer



Figure 5-5. TPS65214EVM Ground Layer 1



Figure 5-6. TPS65214EVM Signal Layer 1



Figure 5-7. TPS65214EVM Signal Layer 2





Figure 5-8. TPS65214EVM Ground Layer 2



Figure 5-9. TPS65214EVM Bottom Layer

5.3 Bill of Materials

Table 5-1. Bill of Materials

| Designator | Quantity | Description | Package Reference | Part Number | Manufacturer |
|---|----------|---|-------------------|----------------------|--------------|
| C1 | 1 | CAP, CERM, 3300pF, 50V, +/- 10%, X7R, 0603 | 603 | C0603C332K5RACTU | Kemet |
| C2, C4 | 2 | CAP, CERM, 12pF, 50V,+/- 5%, C0G/ NP0, AEC-Q200 Grade 1, 0402 | 402 | CGA2B2C0G1H120J050BA | TDK |
| C3 | 1 | CAP, CERM, 10uF, 10V, +/- 10%, X7R, 0805 | 805 | GCM21BR71A106KE22L | MuRata |
| C5, C11, C13, C14, C17, C18, C19, C20 | 8 | CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, 0402 | 402 | GCM155R71C104KA55D | MuRata |
| C6, C7, C8, C9, C10, C12, C15, C16, C21, C25 | 10 | CAP, CERM, 2.2uF, 6.3V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603 | 603 | GCM188R70J225KE22D | MuRata |
| C23, C24 | 2 | CAP, CERM, 22uF, 10V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206 | 1206 | GCM31CR71A226KE02L | MuRata |
| C26 | 1 | CAP, CERM, 0.22µF, 16V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402 | 402 | GCM155R71C224KE02D | MuRata |
| C27 | 1 | Cap Ceramic Multilayer 4.7uF 6.3V DC 10% SMD Paper T/R | 603 | GCJ188C70J475KE02J | Murata |
| C28, C29, C30 | 3 | Chip Multilayer Ceramic Capacitors for General Purpose, 0805, 4.7uF, X7R, 15%, 10%, 10V | 805 | GRM21BR71A475KE51L | Murata |
| C31 | 1 | CAP, CERM, 4.7uF, 10V, +/- 10%, X7S, 0603 | 603 | C1608X7S1A475K080AC | TDK |
| C32, C33, C35 | 3 | CAP, CERM, 2.2uF, 10V, +/- 10%, X7S, 0402 | 402 | C1005X7S1A225K050BC | TDK |
| C34, C36, C46, C47, C48 | 5 | Cap Ceramic 10uF 6.3V X7R ±10% SMD 1206 +125°C Embossed T/R | 1206 | CL31B106KQHNFNE | Samsung |
| C37, C38, C39, C42 | 4 | CAP, CERM, 22uF, 10V, +/- 20%, X7R, 0805 | 805 | GRM21BZ71A226ME15L | MuRata |
| C49 | 1 | CAP, AL, 100uF, 63V, +/- 20%, 0.35 ohm, AEC-Q200 Grade 2, SMD | SMT Radial G | EEE-FK1J101P | Panasonic |
| C50, C51, C59, C60 | 4 | CAP, CERM, 0.47uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603 | 603 | CGA3E3X7R1H474K080AE | TDK |
| C52, C54 | 2 | CAP, CERM, 10uF, 50V, +/- 10%, X5R, 1210 | 1210 | C3225X5R1H106K250AB | TDK |
| C53, C55, C57 | 3 | CAP, CERM, 2.2uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805 | 805 | CGA4J3X7R1H225K125AB | TDK |
| C56, C58 | 2 | CAP, CERM, 0.47uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603 | 603 | CGA3E3X7R1H474K080AB | TDK |
| C61 | 1 | CAP, CERM, 1uF, 16V, +/- 20%, X7R, AEC-Q200 Grade 1, 0603 | 603 | GCM188R71C105MA64D | MuRata |



| Designator | Quantity | Description | Package Reference | Part Number | Manufacturer |
|--|----------|---|--|----------------------|-----------------------------|
| C62 | 1 | CAP, CERM, 0.1uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402 | 402 | CGA2B3X7R1H104K050BB | TDK |
| C63 | 1 | CAP, CERM, 0.15uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603 | 603 | CGA3E3X7R1H154K080AB | TDK |
| C64 | 1 | CAP, CERM, 10pF, 50V, +/- 5%, C0G/ NP0, AEC-Q200 Grade 1, 0603 | 603 | CGA3E2C0G1H100D080AA | TDK |
| C65, C69 | 2 | CAP, CERM, 2.2µF, 10V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603 | 603 | GRM188R71A225KE15J | MuRata |
| C66, C67 | 2 | CAP, CERM, 47µF, 10V,+/- 10%, X7S, AEC-Q200 Grade 1, 1210 | 1210 | GCM32EC71A476KE02K | MuRata |
| C68 | 1 | CAP, AL, 100µF, 16V, +/- 20%, AEC- Q200 Grade 3, SMD | D8xL6.2mm | EEE-1CA101AP | Panasonic |
| D1, D2, D3, D4, D5 | 5 | LED, Blue, SMD | BLUE 0603 LED | LB Q39G-L2N2-35-1 | OSRAM |
| FB1 | 1 | Chip Ferrite Bead, 1206, 120Ω at 25%, 6A | 1206 | BLM31KN121SZ1L | Murata |
| H1, H2, H3, H4 | 4 | Bumpon, Hemisphere, 0.44 X 0.20, Clear | Transparent Bumpon | SJ-5303 (CLEAR) | 3M |
| J1 | 1 | Receptacle, 0.5mm, USB TYPE C, R/A, SMT | Receptacle, 0.5mm, USB TYPE C, R/A, SMT | 12401610E4#2A | Amphenol Canada |
| J2 | 1 | Header (shrouded), 100mil, 5x2, High- Temperature, Gold, TH | 5x2 Shrouded header | N2510-6002-RB | 3M |
| J3, J7, J9, J12, J15, J16, J17, J30, J31, J34, J35, J36 | 12 | Header, 100mil, 2x1, Gold, TH | Header, 100mil, 2x1, TH | HTSW-102-07-G-S | Samtec |
| J5, J10, J13, J18, J20, J22, J24 | 7 | Terminal Block, 2x1, 5mm, Green, TH | Terminal Block, 2x1, 5mm, TH | 1935776 | Phoenix Contact |
| J6 | 1 | Header, 2.54mm, 4x2, Gold, TH | Header, 2.54mm, 4x2, TH | TSW-104-08-L-D | Samtec |
| J8, J11, J14 | 3 | Header, 100mil, 3x1, Gold, TH | 3x1 Header | TSW-103-07-G-S | Samtec |
| J25 | 1 | Header, 100mil, 3x1, Gold, TH | PBC03SAAN | PBC03SAAN | Sullins Connector Solutions |
| J26, J27, J28 | 3 | JUMPER TIN SMD | 6.85x0.97x2.51 mm | S1911-46R | Harwin |
| J29 | 1 | Header, 100mil, 7x1, Gold, TH | 7x1 Header | TSW-107-07-G-S | Samtec |
| L1, L2, L3 | 3 | Thin Film Power Inductor 0.47uH 20% 4.5A 29mOhm 0805 | 805 | TFM201208BLE-R47MTCF | ТDК |
| L4 | 1 | Inductor, Wirewound, 1uH, 7.3A, 0.013 ohm, SMD | 5.7x2.8x5.2mm | 74437336010 | Wurth Elektronik |
| L5 | 1 | 680nH Shielded Molded Inductor 8A 12mOhm Max 2-SMD | SMD2 | 7.44373E+11 | Wurth Electronics |
| LBL1 | 1 | | PCB Label 0.650 x 0.200 inch | THT-14-423-10 | Brady |
| Q1. Q2 | 2 | MOSFET. N-CH. 50V. 0.22A. SOT-23 | SOT-23 | BSS138 | Fairchild Semiconductor |



| Designator | Quantity | Description | Package Reference | Part Number | Manufacturer |
|--|----------|---|-------------------|------------------|---------------------------|
| R1, R2, R9 | 3 | RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04024K87FKED | Vishay-Dale |
| R3 | 1 | RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW0402100RJNED | Vishay-Dale |
| R4, R7, R14 | 3 | RES, 1.0M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04021M00JNED | Vishay-Dale |
| R5, R6, R46, R47 | 4 | RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04021K00JNED | Vishay-Dale |
| R8, R11, R17, R18, R19, R20 | 6 | RES, 1.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04021K20JNED | Vishay-Dale |
| R10, R12, R29, R30, R31, R32, R33, R34, R35, R36, R39, R41, R48, R49, R50, R54, R55 | 17 | RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW040210K0JNED | Vishay-Dale |
| R13 | 1 | RES, 383 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW0402383KFKED | Vishay-Dale |
| R15, R21, R22, R37, R38, R40, R43, R51, R52, R53, R64 | 11 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04020000Z0ED | Vishay-Dale |
| R16 | 1 | RES, 200 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW0402200KJNED | Vishay-Dale |
| R44, R60, R65, R68 | 4 | RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW0603100KFKEA | Vishay-Dale |
| R56 | 1 | RES, 1.00, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW06031R00FKEA | Vishay-Dale |
| R57 | 1 | RES, 187 k, 1%, 0.1 W, 0603 | 603 | RC0603FR-07187KL | Yageo |
| R58 | 1 | RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060349K9FKEA | Vishay-Dale |
| R62 | 1 | RES, 21.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060321K0FKEA | Vishay-Dale |
| R63 | 1 | RES, 6.81 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW06036K81FKEA | Vishay-Dale |
| R66 | 1 | RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | RMCF0603ZT0R00 | Stackpole Electronics Inc |
| R67 | 1 | RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060349R9FKEA | Vishay-Dale |
| R69 | 1 | RES, 43.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060343K2FKEA | Vishay-Dale |
| R70 | 1 | RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW06034K99FKEA | Vishay-Dale |



| Designator | Quantity | Description | Package Reference | Part Number | Manufacturer |
|---|----------|---|---------------------------------------|-----------------------|-----------------------------|
| R71 | 1 | RES, 59.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060359K0FKEA | Vishay-Dale |
| SH-J1, SH-J2, SH-J3, SH- J4, SH-J5, SH-J6, SH-J7 | 7 | Shunt, 100mil, Flash Gold, Black | Closed Top 100mil Shunt | SPC02SYAN | Sullins Connector Solutions |
| SW1 | 1 | Switch Tactile N.O. SPST Round Button J-Bend 32VAC 32VDC 1VA 100000Cycles 3N SMD Tube/T/R | SMT_SW_7MM1_6MM3 | KT11P3JM34LFS | C&K Components |
| U1 | 1 | Integrated Power Management IC for ARM Cortex®—Low Power Processors and FPGAs | WQFN-HR24 | PTPS6521401VAFR | Texas Instruments |
| U2 | 1 | 4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6) | DRY0006A | TPD4S012DRYR | Texas Instruments |
| U3 | 1 | Automotive Catalog, Dual, 200mA, Low- IQ Low-Dropout Regulator for Portable Devices, DSE0006A (WSON-6) | DSE0006A | TLV7103318QDSERQ1 | Texas Instruments |
| U4 | 1 | Low-Capacitance 6-Channel +/-15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8) | RSE0008A | TPD6E004RSER | Texas Instruments |
| U5 | 1 | 8-BIT BIDIRECTIONAL LOW-VOLTAGE TRANSLATOR, PW0020A (TSSOP-20) | PW0020A | SN74GTL2003PWR | Texas Instruments |
| U6 | 1 | Quad Low Voltage, Rail-to-Rail Comparator, Open-drain output, TSSOP14 | TSSOP14 | LM339LVPWR | Texas Instruments |
| U7 | 1 | Linear Voltage Regulator IC 1 Output 500mA 6-WSON (2x2) | WSON6 | TPS74533PQWDRVRQ1 | Texas Instruments |
| U8 | 1 | MSP432E401YTPDT, PDT0128A (TQFP-128) | PDT0128A | MSP432E401YTPDTR | Texas Instruments |
| U9 | 1 | LM62460RPHR, RPH0016A (VQFN- HR-16) | RPH0016A | LM62460RPHR | Texas Instruments |
| Y1 | 1 | Crystal, 25MHz, 20ppm, AEC-Q200 Grade 1, SMD | 2.5x3.2mm | ECS-250-12-33Q-JES-TR | ECS Inc. |
| C22 | 0 | CAP, Polymer Hybrid, 100uF, 25V, +/- 20%, 30 ohm, 6.3x7.7 SMD | 6.3x7.7 | EEHZC1E101XP | Panasonic |
| C40, C41 | 0 | CAP, CERM, 22uF, 10V, +/- 20%, X7R, 0805 | 805 | GRM21BZ71A226ME15L | MuRata |
| C43, C44, C45 | 0 | 47μF ±20% 10V Ceramic Capacitor X7R 1210 (3225 Metric) | 1210 | GRM32ER71A476ME15L | Murata |
| J4 | 0 | Header (Shrouded), 1.27mm, 5x2, Gold, SMT | Header(Shrouded), 1.27mm, 5x2, SMT | FTSH-105-01-F-DV-K | Samtec |
| J19, J21, J23, J32, J33 | 0 | SMA Jack, Straight, 50 Ohm, Gold, TH | TH, 5-Leads, Body 7x7mm | SMA-J-P-H-ST-TH1 | Samtec |
| J38, J39, J40, J41, J42 | 0 | Header, 100mil, 2x1, Gold, TH | Header, 100mil, 2x1, TH | HTSW-102-07-G-S | Samtec |

| Designator | Quantity | Description | Package Reference | Part Number | Manufacturer |
|---------------------------------|----------|---|-------------------|------------------|--------------|
| R23, R24, R25, R26, R27, R28 | 0 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04020000Z0ED | Vishay-Dale |
| R45 | 0 | RES, 47.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060347K0FKEA | Vishay-Dale |
| R59, R61 | 0 | RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW0603100KFKEA | Vishay-Dale |



6 Additional Information

6.1 Trademarks

Chrome[™] is a trademark of Google. Firefox[™] is a trademark of Mozilla. Microsoft Edge[™] is a trademark of Microsoft. USB-C[®] is a registered trademark of USB Implementers Forum. All trademarks are the property of their respective owners.

STANDARD TERMS FOR EVALUATION MODULES

- 1. Delivery: TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
- 2 Limited Warranty and Related Remedies/Disclaimers:
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

- 3.3 Japan
 - 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けて

いないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの 措置を取っていただく必要がありますのでご注意ください。

- 1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用 いただく。
- 2. 実験局の免許を取得後ご使用いただく。
- 3. 技術基準適合証明を取得後ご使用いただく。
- なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。 上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿6丁目24番1号

西新宿三井ビル

- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧くださ い。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html
- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 EVM Use Restrictions and Warnings:

- 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
- 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
- 4.3 Safety-Related Warnings and Restrictions:
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and inability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
- 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
- 5. Accuracy of Information: To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
- 6. Disclaimers:
 - 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
 - 6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.
- 7. USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS. USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

www.ti.com

- 8. Limitations on Damages and Liability:
 - 8.1 General Limitations. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.
 - 8.2 Specific Limitations. IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.
- 9. Return Policy. Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.
- 10. Governing Law: These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2023, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated