User's Guide

TPS61288EVM-064 Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and the use of the TPS61288EVM-064 evaluation module (EVM). The EVM contains the TPS61288 device, which is a high-performance, high-efficiency synchronous boost converter which integrates two low on resistance power FETs. This user's guide includes EVM specifications, recommended test setup, test results, schematic diagram, bill of materials, and the board layout.

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1 Introduction

1.1 Performance Specification

Table 1-1 provides a summary of the TPS61288 EVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1-1. Performance Specification Summary

Parameter	Test Condition	MIN	TYP	MAX	Unit
V_{IN}		2.7	3.6	8.8	V
V_{OUT}	V_{IN} = 3.5 V, I_O < 2.3 A	12.66	12.92	13.17	V
Default Switching Frequency			500		kHz

1.2 Modification

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. The external component can be changed according to the real application.

2 Connector, Test Point and Jumper Descriptions

This section describes how to properly connect, set up, and use the TPS61288EVM-064.

2.1 Connector and Test Point Descriptions

This EVM includes I/O connectors and test points as shown in Table 2-1. The power supply must be connected to input connectors, J1 and J2. The load must be connected to output connectors, J3 and J4.

Table 2-1. Connectors and Test Points

Reference Designator	Description
J1	Input voltage positive connection
J2	Input voltage return connection
J3	Output voltage positive connection
J4	Output voltage return connection
TP1	VIN_S+ is for positive input voltage sensing
TP2	VIN_S- is for negative input voltage sensing
TP3	VO_S+ is for positive output voltage sensing
TP4	VO_S- is for negative output voltage sensing
TP5	Bode+ is for bode plot measurement connection
TP6	Bode- is for bode plot measurement connection
TP7	Test point to measure SW pin waveform

2.2 Jumper Configuration

JP1 (VIN Control)

The JP1 jumper connects the control VIN with power VIN. By default, this jumper is set to the ON position. Take off the jumper for a user-defined voltage.

2.2.1 JP2 (Enable)

The JP2 jumper enables the device. By default, this jumper is set to the VCC position. Put this jumper in the GND position to disable the output.

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3 Schematic, Bill of Materials, and Board Layout

This section provides the TPS61288EVM-064 schematic, bill of materials (BOM), and board layout.

3.1 Schematic

Figure 3-1 shows the schematic of the TPS61288EVM-064.

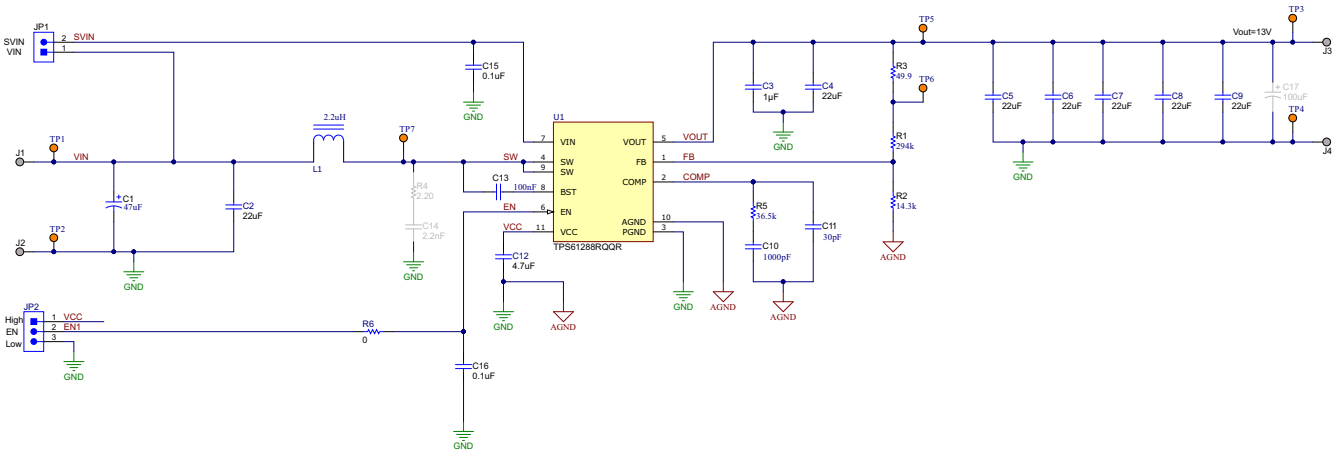

Figure 3-1. TPS61288EVM-064 Schematic

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3.2 Bill of Materials

Table 3-1 lists the BOM of the TPS61288EVM-064.

Table 3-1. Bill of Materials

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	47 µF	CAP, CERM, 22 µF, 25 V, ± 10%, X7R, 1210	7343-31	T495D476M025ATE120	Kemet
C2, C4, C5, C6, C7, C8, C9	7	22 µF	CAP, CERM, 22 µF, 25 V, ± 10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata
C3	1	1 µF	CAP, CERM, 1 µF, 50 V, ± 20%, X5R, AEC-Q200 Grade 3, 0603	0603	GRT188R61H105ME13D	MuRata
C10	1	1000 pF	CAP, CERM, 1000 pF, 50 V, ± 10%, X5R, 0402	0402	GRM155R61H102KA01D	MuRata
C11	1	30 pF	CAP, CERM, 30 pF, 50 V, ± 5%, C0G/NP0, 0402	0402	GRM1555C1H300JA01D	MuRata
C12	1	4.7 µF	CAP, CERM, 4.7 µF, 10 V, ± 10%, X5R, 0603	0603	0603ZD475KAT2A	AVX
C13	1	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, 0603	0603	GCM188R71H104KA57D	MuRata
C15, C16	2	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104K050BB	TDK
J1, J2, J3, J4	4		Terminal, Turret, TH, Double	Keystone1502-2	1502-2	Keystone
JP1	1		Header, 100 mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
JP2	1		Header, 100 mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
L1	1		Fixed Inductor 2.2 µH 20% 100 kHz 19.5A 4.5mΩ	SMT_IND_11MM15_10MM0	CMLE105T-2R2MS	Cyntec
R1	1	294k	RES, 294 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402294KFKED	Vishay-Dale
R2	1	14.3k	RES, 14.3 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040214K3FKED	Vishay-Dale
R3	1	49.9	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040249R9FKED	Vishay-Dale
R5	1	36.5k	RES, 36.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040236K5FKED	Vishay-Dale
R6	1	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
SH-JP1, SH-JP2	2		Shunt, 100mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone

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Table 3-1. Bill of Materials (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
U1	1		Fully Integrated Synchronous Boost Converter	VQFN-HR11	TPS61288RQQR	Texas Instruments
C14	0	2200 pF	CAP, CERM, 2200 pF, 250 V, ± 10%, X7R, 0805	0805	GRM21AR72E222KW01D	MuRata
C17	0	100 µF	CAP, Polymer Hybrid, 100 µF, 25 V, ± 20%, 30 Ω, 6.3x7.7 SMD	6.3x7.7	EEHZA1E101XP	Panasonic
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R4	0	2.20	RES, 2.20, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8RQF2R2V	Panasonic

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3.3 Board Layout

The TPS61288EVM board is a 4-layer PCB. The top and bottom layers copper thickness is 2-oz. The two inner layers copper thickness is 1-oz. Figure 3-2 and Figure 3-5 show the top view and bottom view, respectively. Figure 3-3 and Figure 3-4 show the inner layer 1 and inner layer 2, respectively.

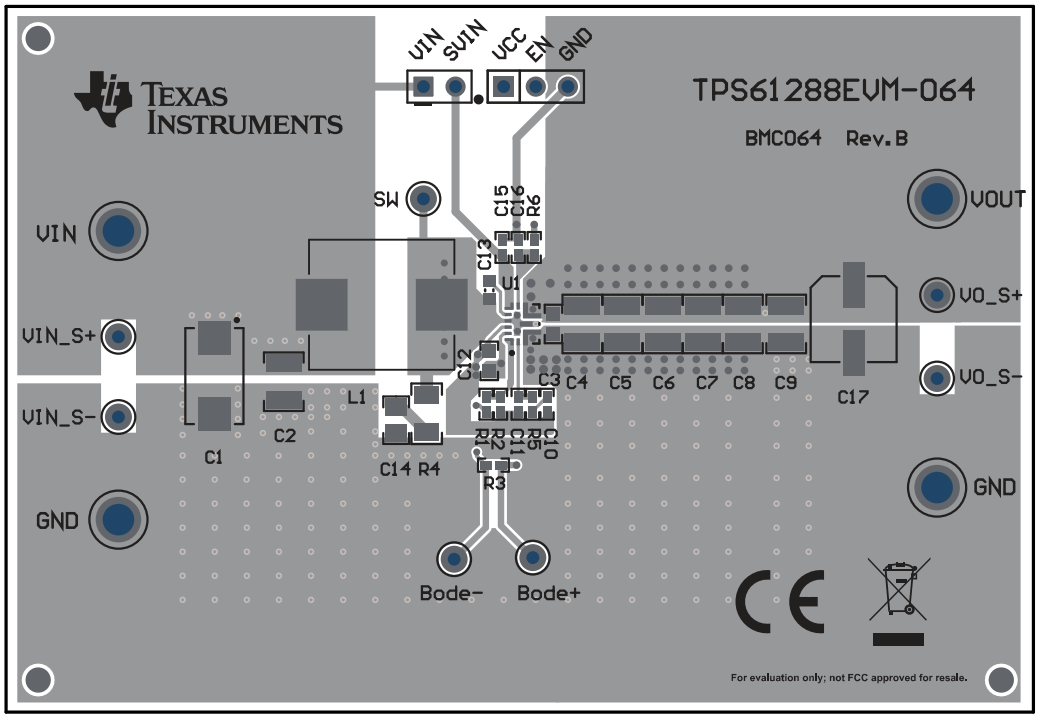

Figure 3-2. TPS61288EVM-064 Top-Side Layout

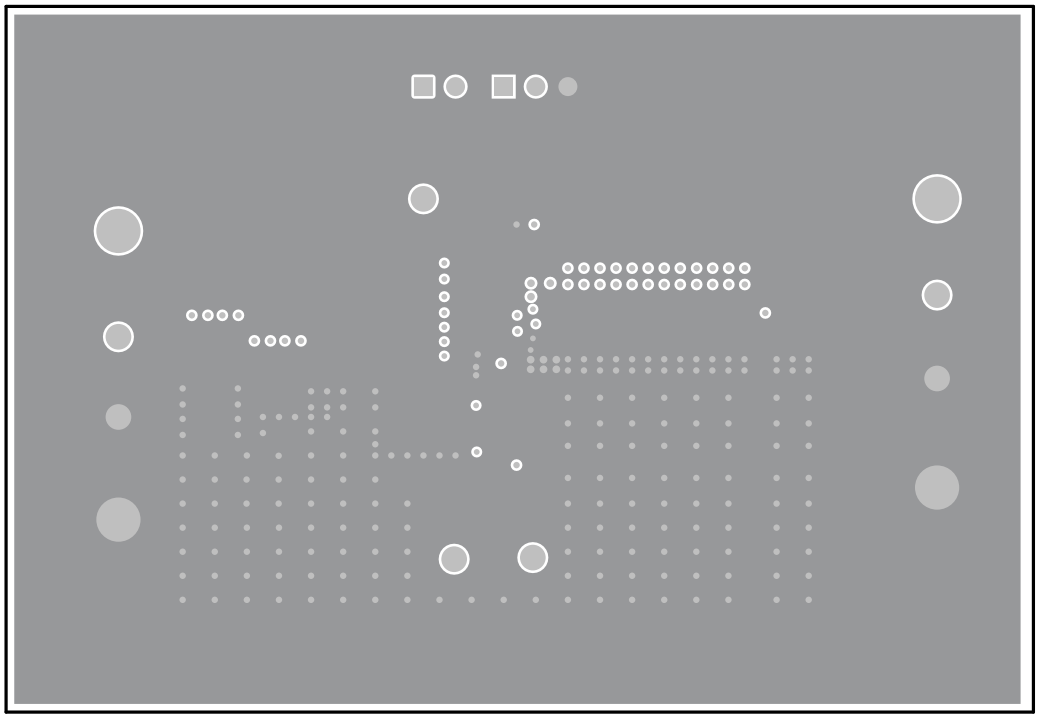

Figure 3-3. TPS61288EVM-064 Inner Layer1 Layout

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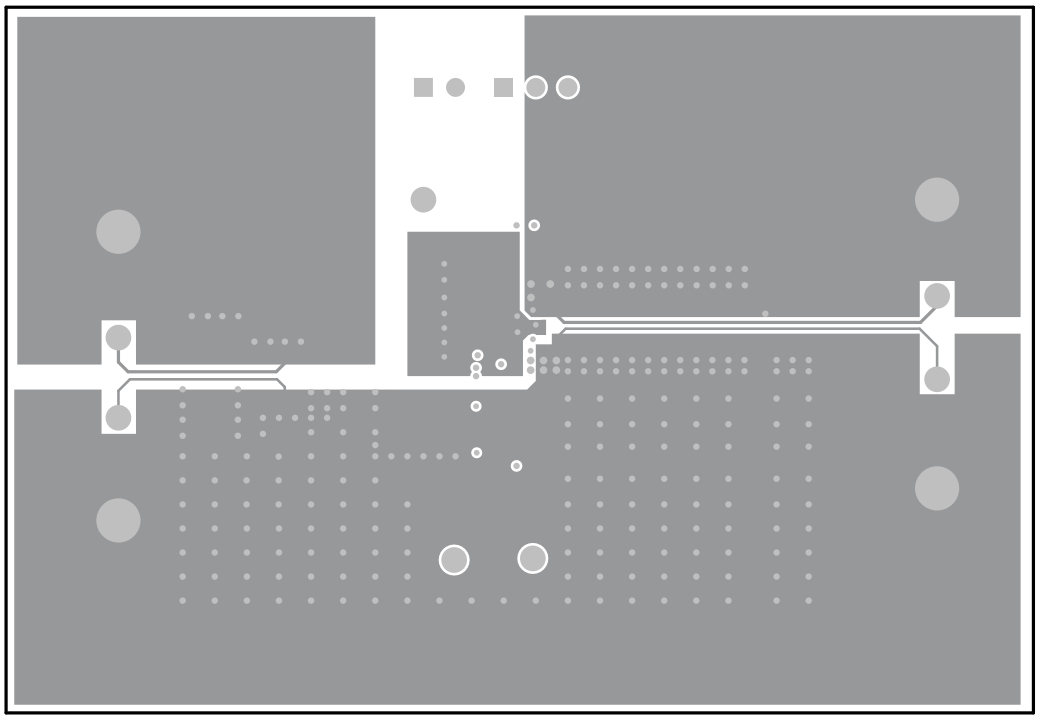

Figure 3-4. TPS61288EVM-064 Inner Layer2 Layout

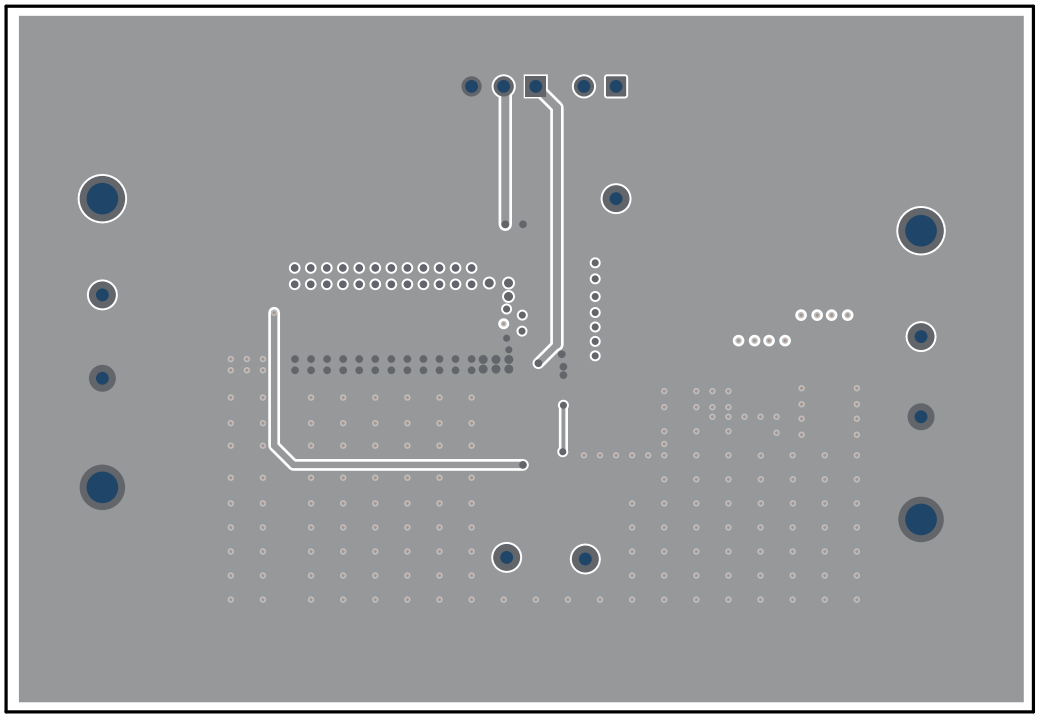

Figure 3-5. TPS61288EVM-064 Bottom-Side Layout

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2020) to Revision A (December 2020)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Update was made in Section 3.1	3
• Update was made in Section 3.2	4
• Update was made in Section 3.3	6

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