

TPS54623 Step-Down Converter Evaluation Module User's Guide



ABSTRACT

This user's guide contains background information for the TPS54623 as well as support documentation for the TPS54623EVM-012 evaluation module (PWR012-002). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54623EVM-012.

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1 Introduction

1.1 Background

The TPS54623 DC/DC converter is designed to provide up to a 6-A output. The TPS54623 implements split-input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V whereas the control input (VIN) is rated for 4.5 V to 17 V. The TPS54623EVM-012 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in [Table 1-1](#). This evaluation module is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54623 regulator. The switching frequency is externally set at a nominal 480 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54623 package along with the gate drive circuitry. The low, drain-to-source on-resistance of the MOSFET allows the TPS54623 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54623 provides adjustable slow start, tracking, and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS54623EVM-012.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54623EVM-012	VIN = 8 V to 17 V (VIN start voltage = 6.521 V)	0 A to 6 A

1.2 Performance Specification Summary

A summary of the TPS54623EVM-012 performance specifications is provided in [Table 1-2](#). Specifications are given for an input voltage of $V_{IN} = 12$ V and an output voltage of 3.3 V, unless otherwise specified. The TPS54623EVM-012 is designed and tested for $V_{IN} = 8$ V to 17 V with the VIN and PVIN pins connected by the J5 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54623EVM-012 Performance Specification Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} voltage range (PVIN = VIN)		8	12	17	V
V_{IN} start voltage			6.528		V
V_{IN} stop voltage			6.19		V
Output voltage set point			3.3		V
Output current range	$V_{IN} = 8$ V to 17 V	0		6	A
Line regulation	$I_O = 3$ A, $V_{IN} = 8$ V to 17 V		± 0.02		%
Load regulation	$V_{IN} = 12$ V, $I_O = 0$ A to 6 A		± 0.013		%
Load transient response	$I_O = 1.5$ A to 4.5 A	Voltage change	-150		mV
		Recovery time	200		μ s
	$I_O = 4.5$ A to 1.5 A	Voltage change	150		mV
		Recovery time	200		μ s
Loop bandwidth	$V_{IN} = 12$ V, $I_O = 1.9$ A		44.7		kHz
Phase margin	$V_{IN} = 12$ V, $I_O = 1.9$ A		54		°
Input ripple voltage	$I_O = 6$ A		420		mVPP
Output ripple voltage	$I_O = 6$ A		18		mVPP
Output rise time			6		ms
Operating frequency			480		kHz
Maximum efficiency	TPS54623EVM-012, $V_{IN} = 8$ V, $I_O = 2$ A		94.9		%

1.3 Modifications

These evaluation modules (EVM) are designed to provide access to the features of the TPS54623. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The output voltage is set by the resistor divider network of R6 and R7. R6 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R7. Changing the value of R7 can change the output voltage above 0.6 V. The value of R7 for a specific output voltage can be calculated using Equation 1.

$$R7 = \frac{10 \text{ k}\Omega \times 0.6 \text{ V}}{V_{\text{OUT}} - 0.6 \text{ V}} \quad (1)$$

Table 1-3 lists the R7 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on time is greater than 120 ns, and the maximum duty cycle is less than 95%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

OUTPUT VOLTAGE (V)	R7 VALUE (kΩ)
1.8	4.99
2.5	3.16
3.3	2.21
5	1.37

1.3.2 Slow-Start Time

The slow-start time can be adjusted by changing the value of C9. Use Equation 2 to calculate the required value of C9 for a desired slow-start time

$$C9(\text{nF}) = \frac{T_{\text{SS}}(\text{ms}) \times I_{\text{SS}}(\mu\text{A})}{V_{\text{REF}}(\text{V})} \quad (2)$$

The EVM is set for a slow-start time of approximately 6 ms using $C9 = 0.022 \mu\text{F}$.

1.3.3 Track In

The TPS54623 can track an external voltage during start-up. The J6 connector is provided to allow connection to that external voltage. Ratiometric or simultaneous tracking can be implemented using resistor divider R5 and R6. See the TPS54623 data sheet (SLVSA70) for details.

1.3.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 6.528 V and a stop voltage of 6.190 V using $R1 = 35.7 \text{ k}\Omega$ and $R2 = 8.06 \text{ k}\Omega$. Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

$$R1 = \frac{V_{\text{START}} \left(\frac{V_{\text{ENFALLING}}}{V_{\text{ENRISING}}} \right) - V_{\text{STOP}}}{I_p \left(1 - \frac{V_{\text{ENFALLING}}}{V_{\text{ENRISING}}} \right) + I_h} \quad (3)$$

$$R2 = \frac{R1 \times V_{\text{ENFALLING}}}{V_{\text{STOP}} - V_{\text{ENFALLING}} + R1(I_p + I_h)} \quad (4)$$

1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected using a jumper across J5. The single input voltage is supplied at J1. If desired, these two input voltage rails may be separated by removing the jumper across J5. Two input voltages must then be provided at both J1 and J4.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54623EVM-012 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS54623EVM-012 is provided with input/output connectors and test points as shown in [Table 2-1](#). A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The jumper across J5 must be in place. See [Section 1.3.5](#) for split-input voltage rail operation. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability must be 6 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP5 as the ground reference.

Table 2-1. EVM Connectors and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	PVIN input voltage connector (see Table 1-1 for V_{IN} range.)
J2	V_{OUT} , 3.3 V at 6 A maximum
J3	2-pin header for enable. Connect EN to ground to disable, open to enable.
J4	VIN input voltage connector. Not normally used
J5	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
J6	2-pin header for tracking voltage input and ground
J7	2-pin header for tracking output and ground
TP1	PVIN test point at PVIN connector
TP2	GND test point at PVIN connector
TP3	Output voltage test point at VOUT connector
TP4	PH test point
TP5	GND test point at VOUT connector
TP6	Test point between voltage divider network and output. Used for loop response measurements. Slow start/track in test point
TP7	COMP pin test point
TP8	VIN test point at VIN connector
TP9	GND test point at VIN connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 2 A and then decreases as the load current increases toward full load. [Figure 2-1](#) shows the efficiency for the TPS54623EVM-012 at an ambient temperature of 25°C.

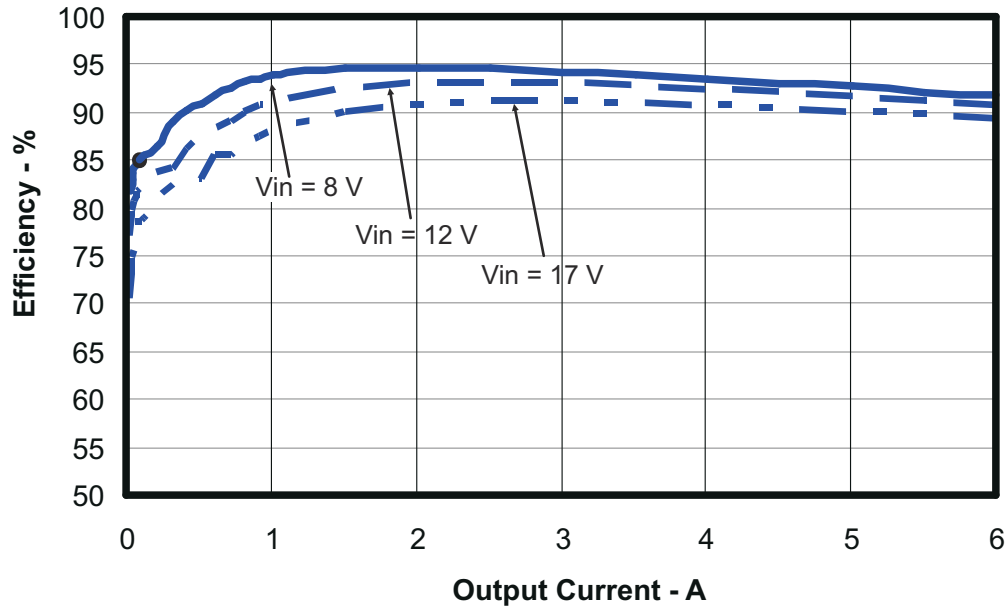


Figure 2-1. TPS54623EVM-012 Efficiency

[Figure 2-2](#) shows the efficiency for the TPS54623EVM-012 using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

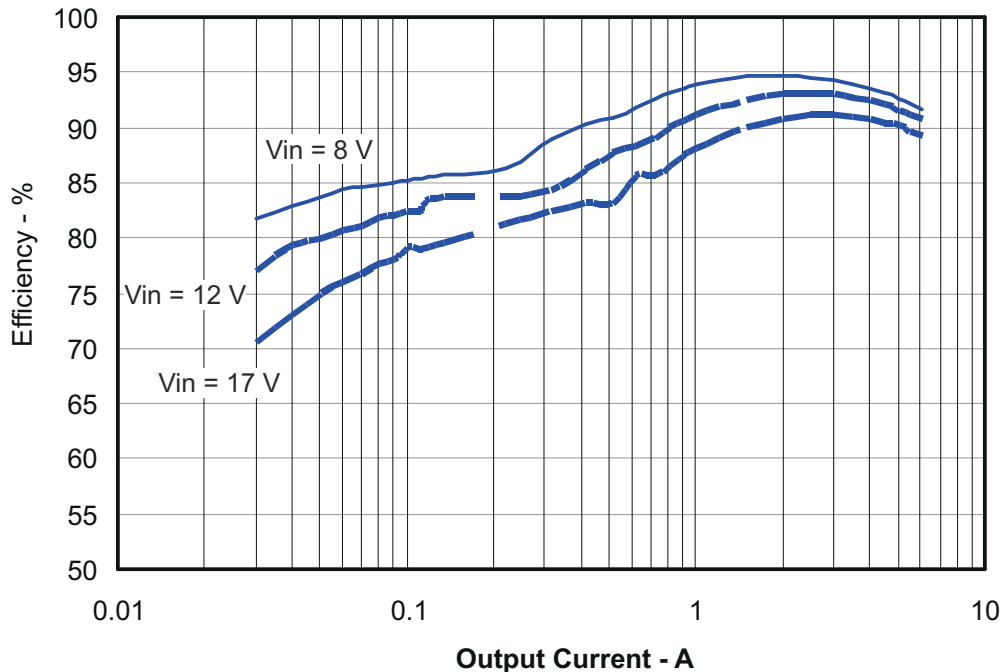


Figure 2-2. TPS54623EVM-012 Low-Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54623EVM-012.

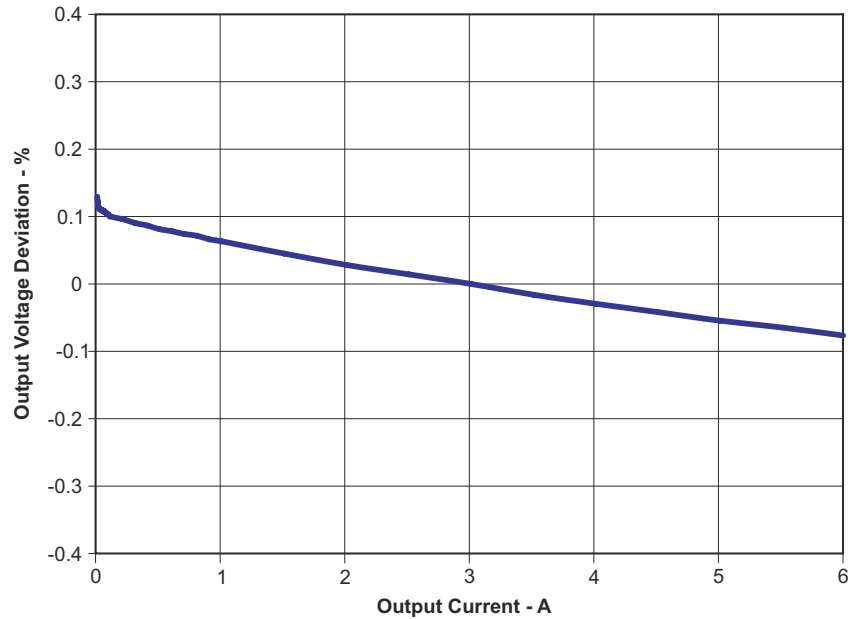


Figure 2-3. TPS54623EVM-012 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54623EVM-012.

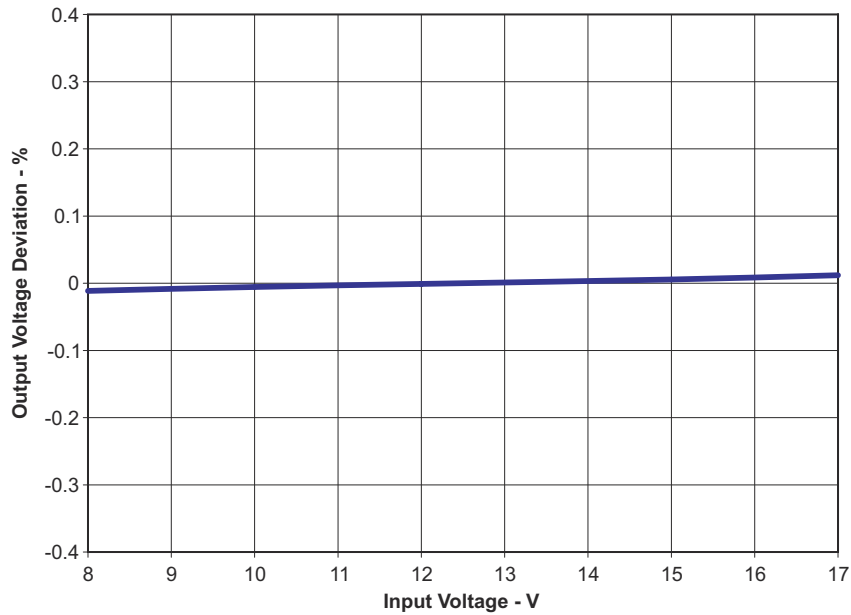


Figure 2-4. TPS54623EVM-012 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54623EVM-012 response to load transients. The current step is from 25% to 75% of maximum rated load at 12-V input. The current step slew rate is 100 mA/μs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

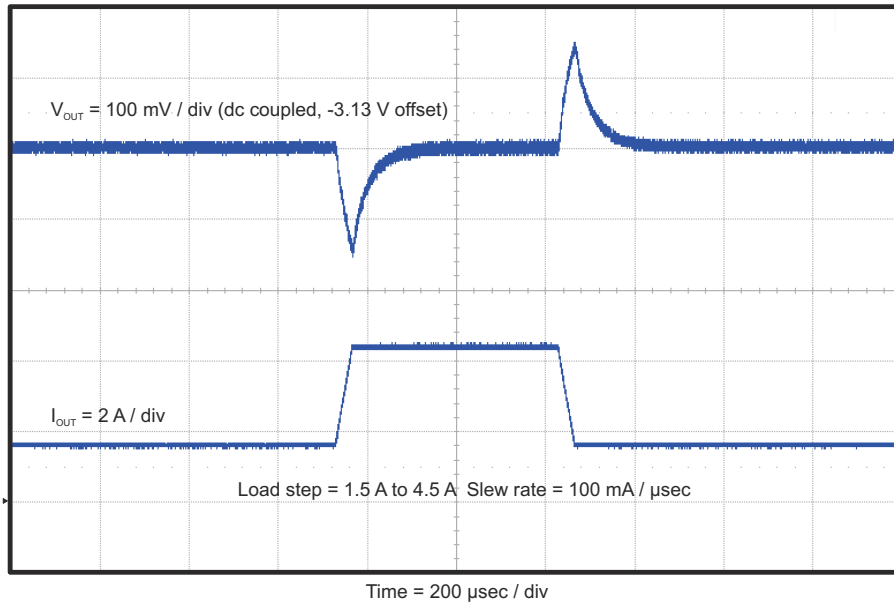


Figure 2-5. TPS54623EVM-012 Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54623EVM-012 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 1.9 A.

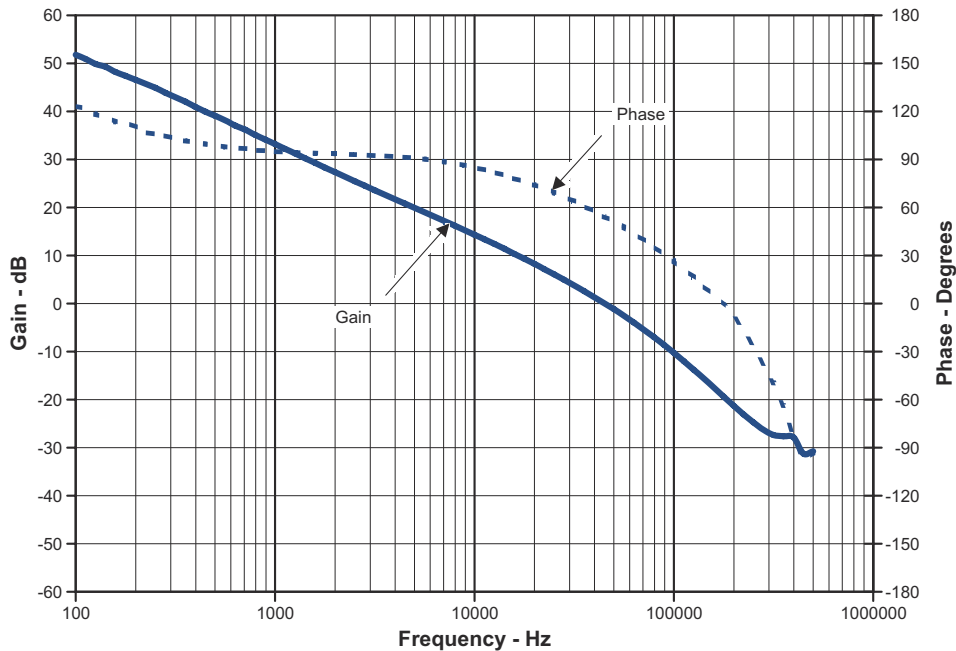


Figure 2-6. TPS54623EVM-012 Loop Response

2.7 Output Voltage Ripple

Figure 2-7 shows the TPS54623EVM-012 output voltage ripple. The output current is the rated full load of 6 A and $V_{IN} = 12$ V. The ripple voltage is measured directly across the output capacitors.

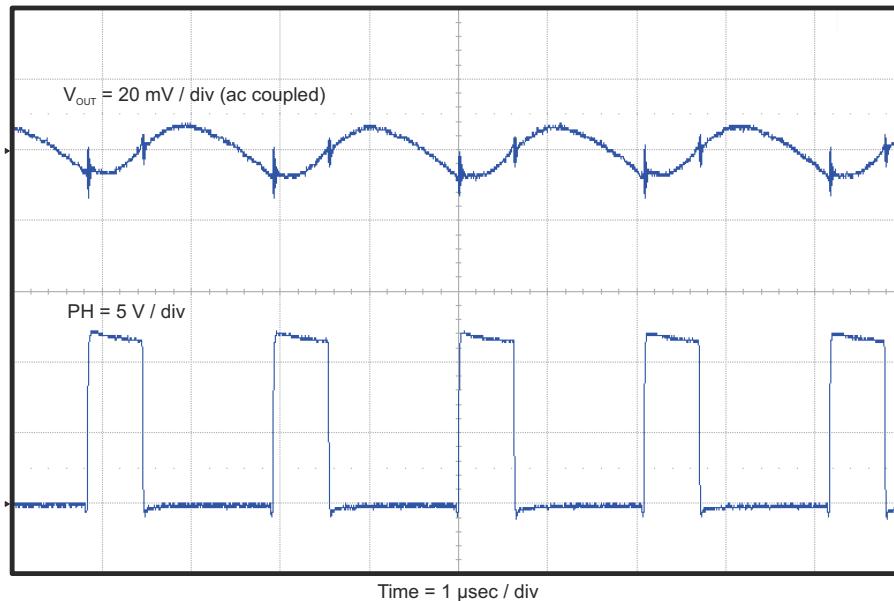


Figure 2-7. TPS54623EVM-012 Output Ripple

2.8 Input Voltage Ripple

Figure 2-8 shows the TPS54623EVM-012 input voltage. The output current is the rated full load of 6 A and $V_{IN} = 12$ V. The ripple voltage is measured directly across the input capacitors.

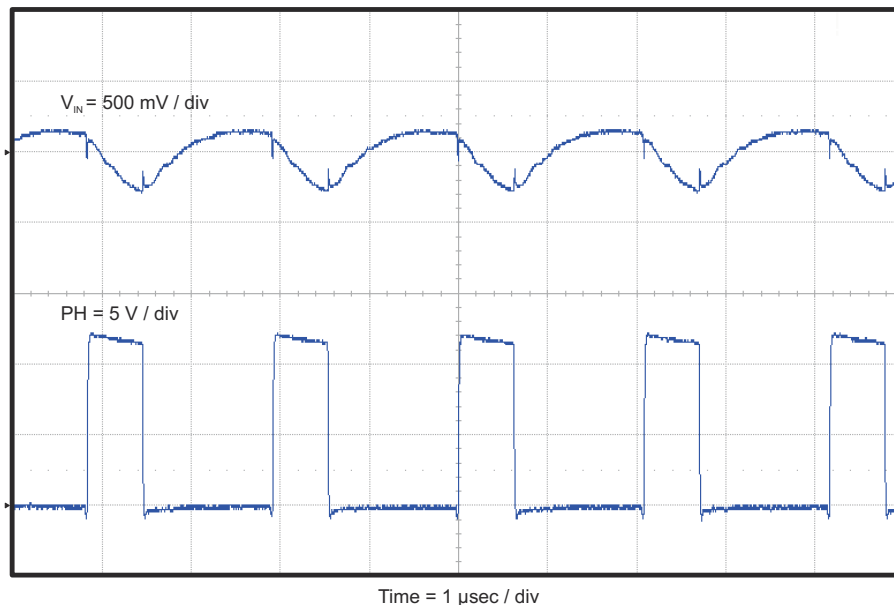


Figure 2-8. TPS54623EVM-012 Input Ripple

2.9 Powering Up

Figure 2-9 and Figure 2-10 show the start-up waveforms for the TPS54623EVM-012. In Figure 2-9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 2-10, the input voltage is initially applied and the output is inhibited by using a jumper at J3 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 12 V and the load is 1 Ω .

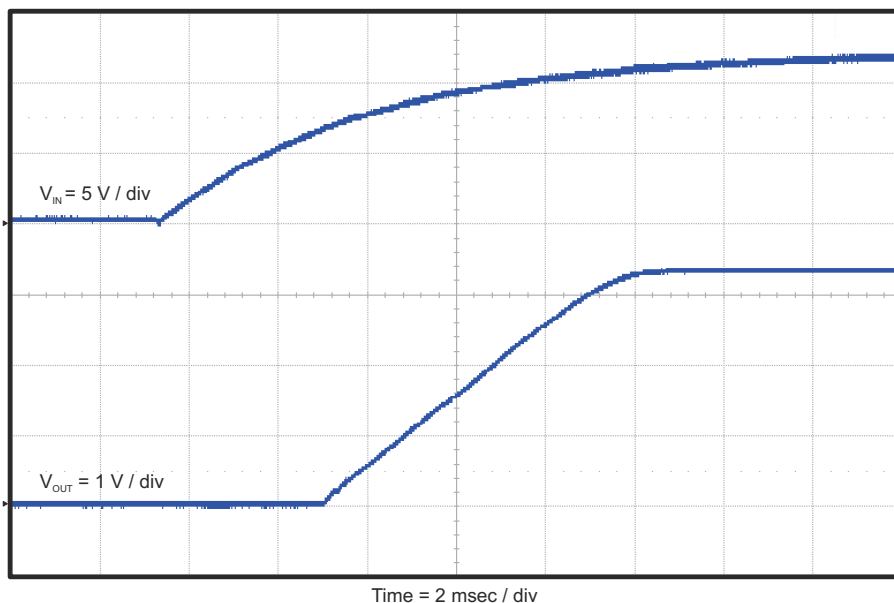


Figure 2-9. TPS54623EVM-012 Start-Up Relative to V_{IN}

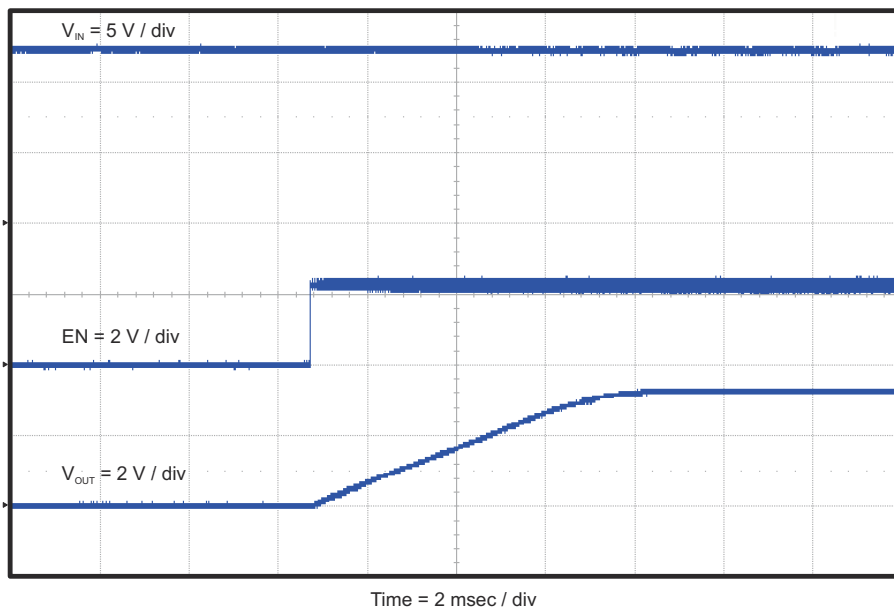


Figure 2-10. TPS54623EVM-012 Start-Up Relative to Enable

2.10 Prebias Start-Up

The TPS54623 is designed to start up into a prebiased output. The output voltage is not discharged to ground at the beginning of the slow-start sequence. [Figure 2-11](#) shows the start-up waveform with the output voltage prebiased to 1 V.

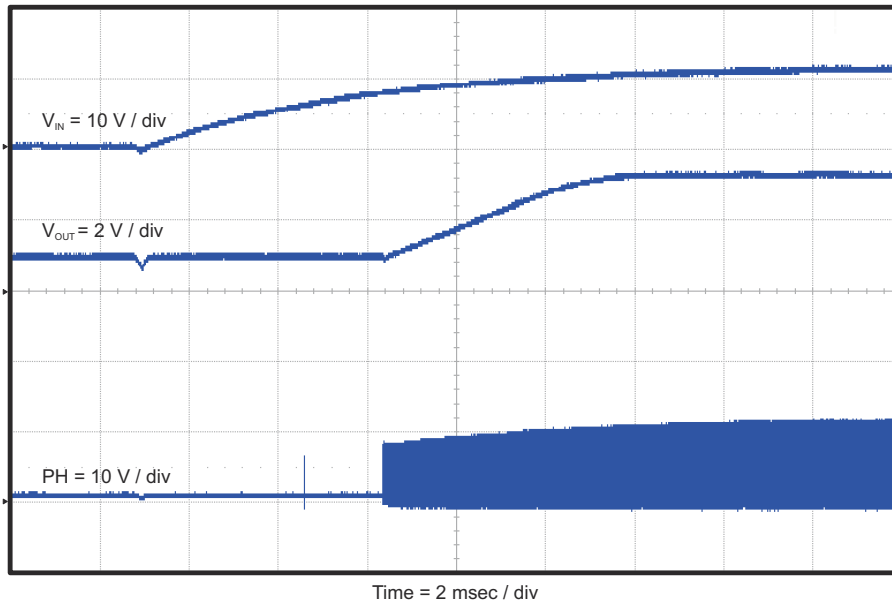


Figure 2-11. TPS54623EVM-012 Start-Up Into Prebias

2.11 Hiccup Mode Current Limit

The TPS54623 features hiccup mode current limit. When an overcurrent event occurs, the TPS54623 shuts down and restarts. [Figure 2-12](#) shows restart sequence in an overcurrent condition.

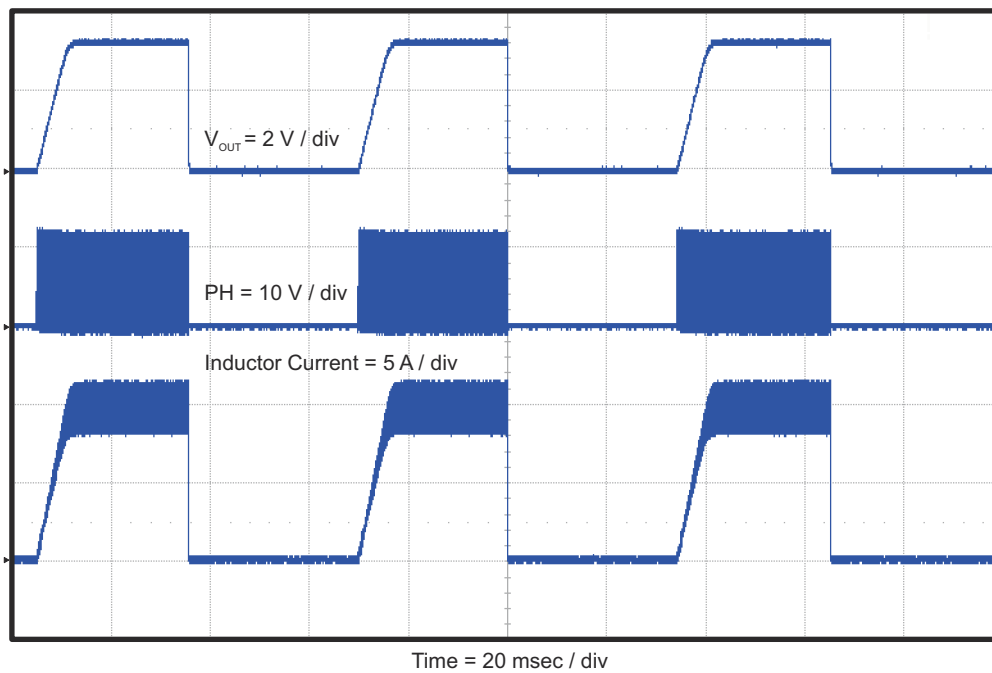


Figure 2-12. TPS54623EVM-012 Hiccup Mode Current Limit

3 Board Layout

This section provides a description of the TPS54623EVM-012 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54623EVM-012 is shown in [Figure 3-1](#) through [Figure 3-5](#). The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for PVIN, VIN, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54623 and a large area filled with ground. The bottom and internal ground layers contain ground planes only. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board including two vias directly under the TPS54623 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C1 and C2) and bootstrap capacitor (C3) are all located as close to the IC as possible. Additionally, the voltage set-point resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the J2 output connector. For the TPS54623, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage setpoint divider, frequency set resistor, slow-start capacitor, and compensation components are terminated to ground using a wide ground trace separate from the power ground pour.

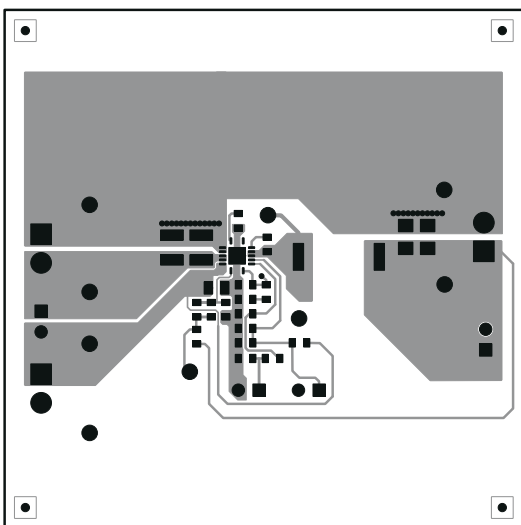


Figure 3-1. TPS54623EVM-012 Top-Side Layout

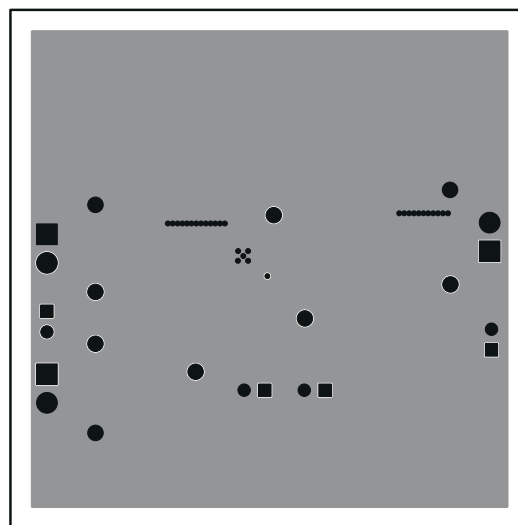


Figure 3-2. TPS54623EVM-012 Layout 2

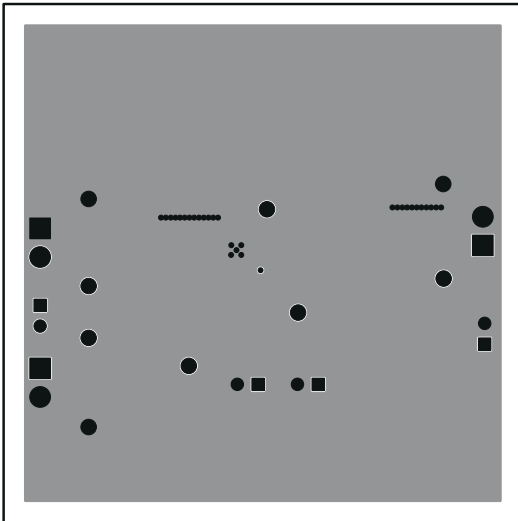


Figure 3-3. TPS54623EVM-012 Layout 3

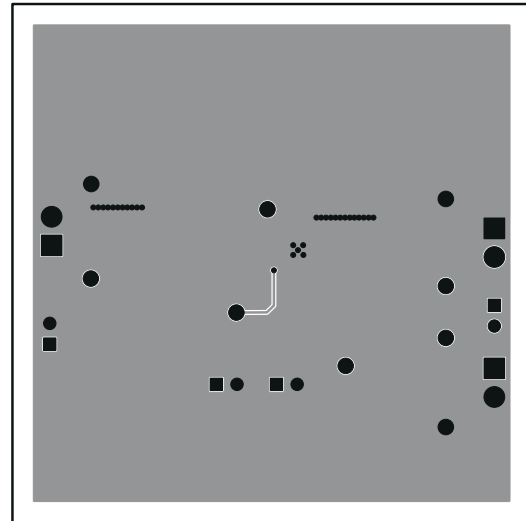


Figure 3-4. TPS54623EVM-012 Bottom-Side Layout

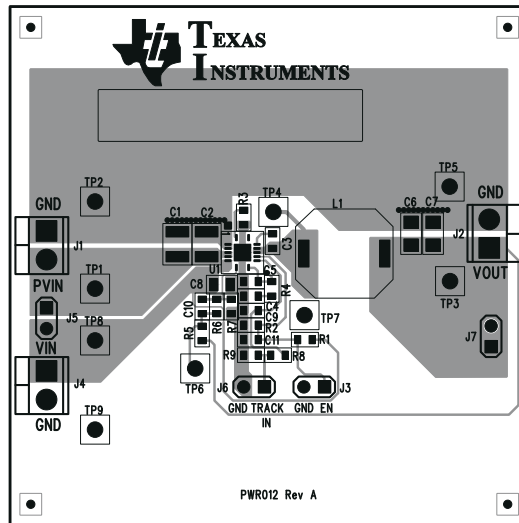


Figure 3-5. TPS54623EVM-012 Top-Side Assembly

4 Schematic and Bill of Materials

This section presents the TPS54623EVM-012 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54623EVM-012.

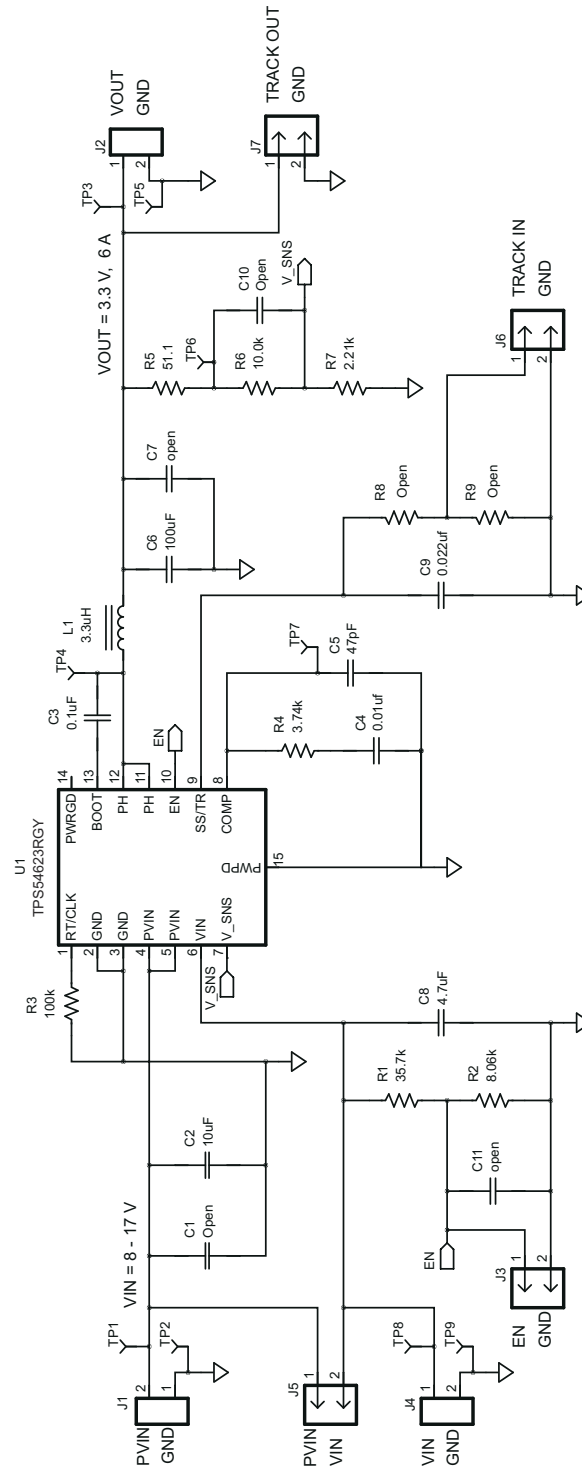


Figure 4-1. TPS54623EVM-012 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54623EVM-012.

Table 4-1. TPS54623EVM-012 Bill of Materials

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
0	C1	Open	Capacitor, Ceramic	1210	Std	Std
1	C2	10 μ F	Capacitor, Ceramic, 25 V, X5R, 20%	1210	Std	Std
1	C3	0.1 μ F	Capacitor, Ceramic, 25 V, X7R, 10%	0603	Std	Std
1	C4	0.01 μ F	Capacitor, Ceramic, 25 V, X7R, 10%	0603	Std	Std
1	C5	47 pF	Capacitor, Ceramic, 50 V, COG, 10%	0603	Std	Std
1	C6	100 μ F	Capacitor, Ceramic, 6.3 V, X5R, 20%	1206	Std	Std
0	C7	Open	Capacitor, Ceramic	1206	Std	Std
1	C8	4.7 μ F	Capacitor, Ceramic, 25 V, X5R, 10%	0805	Std	Std
1	C9	0.022 μ F	Capacitor, Ceramic, 25 V, X5R, 10%	0603	Std	Std
0	C10, C11	Open	Capacitor, Ceramic	0603	Std	Std
3	J1, J2, J4	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5 mm	0.27 x 0.25 inch	ED555/2DS	OST
4	J3, J5, J6, J7	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	3.3 μ H	Inductor, SMT, 7.2A, 10.4milli Ω	0.402 sq inch	MSS1048-332 NL_	Coilcraft
1	R1	35.7 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	8.06 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	100 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	3.74 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	51.1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	2.21 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R8, R9	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
6	TP1, TP3, TP4, TP6, TP7, TP8	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
3	TP2, TP5, TP9	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54623RHL	IC, 1.6V-17V Synchronous Buck PWM Converter with Integrated MOSFET	3.5mm x 3.3mm QFN14	TPS54623RG HL	TI
2	—		Shunt, 100-mil, Black	0.100	929950-00	3M
1	—		Label (see note 5)	1.25 x 0.25 inch	THT-13-457-10	Brady
1	—		PCB, 2.5" x 2.5" x 0.062"		PWR012	Any

Notes

- These assemblies are ESD sensitive, ESD precautions shall be observed.
- These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- These assemblies must comply with workmanship standards IPC-A-610 Class 2.
- Ref designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.
- Install label in silkscreened box after final wash. Text shall be 8 pt font

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2011) to Revision A (August 2021)**Page**

- Updated user's guide title..... 2
 - Updated the numbering format for tables, figures, and cross-references throughout the document.2
 - Edited user's guide for clarity.....2
-

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