TPS7A4001EVM-709

This User's Guide describes operational use of the TPS7A4001EVM-709 Evaluation Module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A4001, low dropout linear regulator (LDO). Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

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1 Introduction

The Texas Instruments TPS7A4001EVM-709 EVM helps design engineers to evaluate the operation and performance of the TPS7A4001 linear regulator for possible use in their own circuit application. This particular EVM configuration contains a single linear regulator with internal thermal and current limit shutdowns, and enable (disable) circuitry in a 3mm x 5mm, MSOP-8, thermally enhanced PowerPad™ package. The regulator, including external components, is capable of delivering up to 50mA to the load, depending on the input-output power dissapation, at an operating input voltage of up to 100V. The EVM output voltage is adjustable by an external resistor divider from 1.2V to 35V, but this is limited by the working voltage of the output capacitor. The LDO supports output voltages to 90V. The resistor divider is preset to provide VOUT equal to 5V.

PowerPad is a trademark of Texas Instruments.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup and use the TPS7A4001EVM.

2.1 Input/Output Connector and Jumper Descriptions

- **J1-EN**: Output enable. To enable the output, connect a jumper to short ON (pin 1) to EN (center pin 2). To disable the output, connect a jumper to short EN (pin 2) to OFF (pin 3).
- **J2 – VIN**: Input power supply voltage connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added between J2 and J4 if the supply leads are greater than six inches. For example, an additional 47µF electrolytic capacitor connected from J2 to ground can improve the transient response of the TPS7A4001 while eliminating unwanted ringing on the input due to long wire connections
- **J4 – GND**: Ground-return connector for the input power supply
- **J3 – VOUT**: Regulated output voltage connector.
- **J5 – GND**: Output ground-return connector.

2.2 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit IC especially.

2.3 Equipment Interconnect

- Turn off the input power supply after verifying that its output voltage is set to the desired supply voltage (less than 100V) and the current limit is set to approximately 100mA. Connect the positive voltage lead from input power supply to VIN, at the J2 connector of the EVM. Connect the ground lead from the input power supply to GND at the J4 connector of the EVM.
- Connect a 0-50mA load (ILoad) between VOUT, at the J3 connector, and the GND, at the J4 connector.
- Disable the output by connecting a jumper at J1 to short the EN (pin 2) to the OFF (pin 3).

3 Operation

- Turn on the input power supply. Verify that the output voltage is near 0.V.
- Enable the output by reconnecting the jumper on J1 to short the EN (pin 2) to the ON (pin 1).
- • Vary the load current and VIN voltage as necessary for test purposes. Note that at room temperature (25°C) the power dissipation (P_{disp}) across the TPS7A4001.

$$P_{disp} = (VIN – VOUT) \times I_{Load} \quad (1)$$

4 Test Results

This section provides typical performance waveforms for the TPS7A4001EVM-709 characteristic of this EVM design.

4.1 Turnon Characteristics

Figure 1 shows the turn-on characteristic where VIN is pre-set to 9V, the output load is set to 50mA, and the regulator is enabled by a 4.5V step voltage (C1, gold) applied to EN (J1, pin 2). The VOUT softstart (C4, green) shows a rise time indicative of the R1 and C2 values selected.

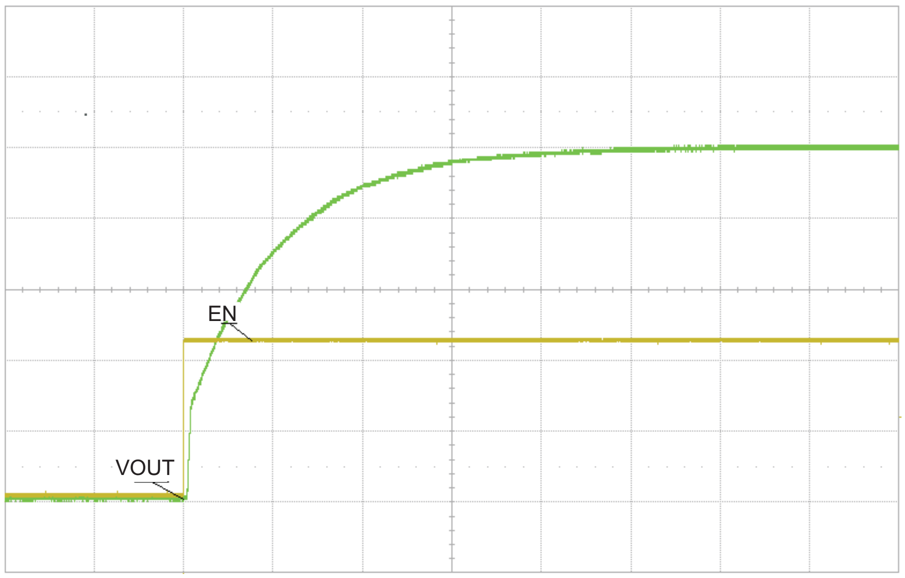

Figure 1. Turnon Sequence: C1 EN - Turnon to 4.5V, C4 VOUT – 5V Turnon Ramp Characteristic

4.2 Output Load Transition

Figure 2 shows the VOUT transient response (C2, red) for a full load step transition from 0mA to 50mA (C1, gold).

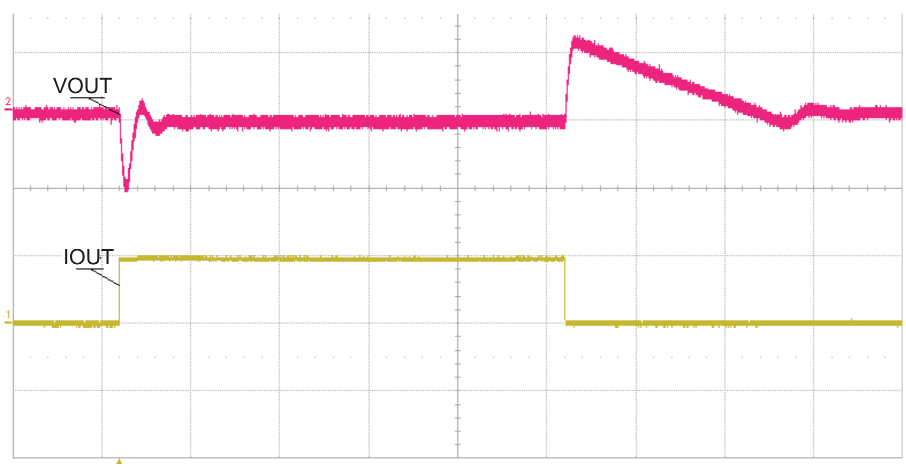

Figure 2. Step Load and Output Voltage Transient Response: C1 – Full Load Current Step, C2 VOUT – Output Voltage Transient Response

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_J = T_A + P_d \times \theta_{JA} \quad (2)$$

where:

T_J is the junction temperature

T_A is the ambient temperature

P_D is the power dissipation in the device (Watts)

θ_{JA} is the thermal resistance from junction to ambient.

All temperatures are in degrees Celcius. The maximum silicon junction temperature, T_J, must not be allowed to exceed 125°C. The layout design must use copper trace and plane areas with care, as thermal sinks. Do not to allow T_J to exceed the absolute maximum rating under all temperature conditions and voltage conditions across the part.

The layout should consider carefully the thermal design of the PCB for optimal performance over temperature. For this EVM, Figure 5 shows that the DQN package footprint employes a thermal pad for further cooling the part. The thermal pad contains a single 6.mil thermal via connection to the bottom side copper ground plane as well as a direct connection to the top side surface copper over the ground pad/pin for IC. The PCB is a two layer board with 2.oz. copper on top and bottom layers. The DQN package drawing can be found at the Texas Instruments web site in the product folder for the TPS707 LDO.

Table 1 repeats information from the Dissipation Ratings Table of the TPS7A4001 data sheet for comparison with the thermal resistance, θ_{JA}, calculated for this EVM layout to show the variation in thermal resistances for given copper areas. The High-K value is determined using a standard JEDEC high-k (2s2p) board having dimensions of 3-inch x 3-inch with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

Table 1. Thermal Resistance, θ_{JA} , and Maximum Power Dissipation

Board	Package	θ_{JA}	Max Dissipation without Derating (T_A = 25°C)	Max Dissipation without Derating (T_A = 70°C)
High-K	DGN	55.1°C/W	1.83W	1.08W
TPS7A4001EVM-709	DGN	49.0°C/W	2.04W	1.12W

The thermal resistance for the TPS7A4001EVM-709, θ_{JA}, is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the volume of copper volume connected to the package.

6 Board Layout

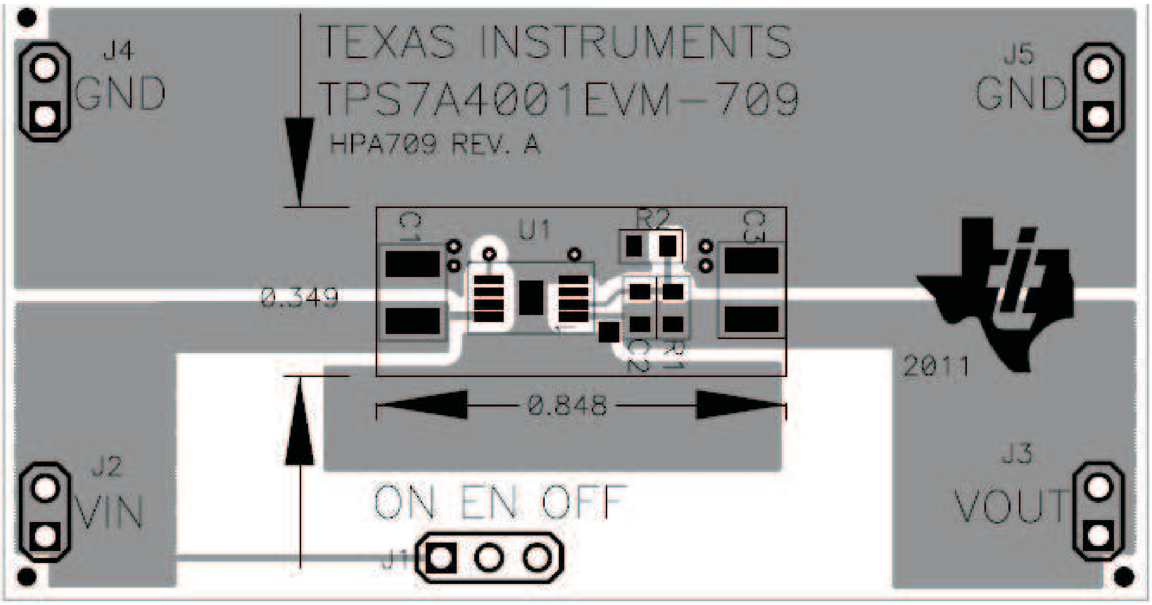

Figure 3. Assembly Layer

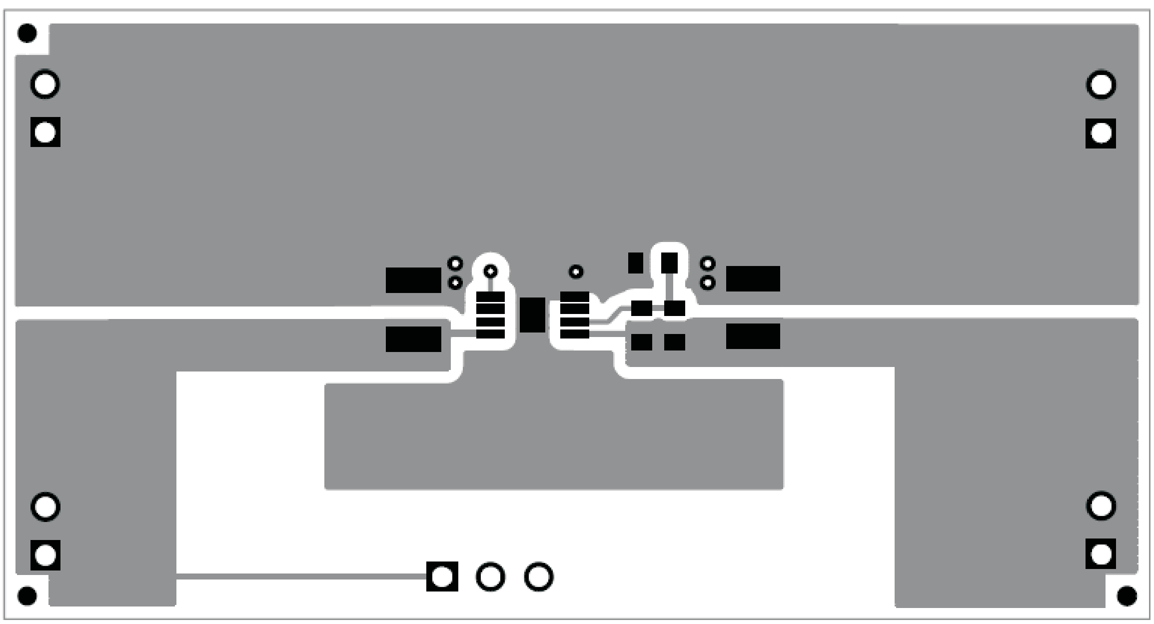

Figure 4. Top Layer Routing

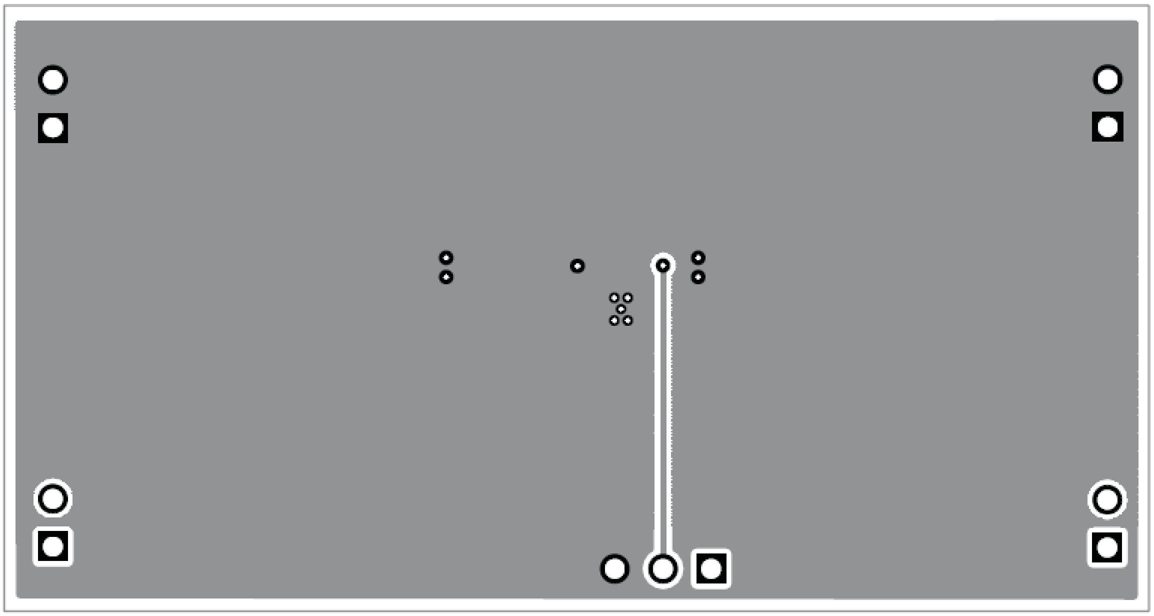

Figure 5. Bottom Layer Routing

7 Schematic and Bill of Materials

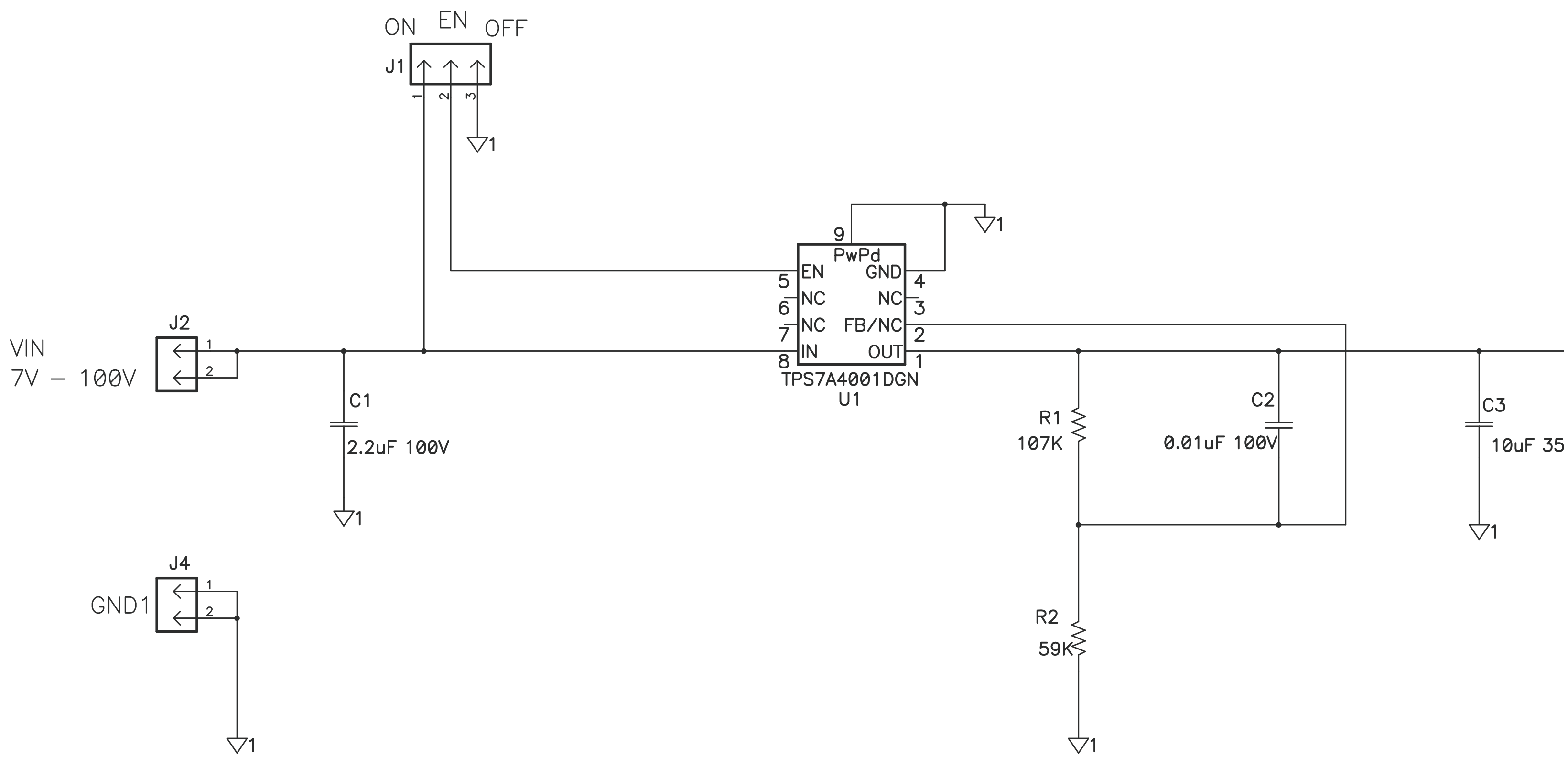

Figure 6. Schematic

Table 2. TPS7A4100EVM-709 Bill of Materials

COUNT	RefDes	Value	Description	Size	Part Number	MFR
1	C1	2.2 uF	Capacitor, Ceramic, 100V, X7R, 10%	1210	STD	STD
1	C2	0.01uF	Capacitor, Ceramic, Low Inductance, 100V, X7R, 20%	0603	STD	STD
1	C3	10.0 uF	Capacitor, Ceramic, 35V, X7R, 10%	1210	STD	STD
1	J1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
4	J2, J3, J4, J5	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	R1	107K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R2	59K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	U1	TPS7A4001DGN	IC, 120 V Input Voltage, 50 mA	DGN	TPS7A4001DGN	TI
1	--	--	PCB, 1.260In x 2.370 In x 0.062 In	--	HPA709	Any
1	--	--	Shunt, 100-mil, Black	0.100 inch	929950-00	3M
Notes:	1. These assemblies are ESD sensitive, ESD precautions shall be observed. 2. These assemblies must be clean and free from flux and all contaminants. 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2. 4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.					

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 7V to 100V and the output voltage range of not to exceed 90V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 160°C. The EVM is designed to operate properly with certain components above 160°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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