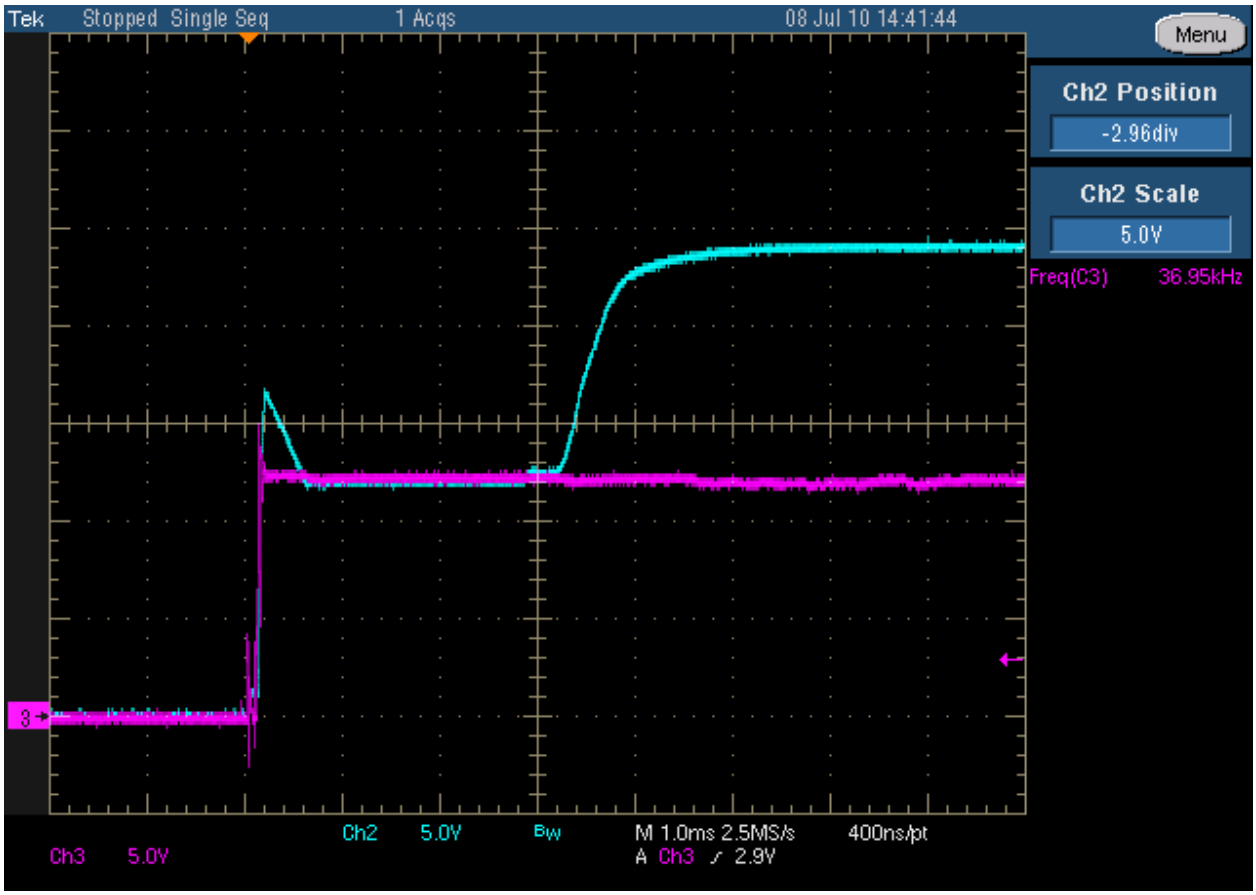
1. Startup

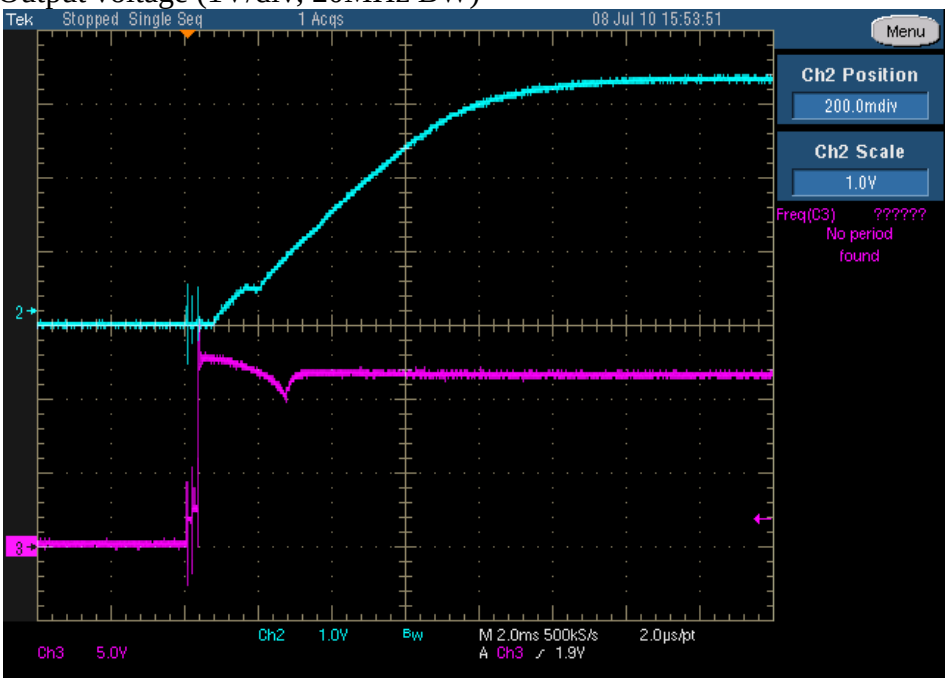
The output voltage at startup behavior was measured for each block and is shown in the images below.

"+24V_ANT" output, U4 controller (input connected to JP2):
Conditions: Input voltage: 12V, Output load: 150mA

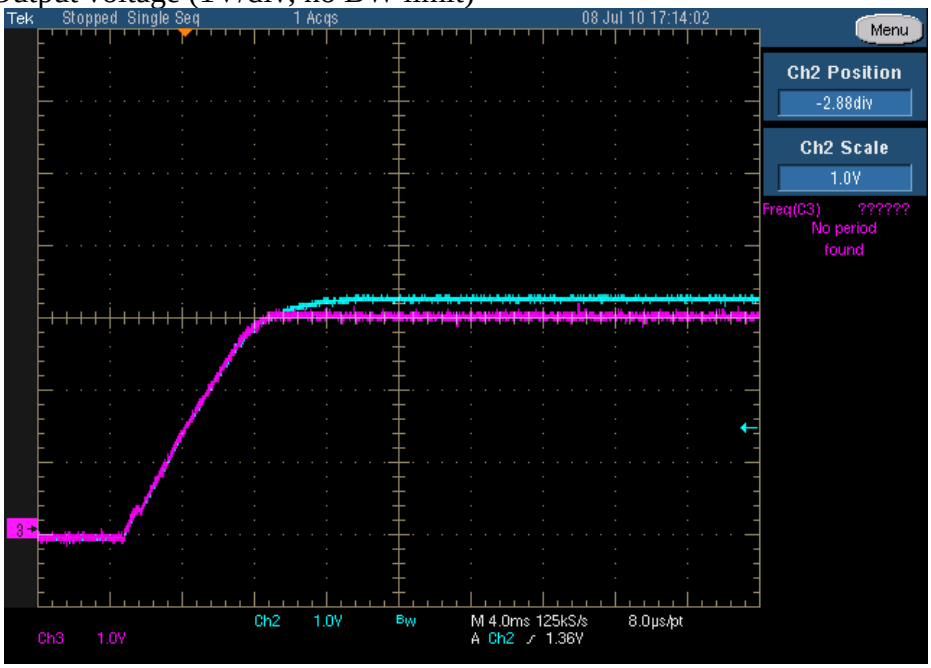
Channel 3: Input voltage (5V/div, 1ms/div, no BW limit)
Channel 2: Output voltage (5V/div, 20MHz BW)



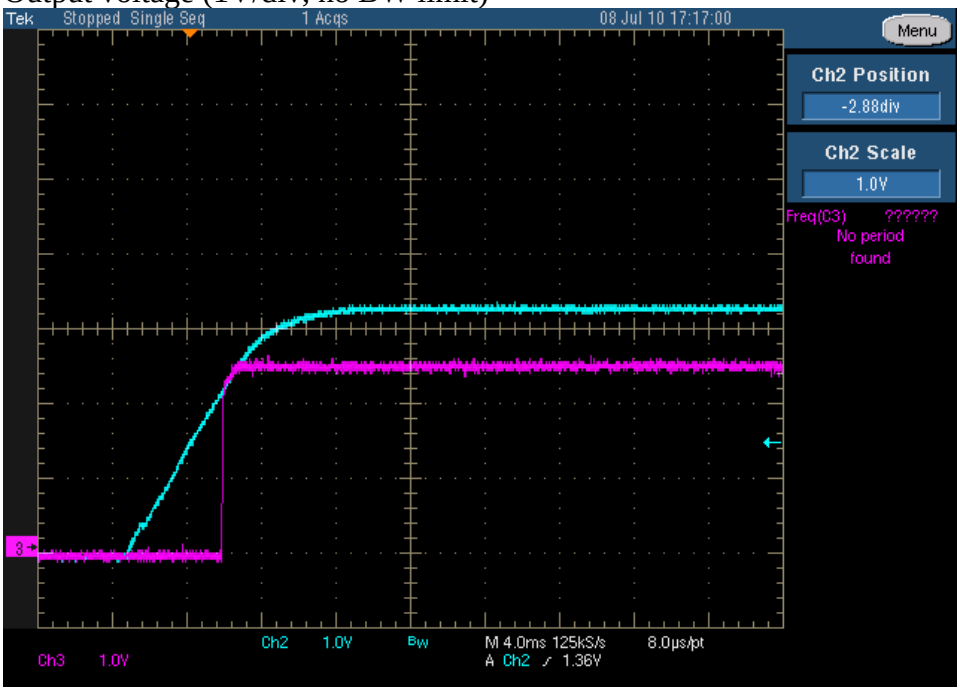
"+3V3_IO" output, U12 controller (input connected to JP3):
Conditions: Input voltage: 12V, Output load: 5A
Channel 3: Input voltage (5V/div, 2ms/div, no BW limit)
Channel 2: Output voltage (1V/div, 20MHz BW)



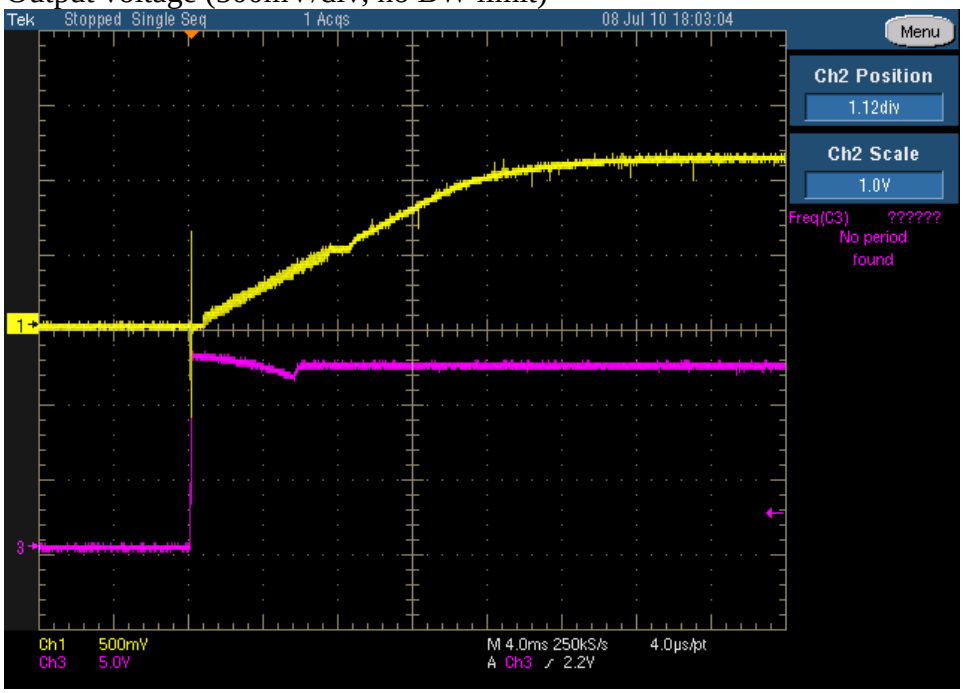
"+3V0_FPGA" output, U13 LDO:
Conditions: Input voltage: +3V3_IO, Output load: 0.5A
Channel 2: Input voltage (1V/div, 4ms/div, 20MHz BW)
Channel 3: Output voltage (1V/div, no BW limit)



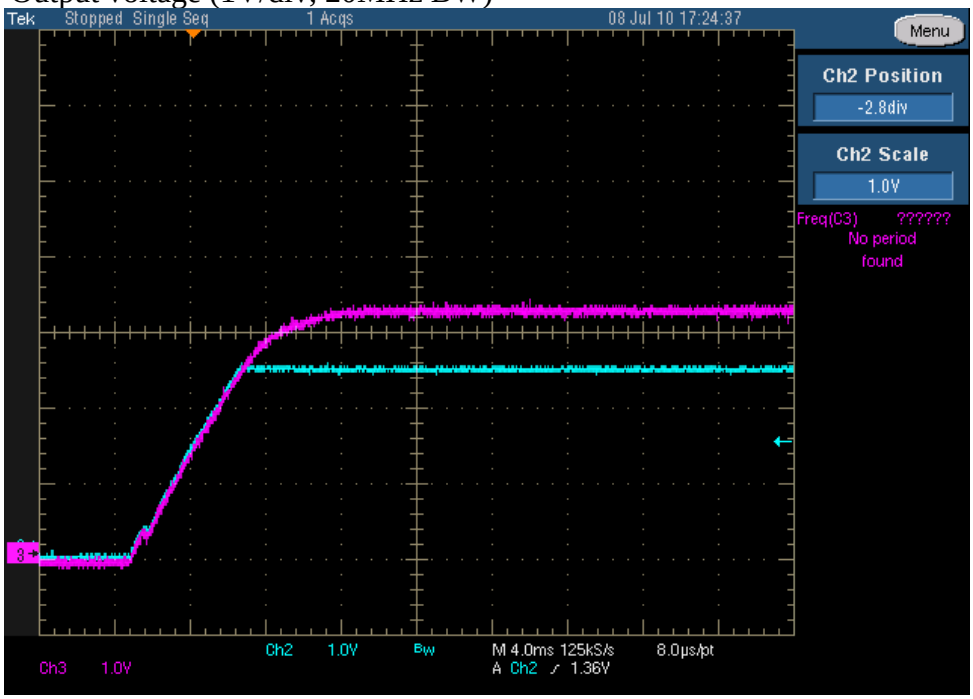
"+2V5_PLL" output, U14 LDO:
Conditions: Input voltage: +3V3_IO, Output load: 0.1A
Channel 2: Input voltage (1V/div, 4ms/div, 20MHz BW)
Channel 3: Output voltage (1V/div, no BW limit)



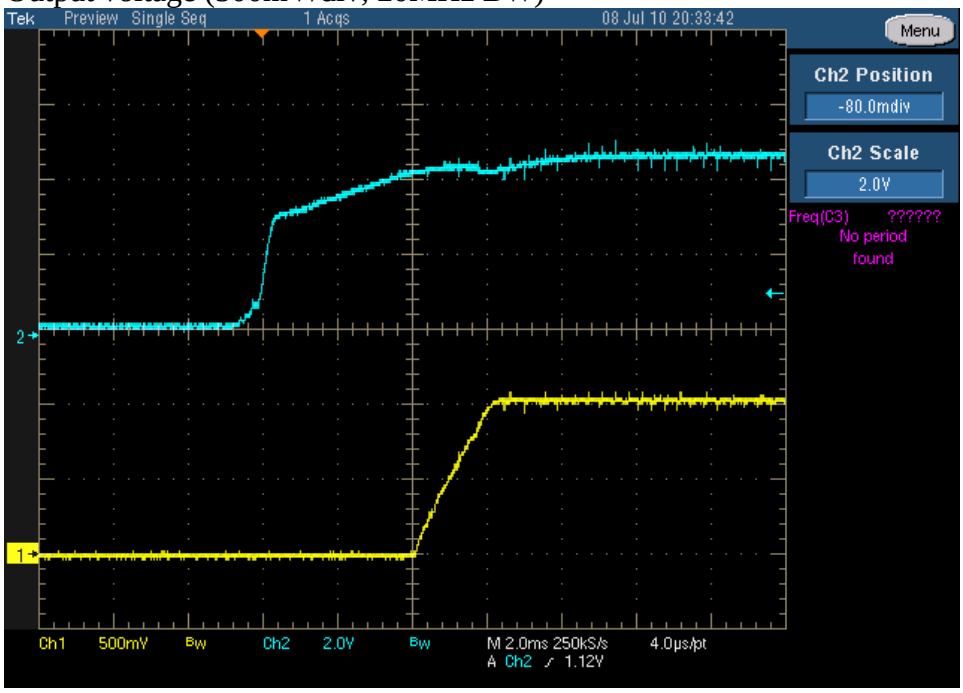
"+1V2_FPGA" output, U16 controller (input connected to JP6):
Conditions: Input voltage: 12V, Output load: 2A
Channel 3: Input voltage (5V/div, 4ms/div, no BW limit)
Channel 2: Output voltage (500mV/div, no BW limit)



“+2V5_RGMII” output, U17 LDO:
Conditions: Input voltage: +3V3_IO, Output load: 0.7A
Channel 3: Input voltage (1V/div, 4ms/div, no BW limit)
Channel 2: Output voltage (1V/div, 20MHz BW)



“+1V05_CORE” output, U19 controller (input connected to JP8):
Conditions: Input voltage: 5V, Output load: 7A
Channel 2: Input voltage (2V/div, 2ms/div, 20MHz BW)
Channel 2: Output voltage (500mV/div, 20MHz BW)

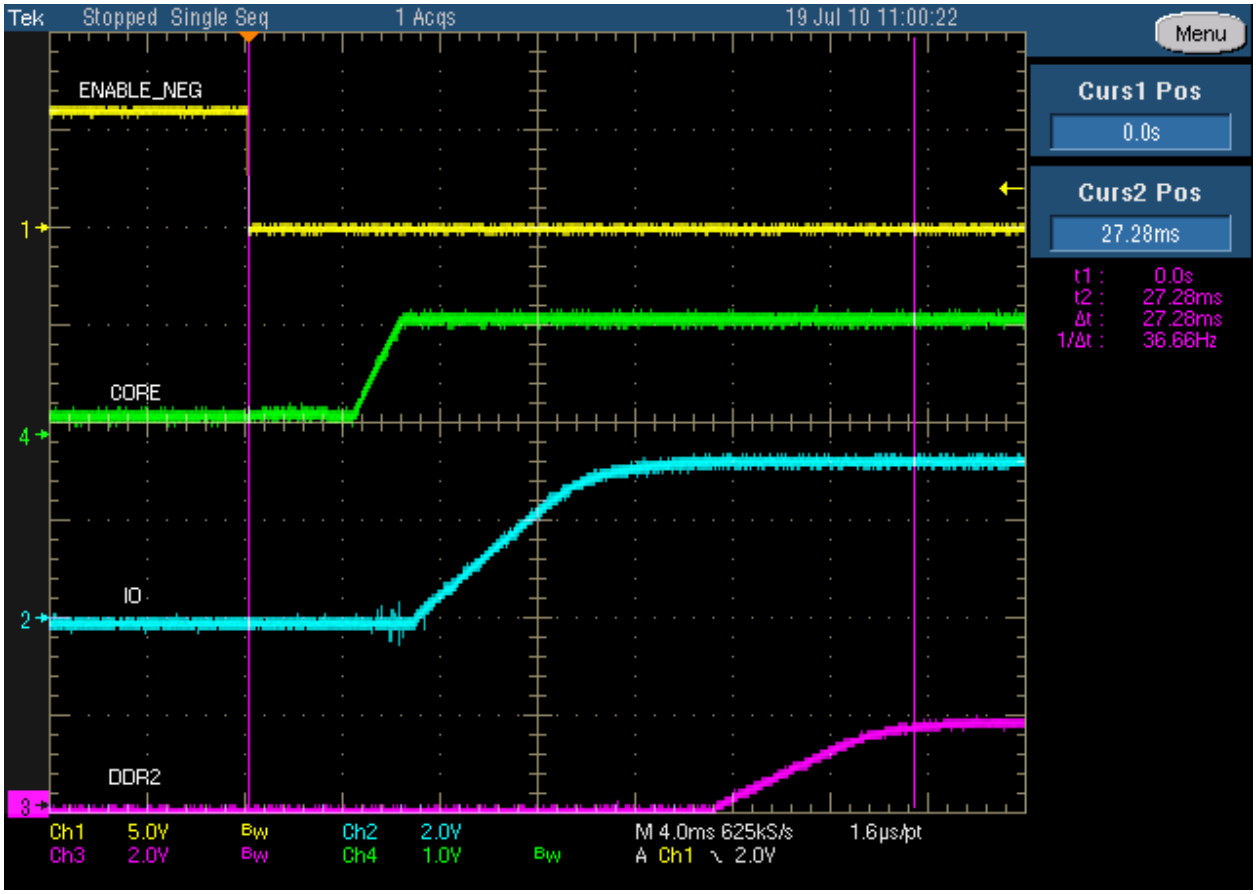


Startup behavior of the CORE, IO, DDR2 voltages after supplying the last input voltage (all the input voltages must be inside the nominal values before enabling any converter): the ENABLE_NEG line goes down, thus enabling all converters.

Conditions:

Input voltages: nominal voltages, Output loads: no load on all outputs

Channel 1: Drain Voltage of Q6 (5V/div, 4ms/div)
Channel 4: “CORE” voltage on TP38 (1V/div)
Channel 2: “IO” voltage on TP17 (1V/div)
Channel 2: “DDR2” voltage on TP47 (1V/div)

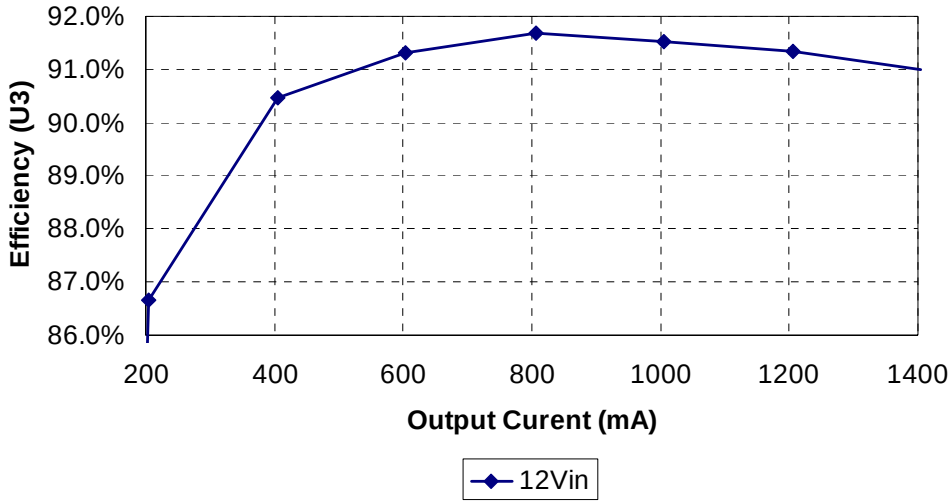


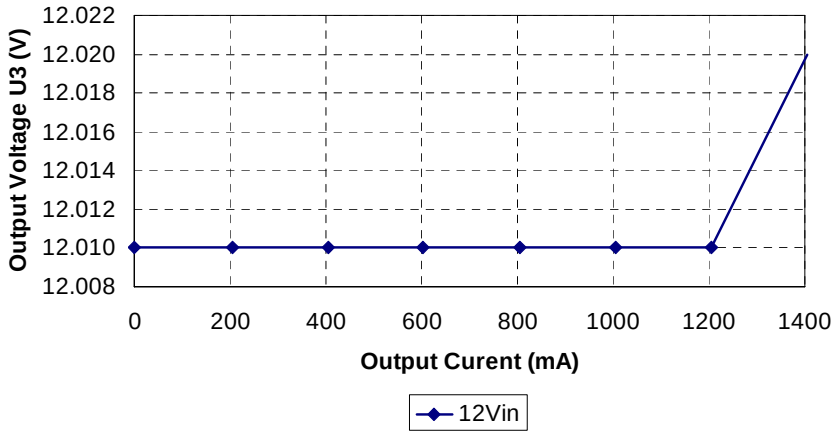
The maximum startup time is 27.28msec < 50ms specified.

2. Efficiency and Voltage Regulation

The efficiency data and voltage regulation behavior are shown in the tables and graph below. The power on each converter was applied to the correspondent input jumper.

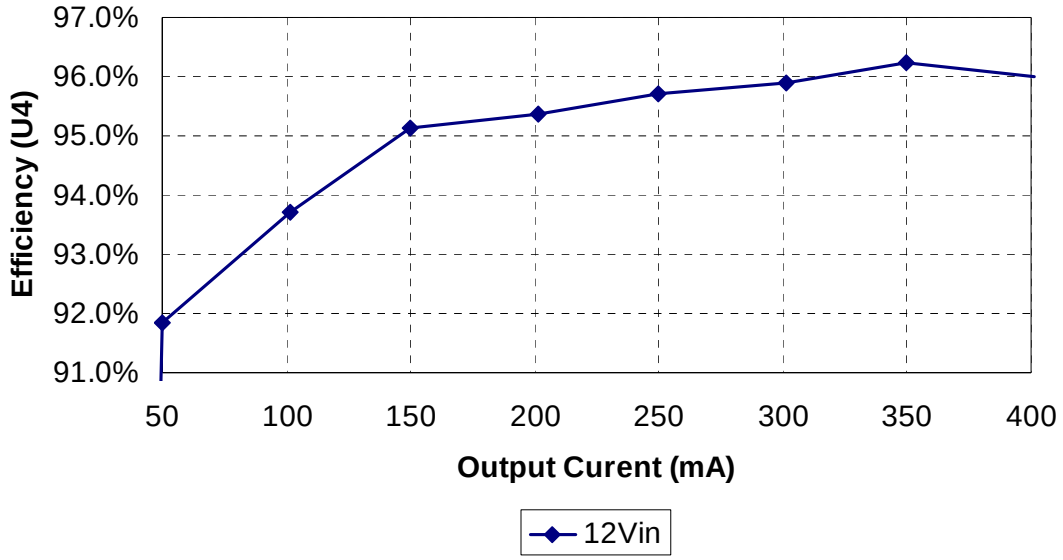
"+12V_ANT" output, U3 controller (input connected to J2):

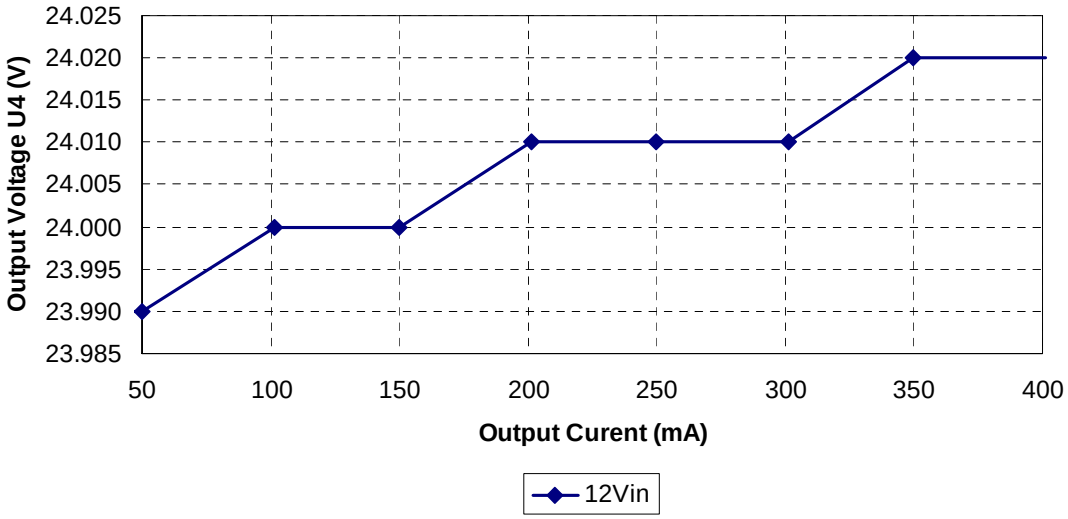




Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.0	12.01	0.00	11	12.05	0.133	0.133	0.0%
204	12.01	2.45	236	11.98	2.827	0.377	86.7%
404	12.01	4.85	447	12.00	5.364	0.512	90.5%
603	12.01	7.24	661	12.00	7.932	0.690	91.3%
806	12.01	9.68	882	11.97	10.558	0.877	91.7%
1005	12.01	12.07	1100	11.99	13.189	1.119	91.5%
1205	12.01	14.47	1316	12.04	15.845	1.373	91.3%
1404	12.02	16.88	1543	12.02	18.547	1.671	91.0%

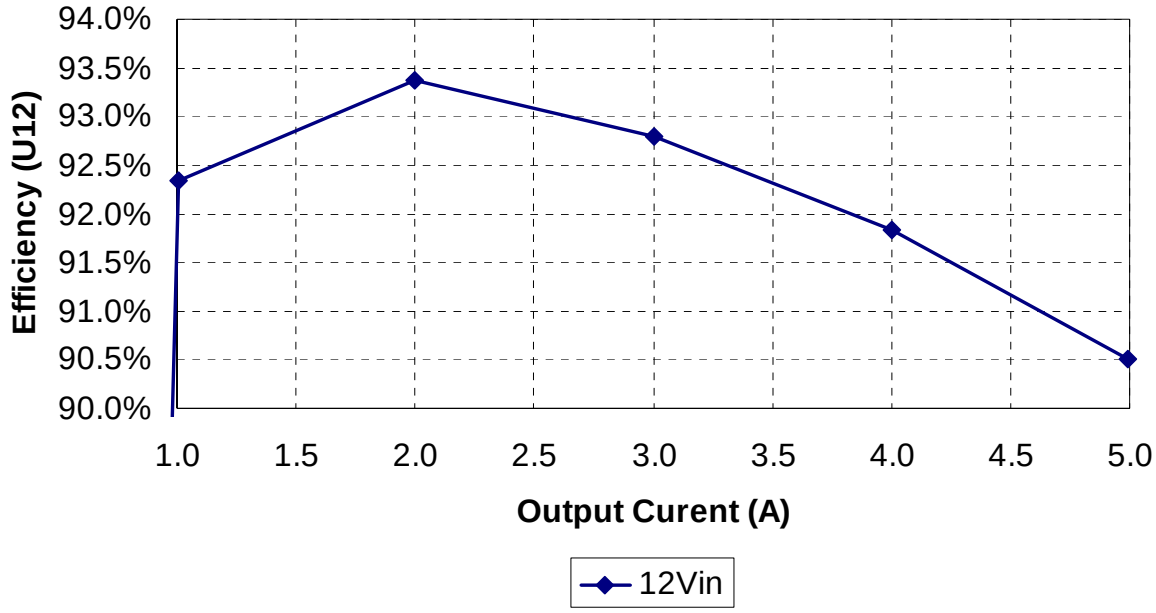
"+24V_ANT" output, U4 controller (input connected to JP2):

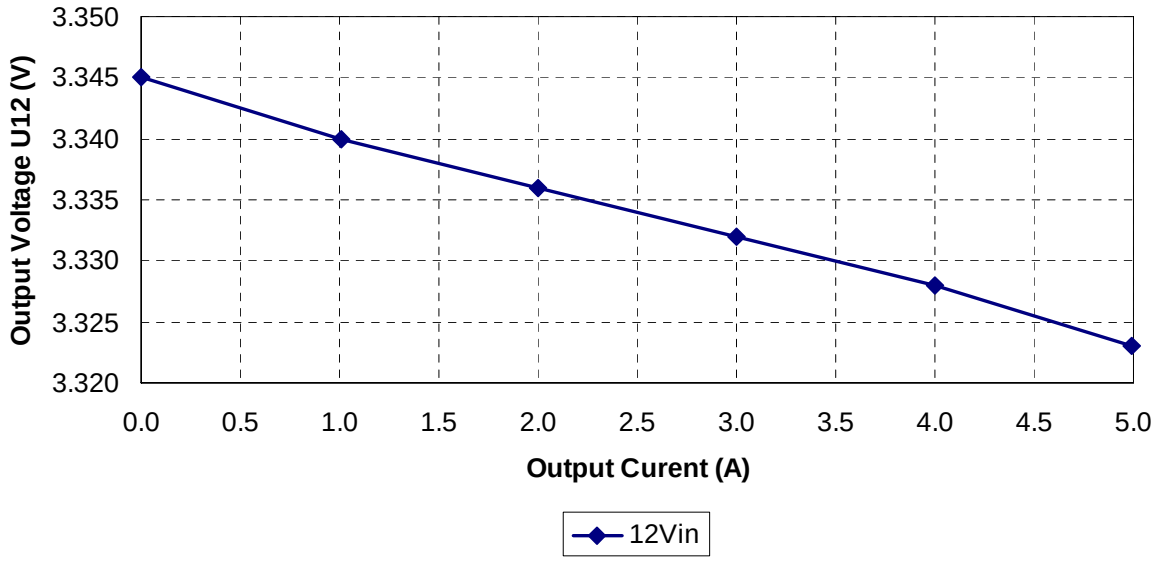




Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.0	23.99	0.00	2.44	12.02	0.029	0.029	0.0%
50.3	23.99	1.21	109.4	12.01	1.314	0.107	91.8%
101.6	24.00	2.44	215.4	12.08	2.602	0.164	93.7%
150.2	24.00	3.60	314.7	12.04	3.789	0.184	95.1%
201.5	24.01	4.84	421	12.05	5.073	0.235	95.4%
250.1	24.01	6.00	522	12.02	6.274	0.270	95.7%
301.5	24.01	7.24	629	12.00	7.548	0.309	95.9%
350.0	24.02	8.41	728	12.00	8.736	0.329	96.2%
401.0	24.02	9.63	834	12.03	10.033	0.401	96.0%

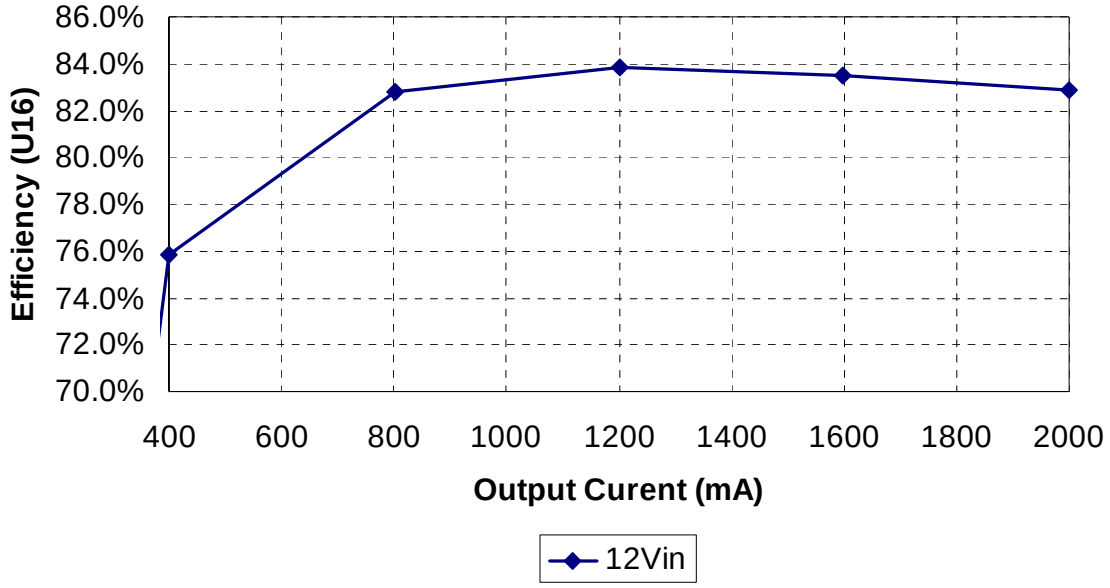
"+3V3_IO" output, U12 controller (input connected to JP3):

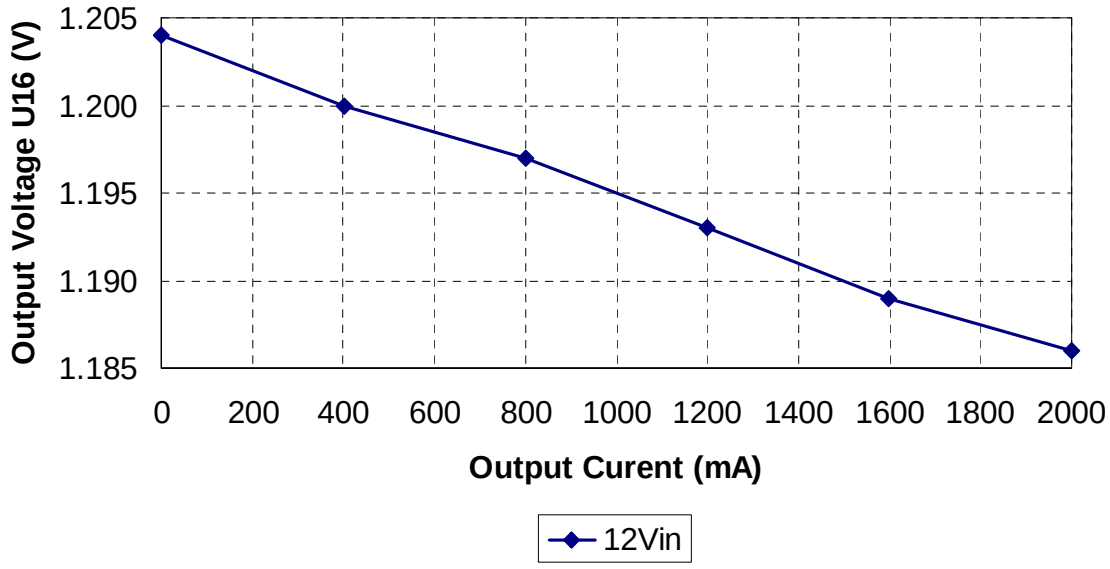




Iout (A)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.000	3.345	0.00	14	12.02	0.168	0.168	0.0%
1.006	3.340	3.36	303	12.01	3.639	0.279	92.3%
2.000	3.336	6.67	595	12.01	7.146	0.474	93.4%
3.000	3.332	10.00	897	12.01	10.773	0.777	92.8%
4.000	3.328	13.31	1207	12.01	14.496	1.184	91.8%
4.992	3.323	16.59	1526	12.01	18.327	1.739	90.5%

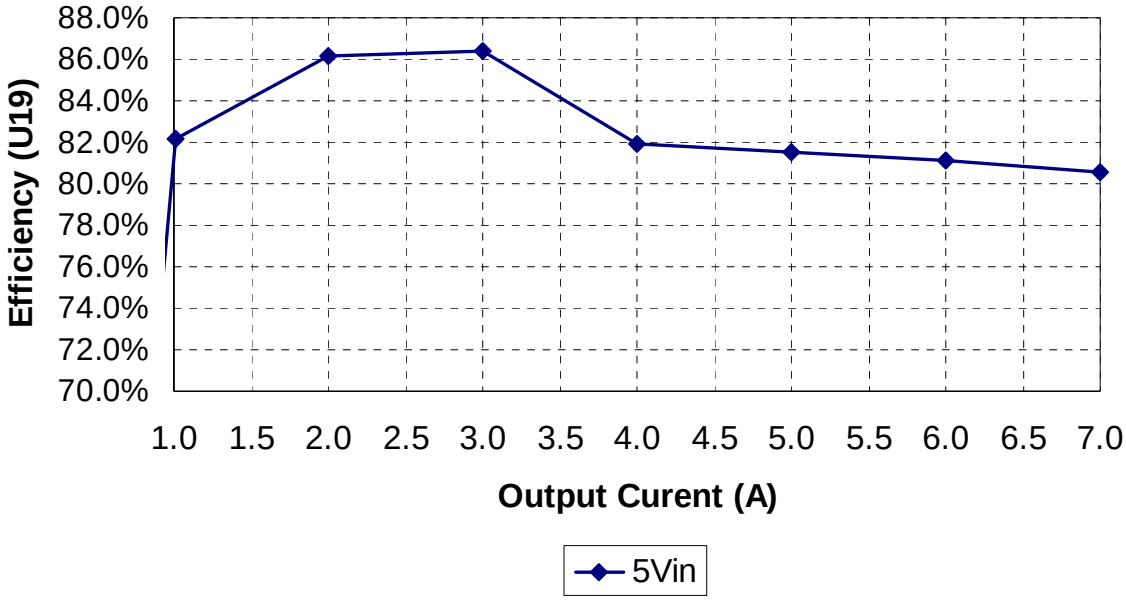
"+1V23_FPGA" output, U16 controller (input connected to JP6):

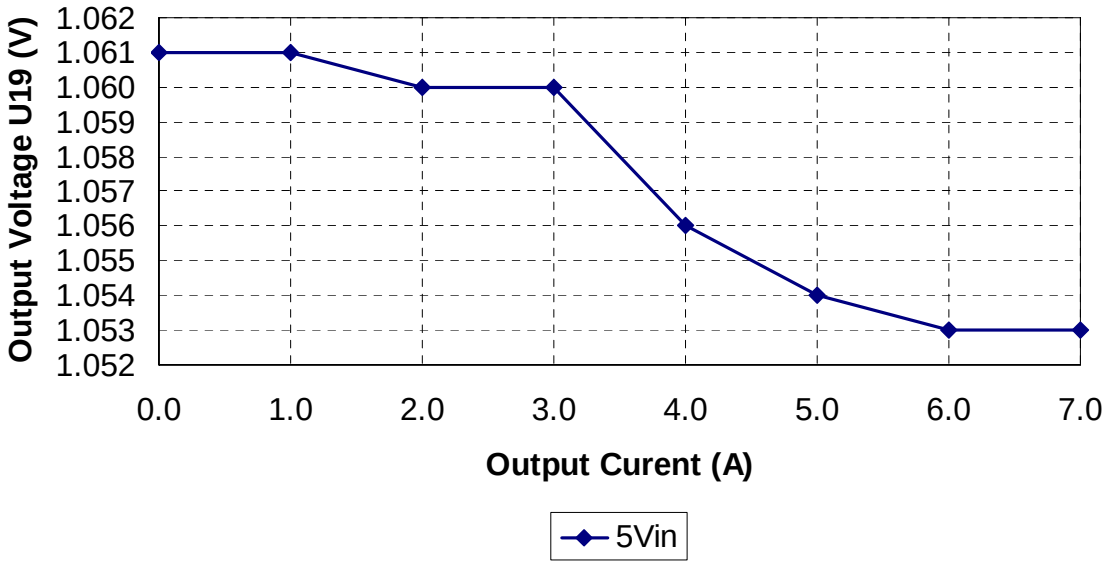




Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.0	1.204	0.00	12.8	12.02	0.154	0.154	0.0%
401.1	1.200	0.48	52.8	12.02	0.635	0.153	75.8%
801	1.197	0.96	96.3	12.02	1.158	0.199	82.8%
1200	1.193	1.43	142.3	12.00	1.708	0.276	83.8%
1597	1.189	1.90	189.0	12.03	2.274	0.375	83.5%
2000	1.186	2.37	238.3	12.01	2.862	0.490	82.9%

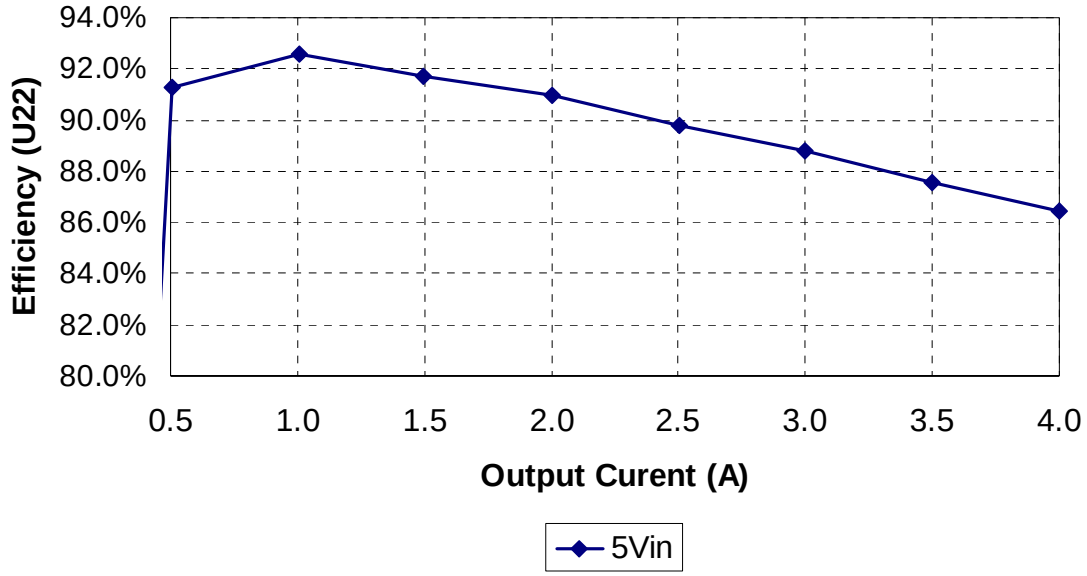
"+1V05_CORE" output, U19 controller (input connected to JP8):

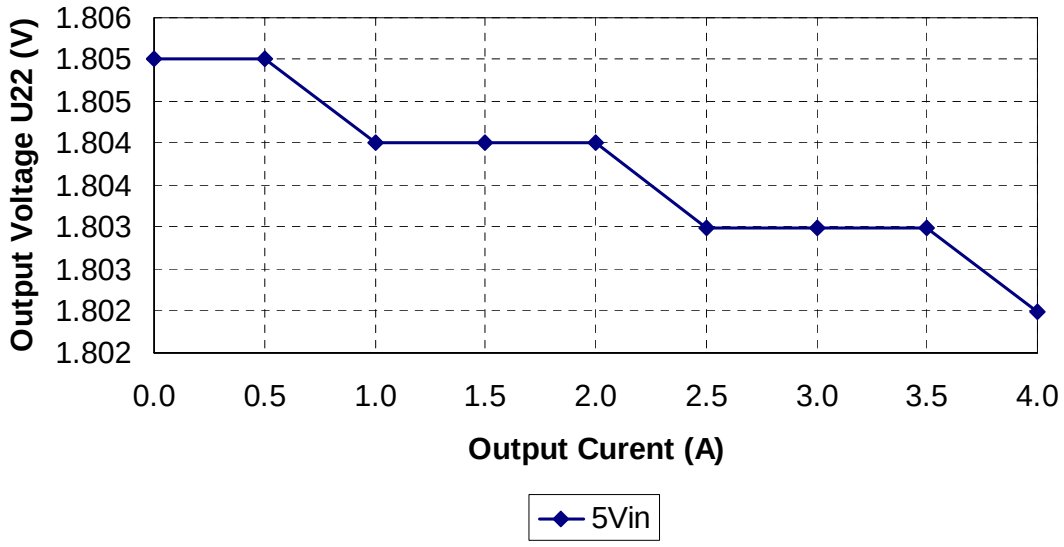




Iout (A)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.000	1.061	0.00	29	5.016	0.145	0.145	0.0%
1.006	1.061	1.07	259	5.017	1.299	0.232	82.1%
2.002	1.060	2.12	492	5.008	2.464	0.342	86.1%
3.000	1.060	3.18	736	5.001	3.681	0.501	86.4%
4.000	1.056	4.22	1027	5.019	5.155	0.931	81.9%
5.001	1.054	5.27	1285	5.031	6.465	1.194	81.5%
6.000	1.053	6.32	1549	5.030	7.791	1.473	81.1%
7.000	1.053	7.37	1828	5.007	9.153	1.782	80.5%

"+1V8_DDR2" output, U22 controller (input connected to JP9):





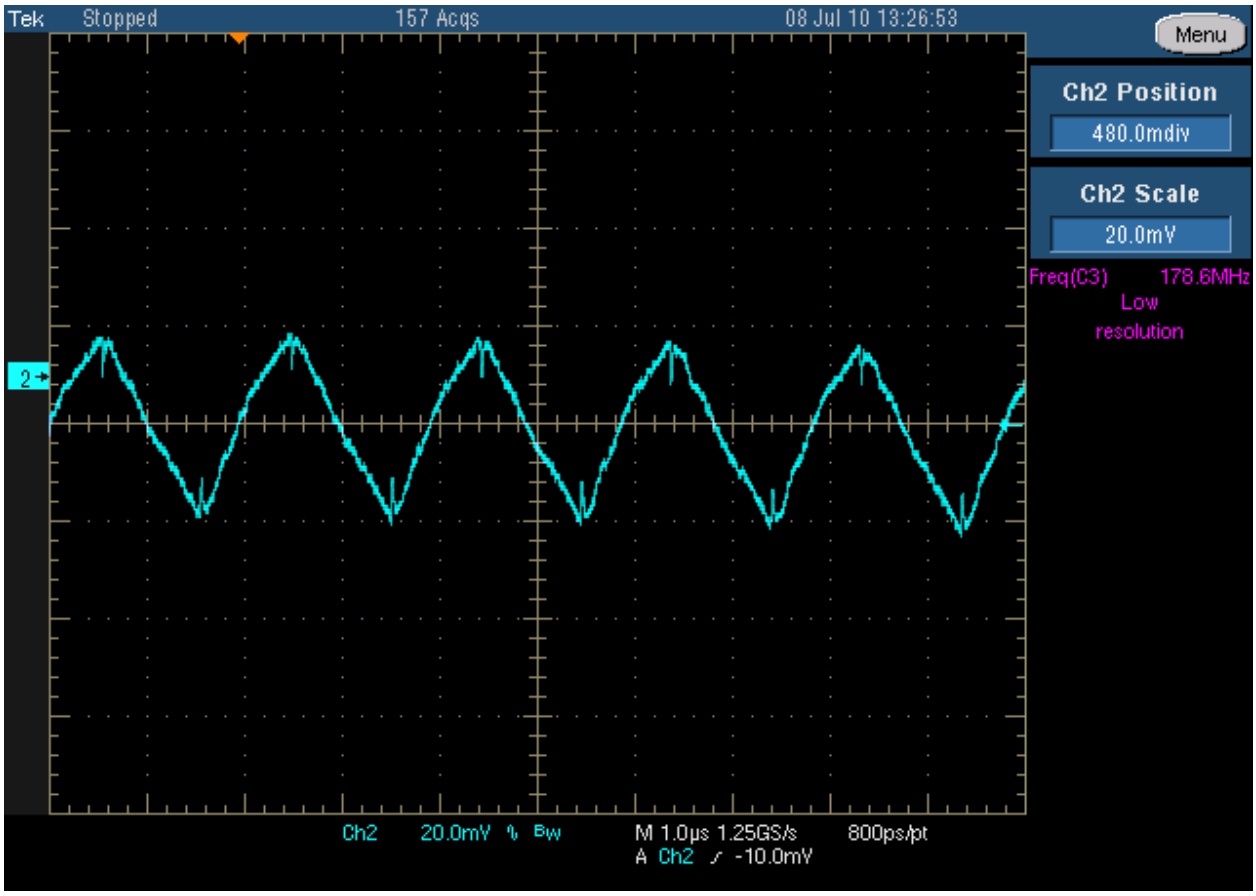
Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff
0.000	1.805	0.00	10	5.004	0.050	0.050	0.0%
0.504	1.805	0.91	199	5.008	0.997	0.087	91.2%
1.006	1.804	1.81	392	5.000	1.960	0.145	92.6%
1.498	1.804	2.70	589	5.003	2.947	0.244	91.7%
2.000	1.804	3.61	793	5.001	3.966	0.358	91.0%
2.503	1.803	4.51	1004	5.006	5.026	0.513	89.8%
3.000	1.803	5.41	1218	5.000	6.090	0.681	88.8%
3.501	1.803	6.31	1442	5.000	7.210	0.898	87.5%
4.000	1.802	7.21	1665	5.008	8.338	1.130	86.4%

3. Output Ripple Voltage

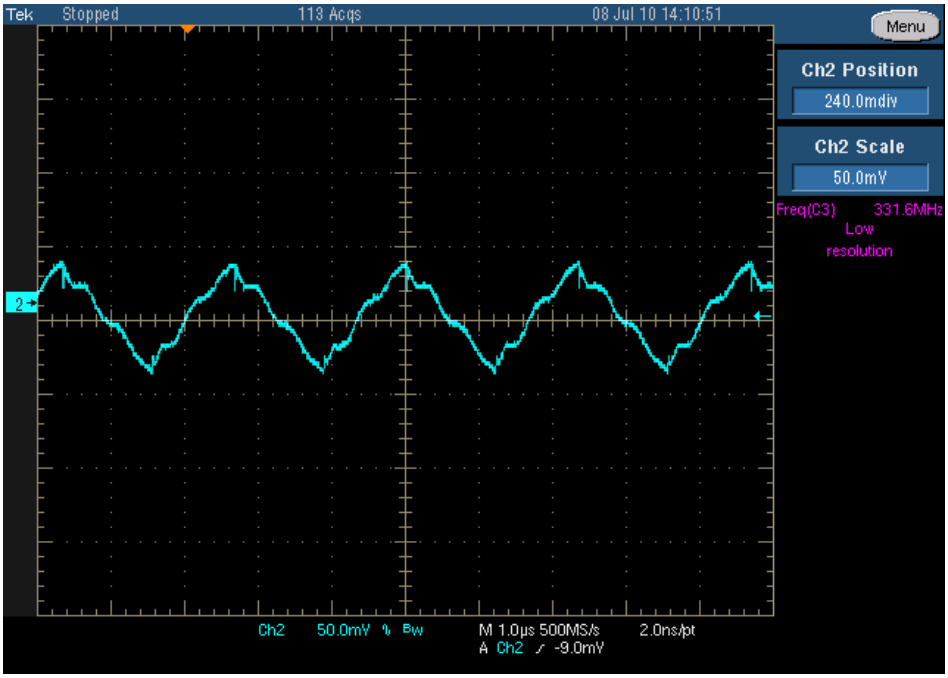
The ripple voltage waveforms measured at the terminal blocks are shown in the plots below.

“+12V_ANT” output, U3 controller (input connected to J2):
Conditions: Input voltage: 12V, Output load: 1.2A

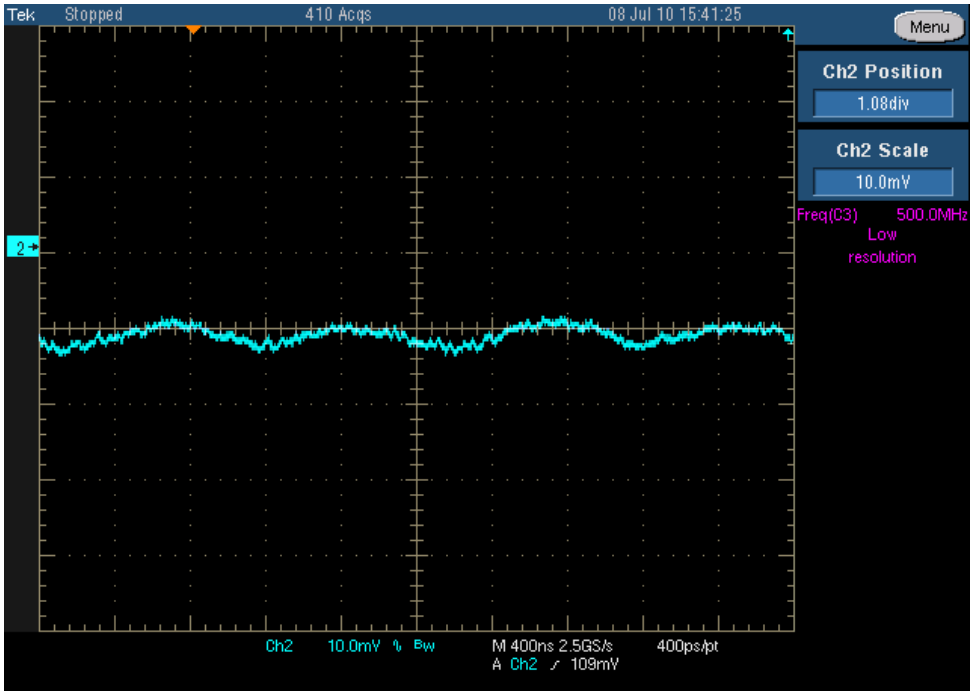
Channel 2: Output voltage (20mV/div, AC coupled, 1usec/div, 20MHz BW)



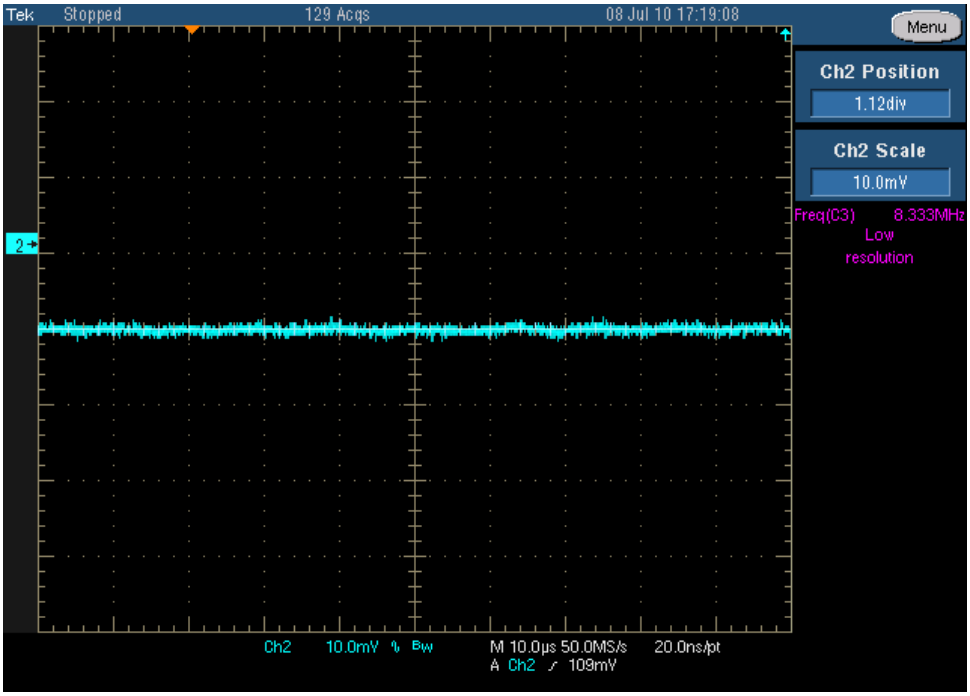
“+24V_ANT” output, U4 controller (input connected to JP2):
Conditions: Input voltage: 12V, Output load: 0.5A
Channel 2: Output voltage (50mV/div, AC coupled, 1usec/div, 20MHz BW)



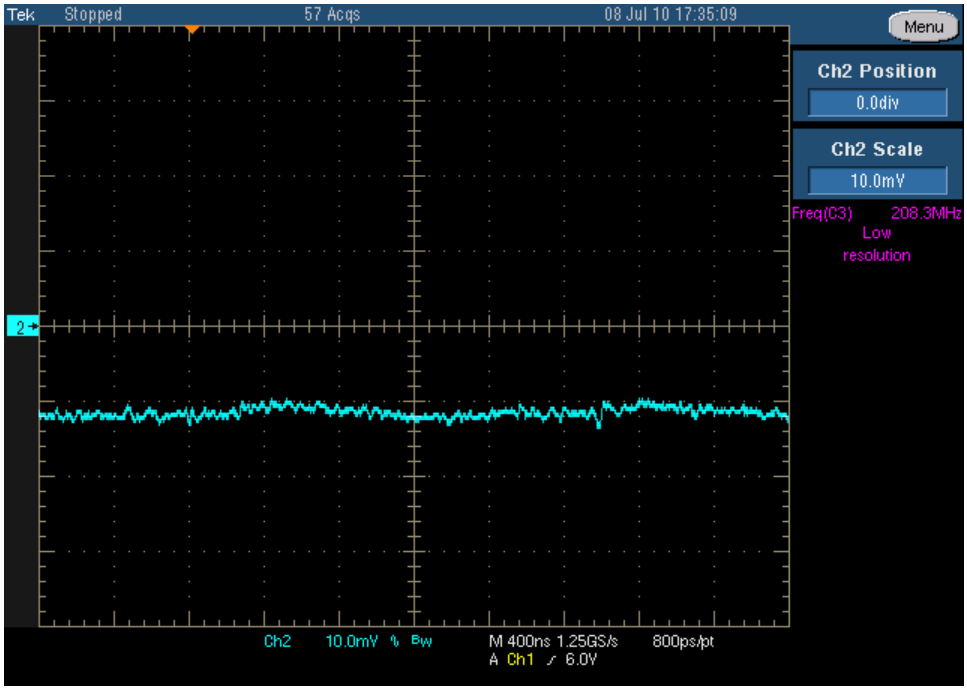
“+3V3_IO” output, U12 controller (input connected to JP3):
Conditions: Input voltage: 12V, Output load: 5A
Channel 2: Output voltage (10mV/div, AC coupled, 400nsec/div, 20MHz BW)



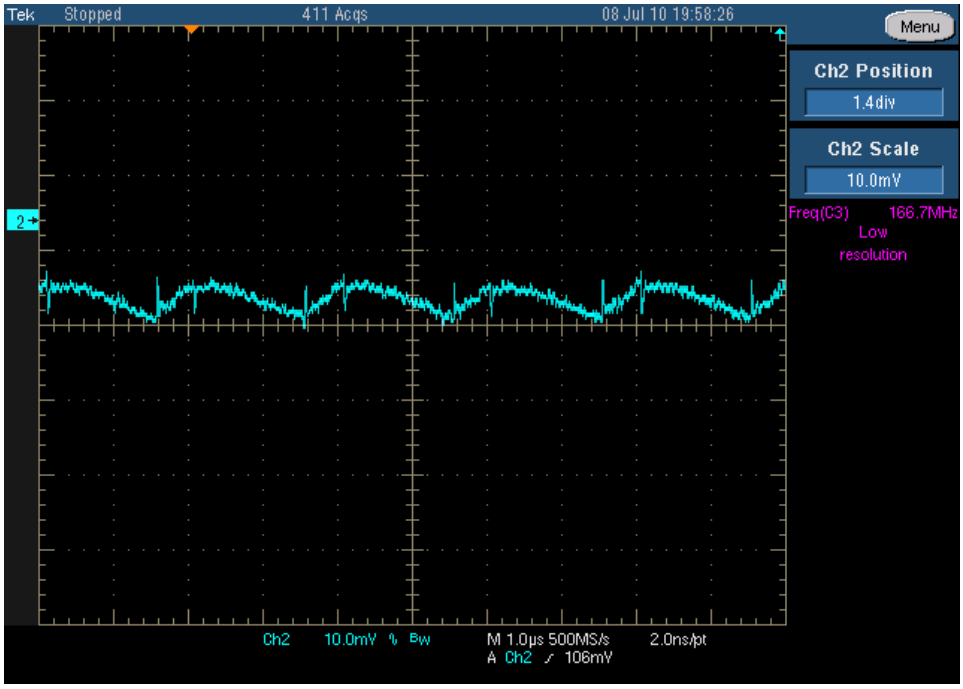
"+2V5_PLL" output, U14 controller
Conditions: Input voltage: 3.3V_IO, Output load: 0.1A
Channel 2: Output voltage (10mV/div, AC coupled, 10usec/div, 20MHz BW)



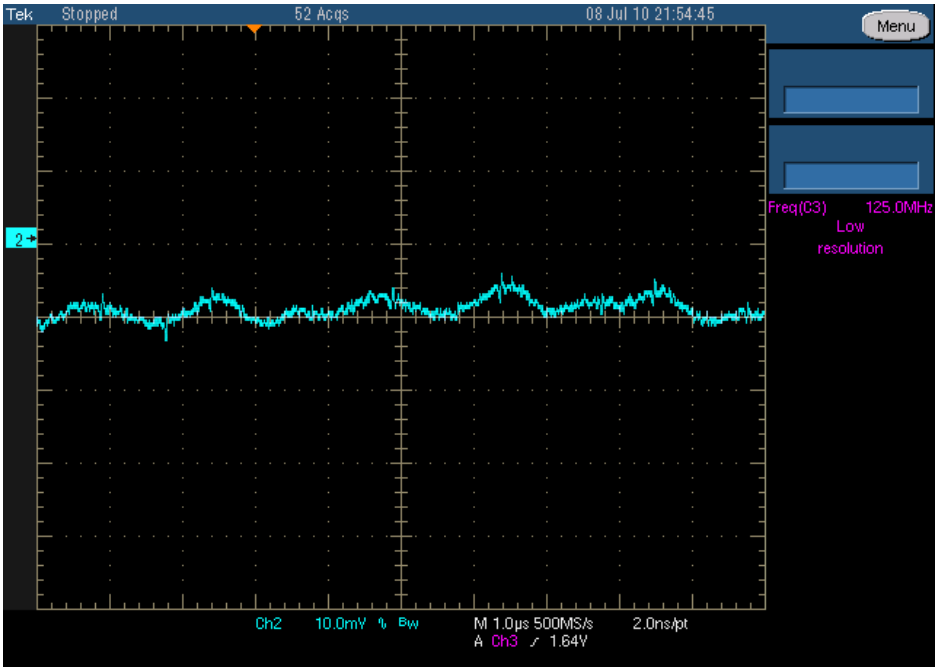
"+1V2_FPGA" output, U16 controller (input connected to JP6):
Conditions: Input voltage: 12V, Output load: 2A
Channel 2: Output voltage (10mV/div, AC coupled, 400nsec/div, 20MHz BW)



“+1V05_CORE” output, U19 controller (input connected to JP8):
Conditions: Input voltage: 5V, Output load: 7A
Channel 2: Output voltage (10mV/div, AC coupled, 1usec/div, 20MHz BW)



“+1V8_DDR2” output, U22 controller (input connected to JP9):
Conditions: Input voltage: 5V, Output load: 4A
Channel 2: Output voltage (10mV/div, AC coupled, 1usec/div, 20MHz BW)

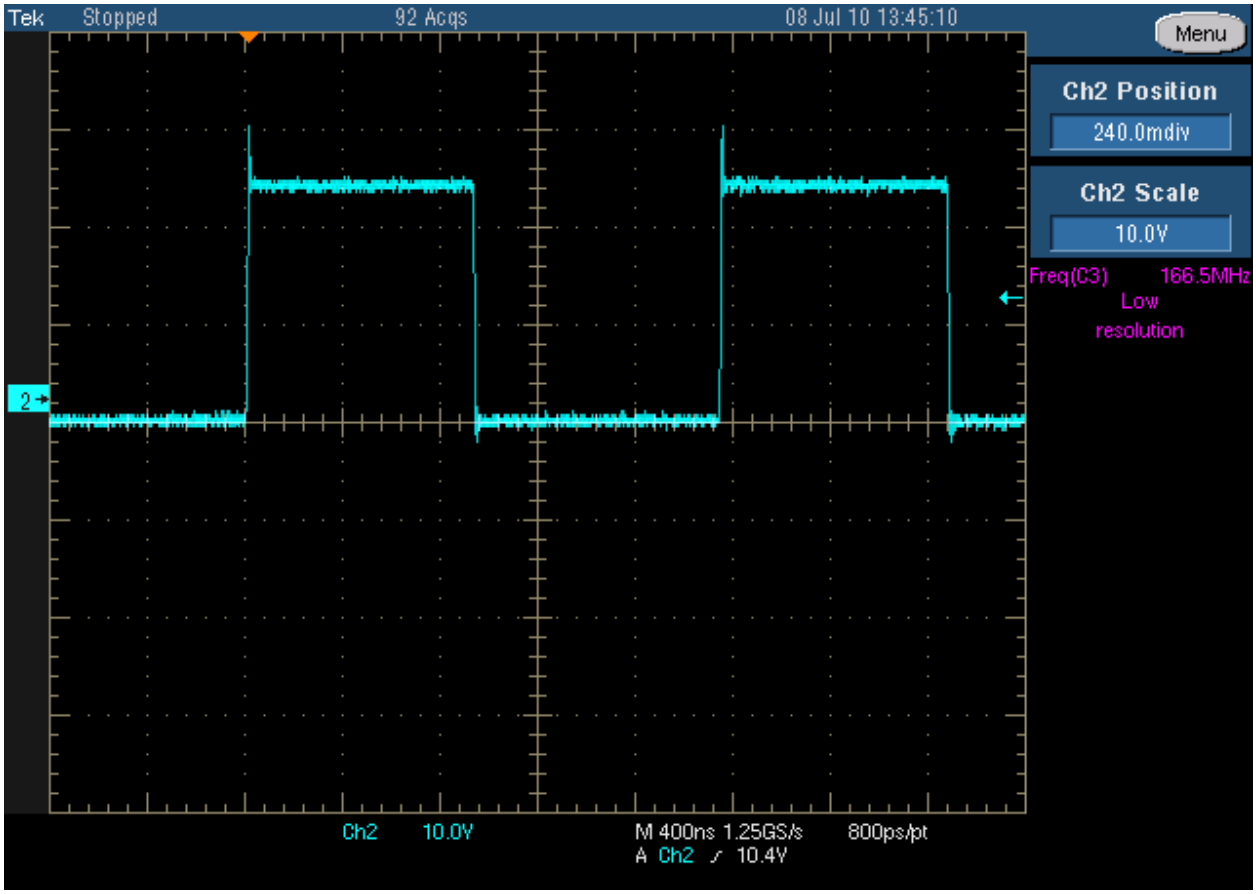


4. Switch-node

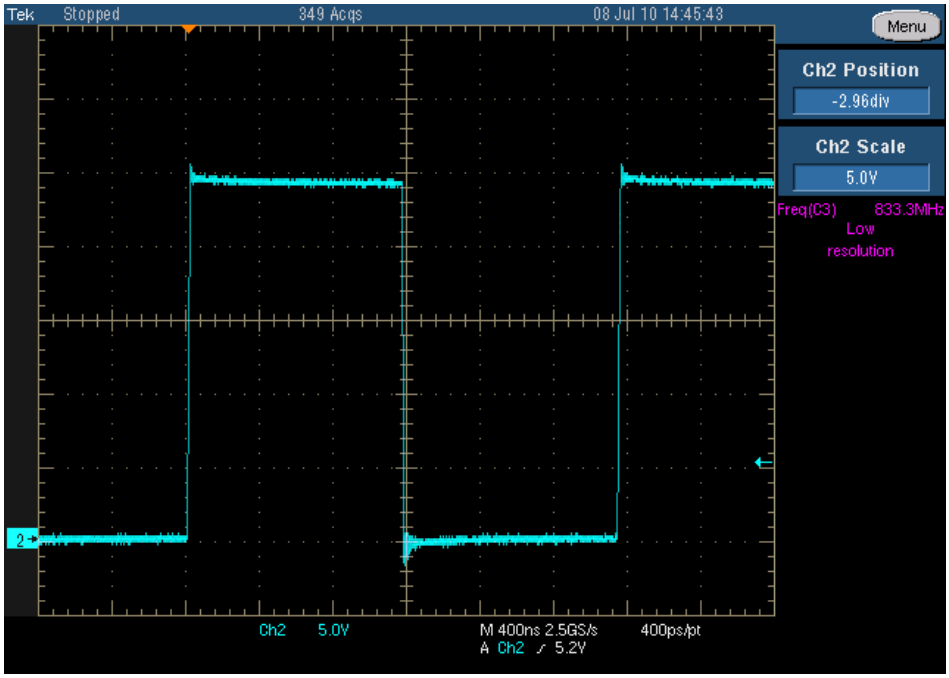
The images below show the switch-node waveforms for each converter, were the load was set to the maximum and the input voltage to the nominal value.

"+12V_ANT" output, U3 controller:

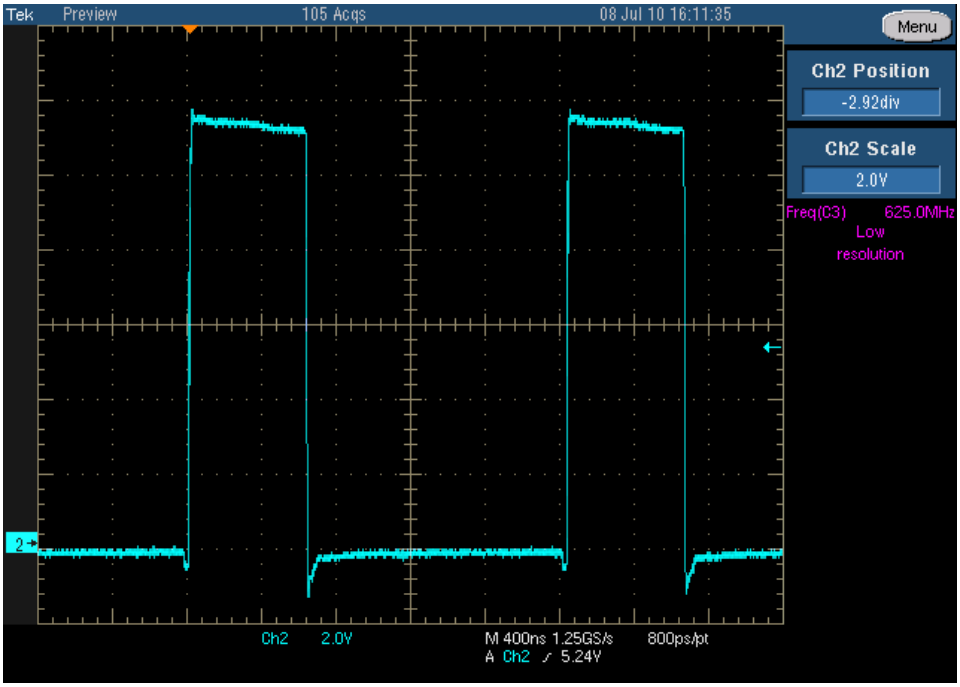
Channel 2: Q3 drain, (10V/div, 400nsec/div), no bandwidth reduction.



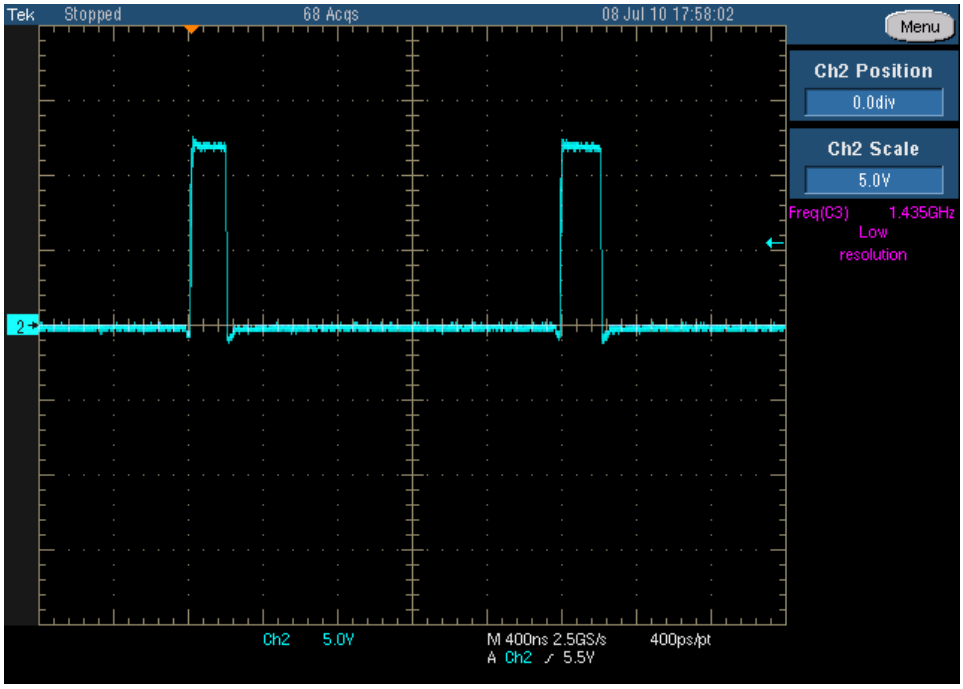
“+24V_ANT” output, U4 controller:
Conditions: Input voltage: 12V, Output load: 150mA
Channel 2: “SW” pin, (5V/div, 400nsec/div), no bandwidth reduction.



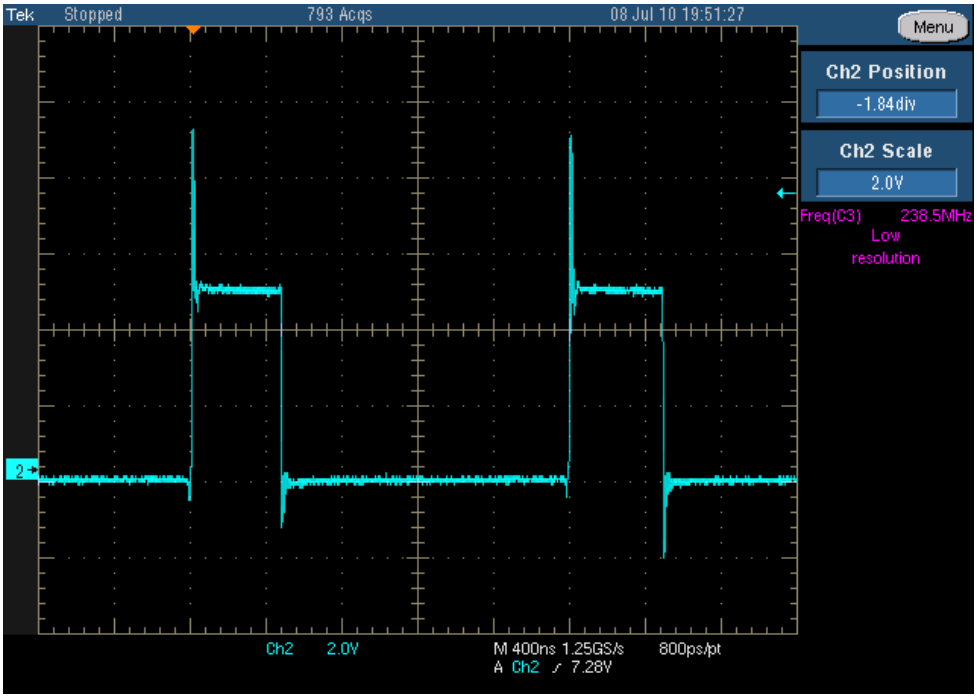
“+3V3_IO” output, U12 controller:
Conditions: Input voltage: 12V, Output load: 5A
Channel 2: “PH” pin, (2V/div, 400nsec/div), no bandwidth reduction.



“+1V2_FPGA” output, U16 controller:
Conditions: Input voltage: 12V, Output load: 2A
Channel 2: “PH” pin, (5V/div, 400nsec/div), no bandwidth reduction.

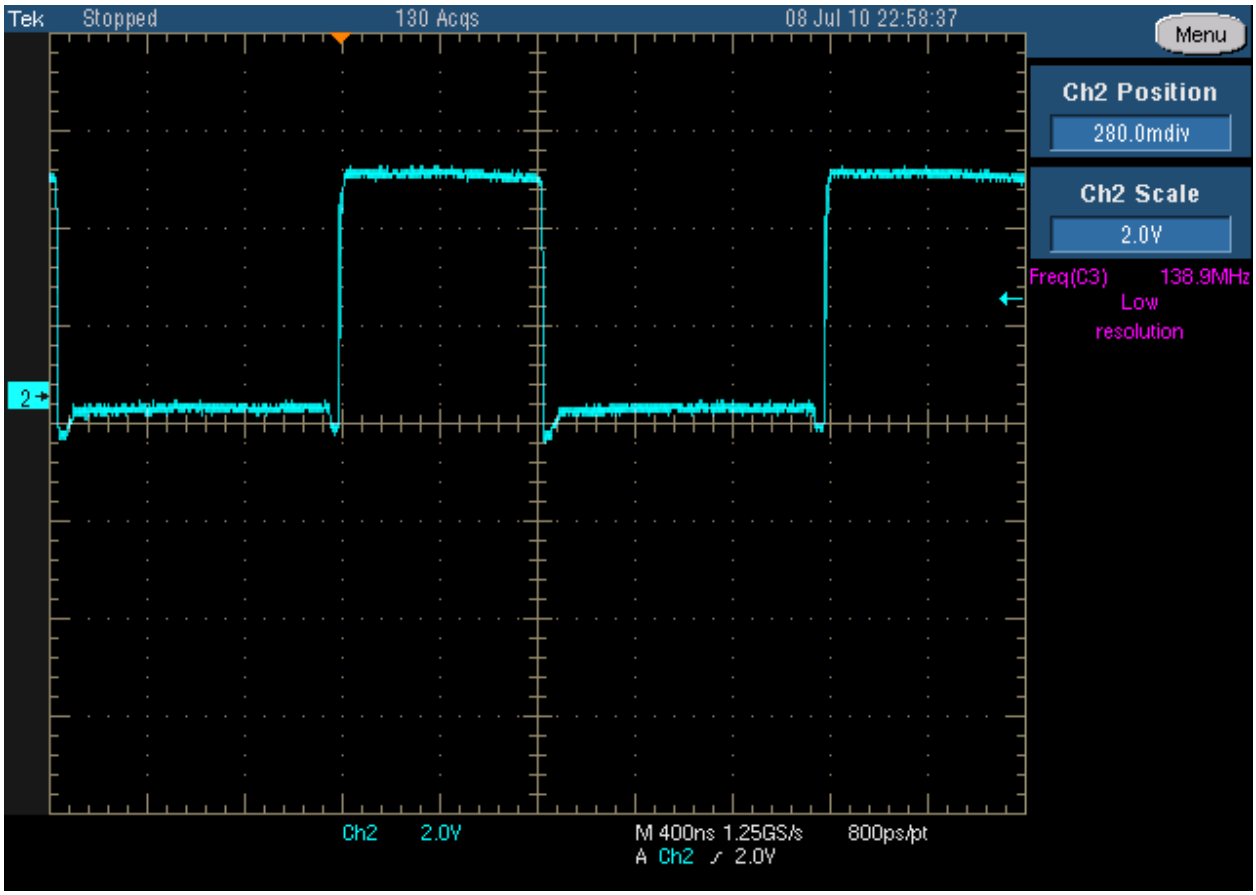


“+1V05_CORE” output, U19 controller:
Conditions: Input voltage: 5V, Output load: 7A
Channel 2: TP37, (2V/div, 400nsec/div), no bandwidth reduction.



“+1V8_DDR2” output, U22 controller:
Conditions: Input voltage: 5V, Output load: 4A

Channel 2: “PH” node, (2V/div, 400nsec/div), no bandwidth reduction.

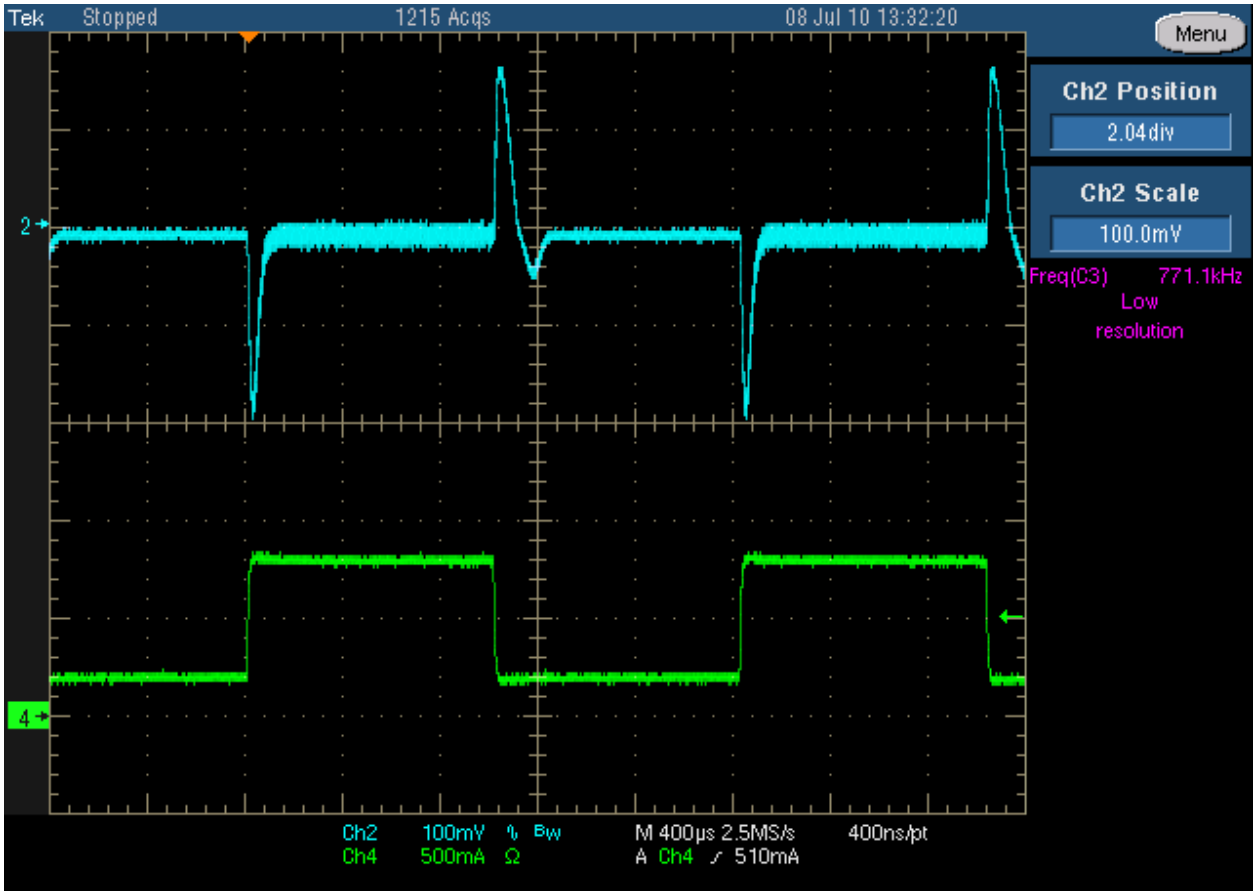


5. Transient Response

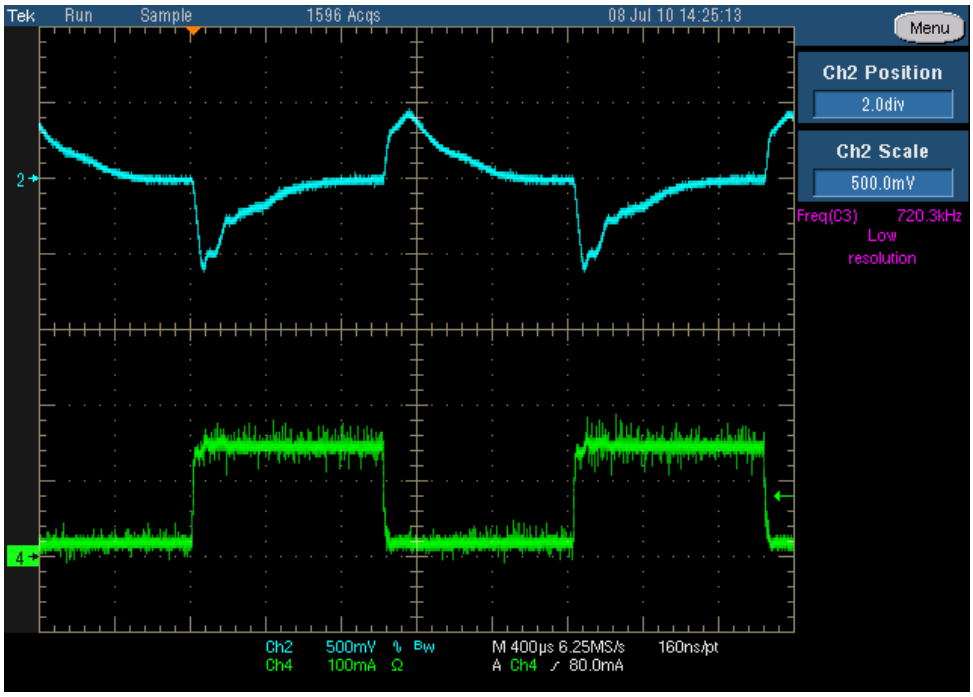
The images below shows the transient behavior for each converter were the output load was switched from 20% to 100% and back to 20%.

“+12V_ANT” output, U3 controller:
Conditions: Input voltage: 12V, Output load: 0.2A to 0.8A

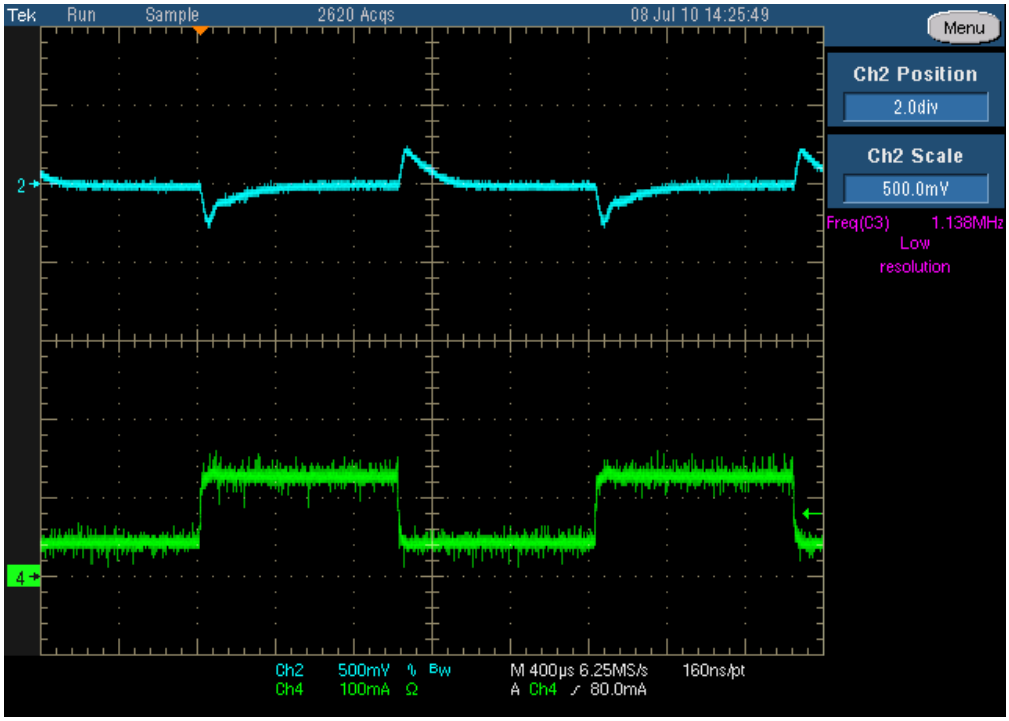
Channel 2: Output voltage (100mV/div, AC coupled, 400usec/div, 20MHz BW)
Channel 4: Output current (500mA/div, DC coupled)



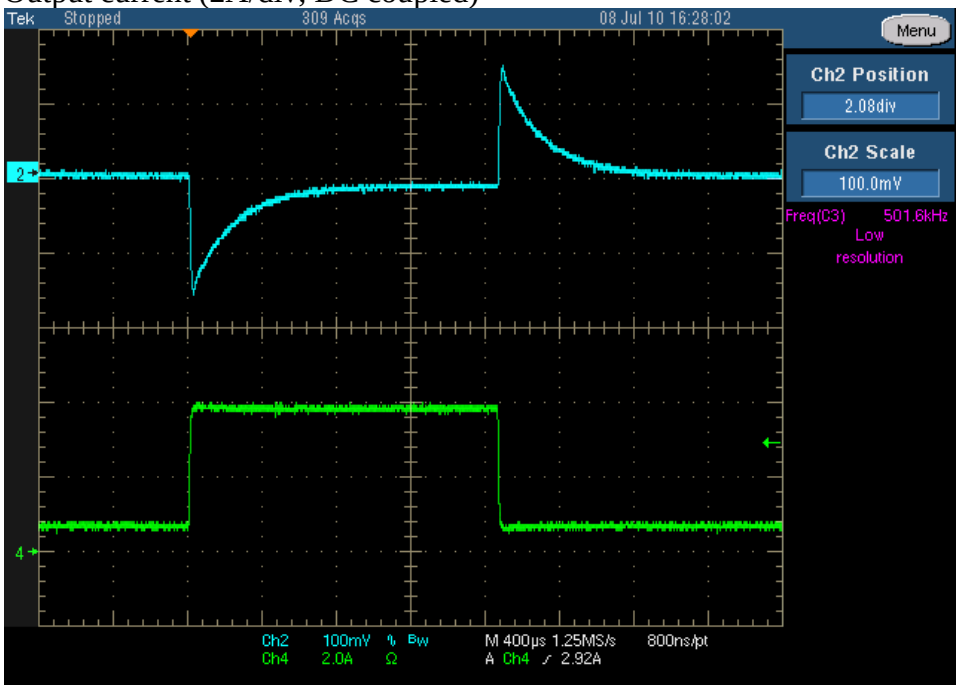
"+24V_ANT" output, U4 controller:
Conditions: Input voltage: 12V, Output load: 30mA to 150mA
Channel 2: Output voltage (500mV/div, AC coupled, 400usec/div, 20MHz BW)
Channel 4: Output current (100mA/div, DC coupled)



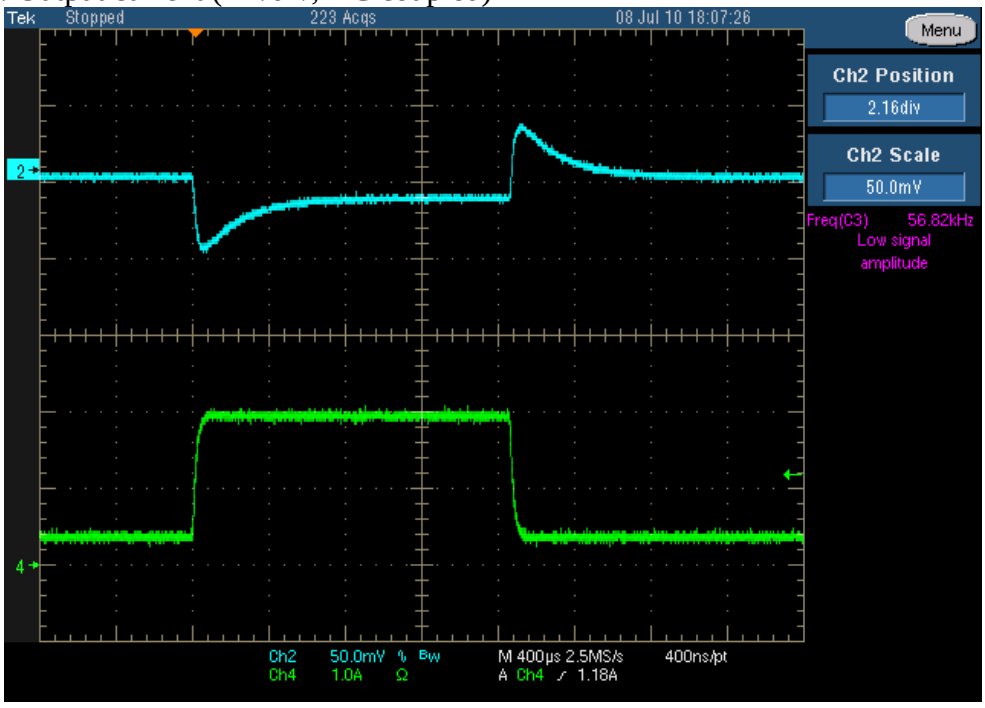
SAME Conditions, but the load was switched from 60mA to 150mA



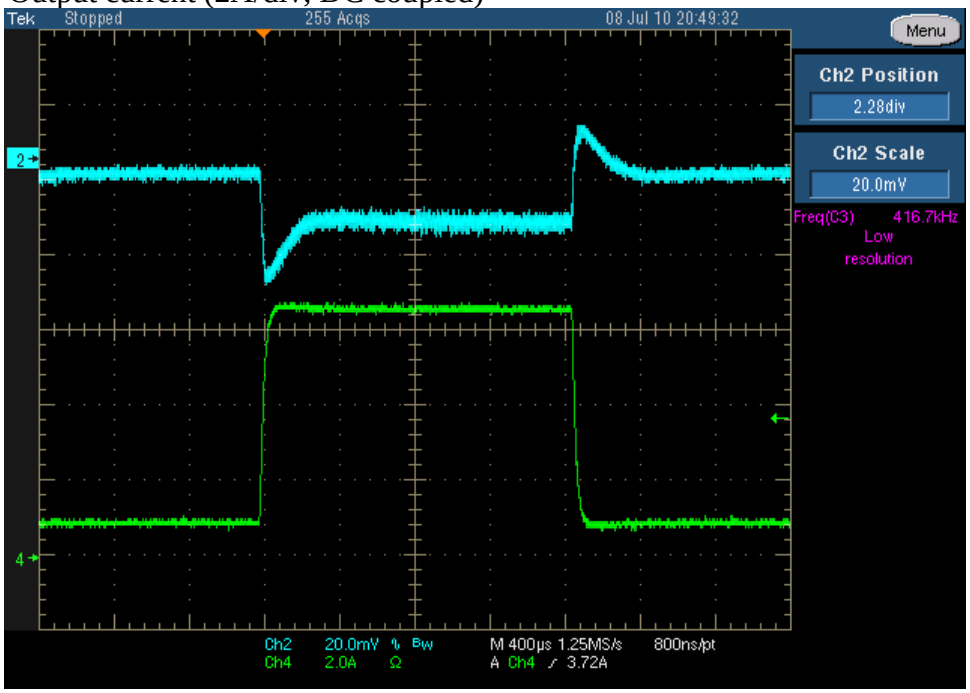
“+3V3_IO” output, U12 controller:
Conditions: Input voltage: 12V, Output load: 0.8A to 4A
Channel 2: Output voltage (100mV/div, AC coupled, 400usec/div, 20MHz BW)
Channel 4: Output current (2A/div, DC coupled)



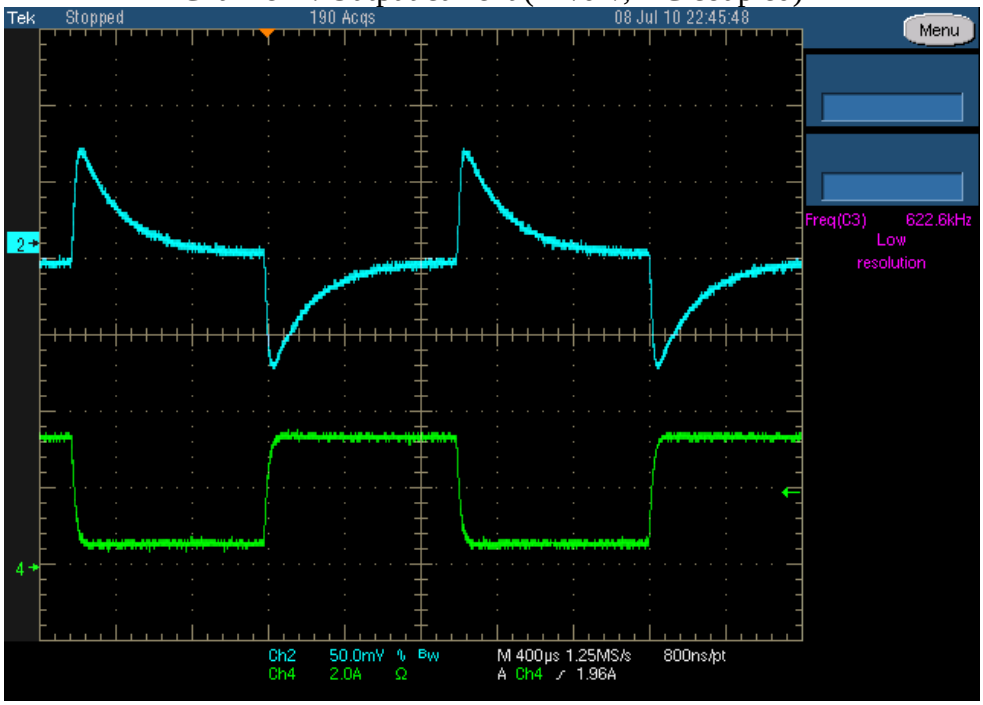
“+1V2_FPGA” output, U16 controller:
Conditions: Input voltage: 12V, Output load: 0.4A to 2A
Channel 2: Output voltage (50mV/div, AC coupled, 400usec/div, 20MHz BW)
Channel 4: Output current (1A/div, DC coupled)



“+1V05_CORE” output, U19 controller:
Conditions: Input voltage: 5V, Output load: 1A to 6.5A
Channel 2: Output voltage (20mV/div, AC coupled, 400usec/div, 20MHz BW)
Channel 4: Output current (2A/div, DC coupled)



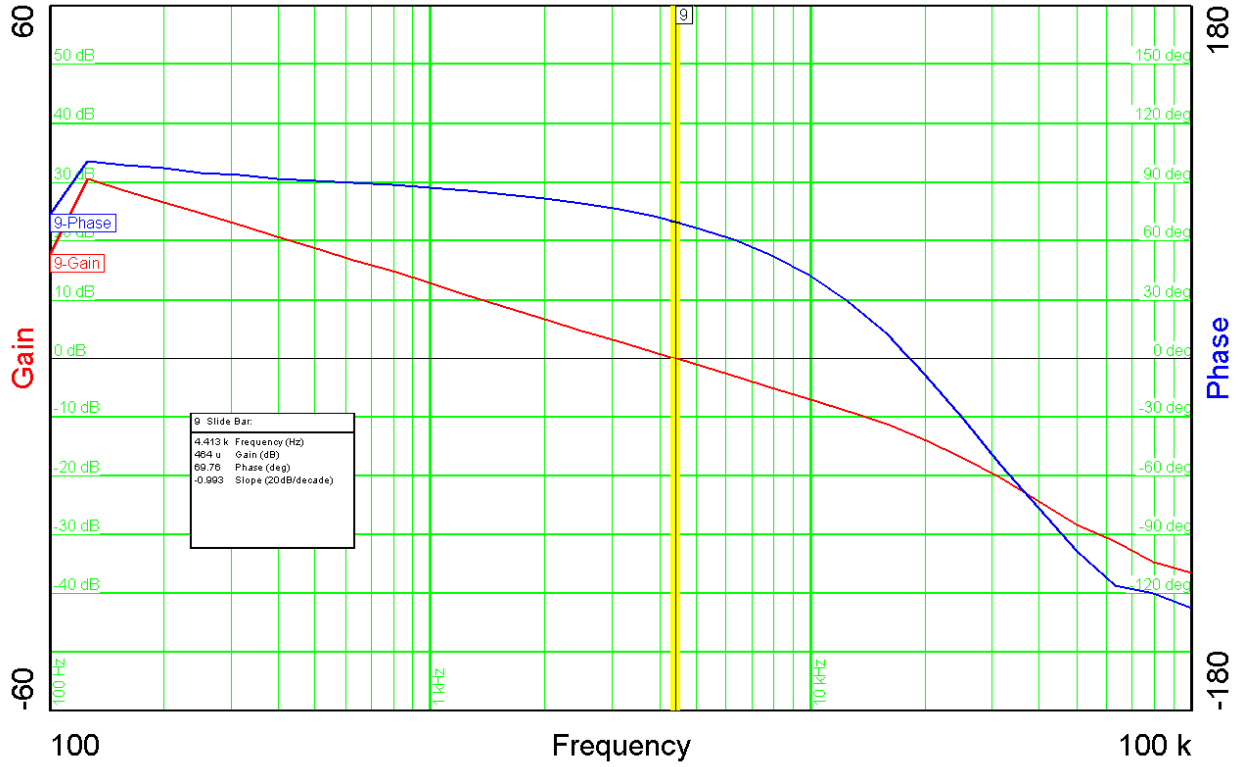
“+1V8_DDR2” output, U22 controller:
Conditions: Input voltage: 5V, Output load: 0.7A to 3.5A
Channel 2: Output voltage (50mV/div, AC coupled, 400usec/div, 20MHz BW)
Channel 4: Output current (2A/div, DC coupled)



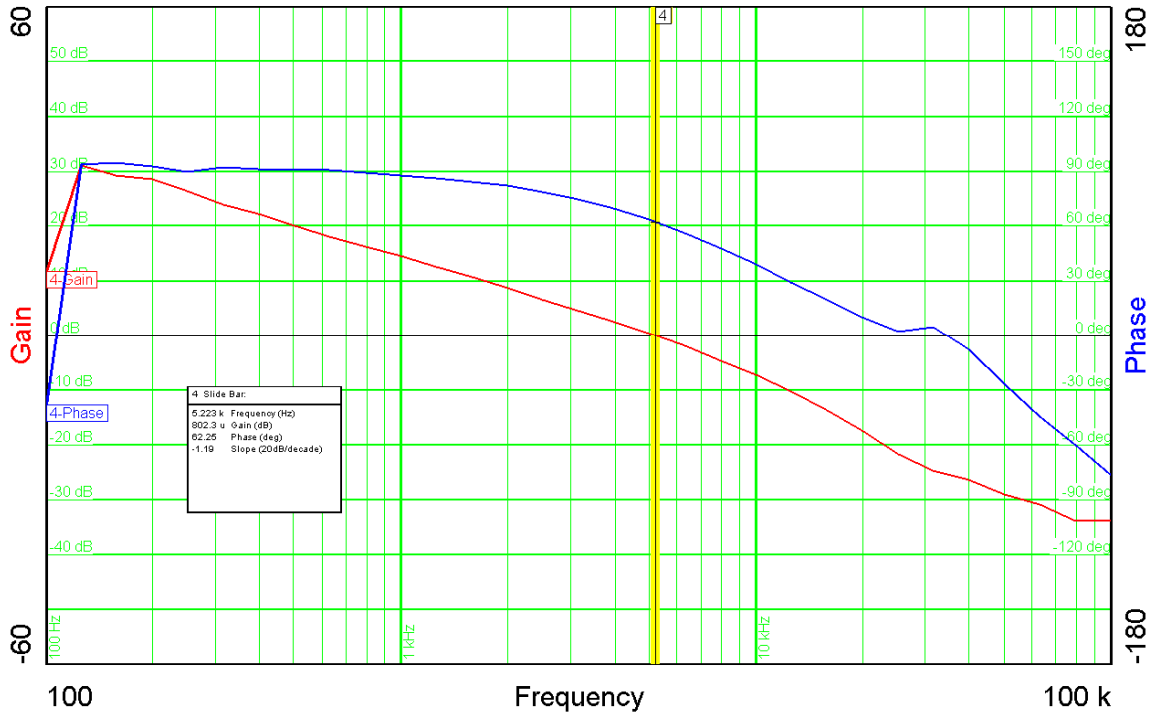
6. Loop Response

The images below show the loop response of the converters measured with a the nominal input voltage, and nominal output load.

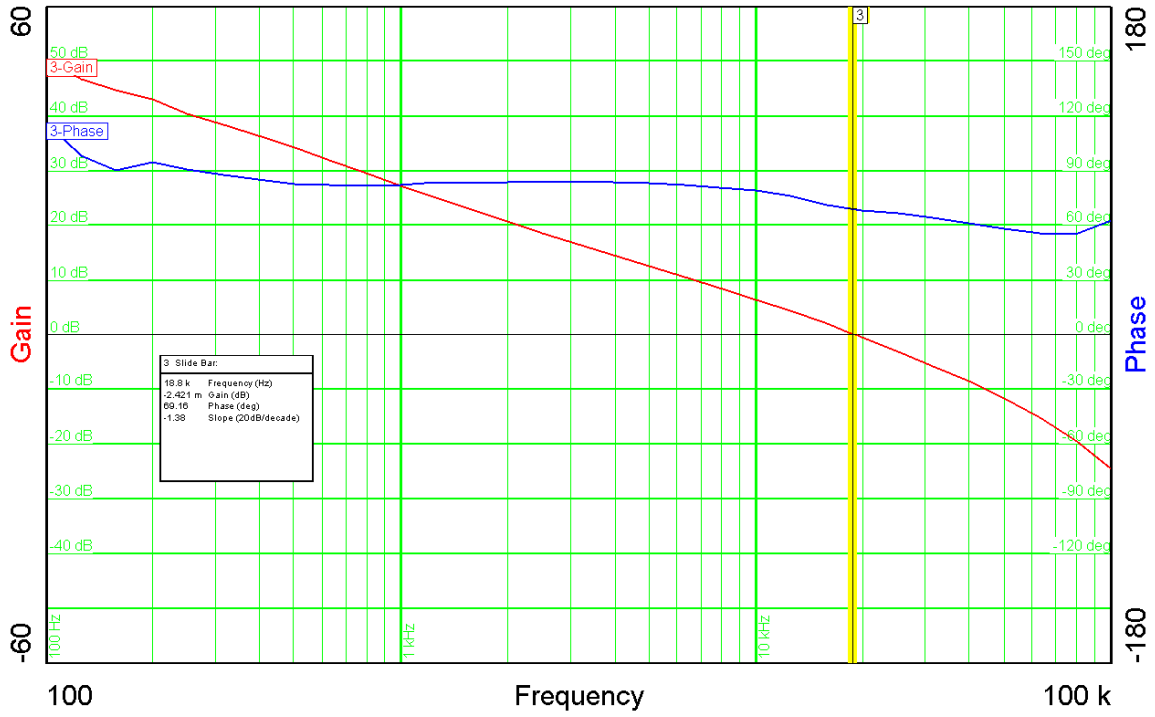
U3:



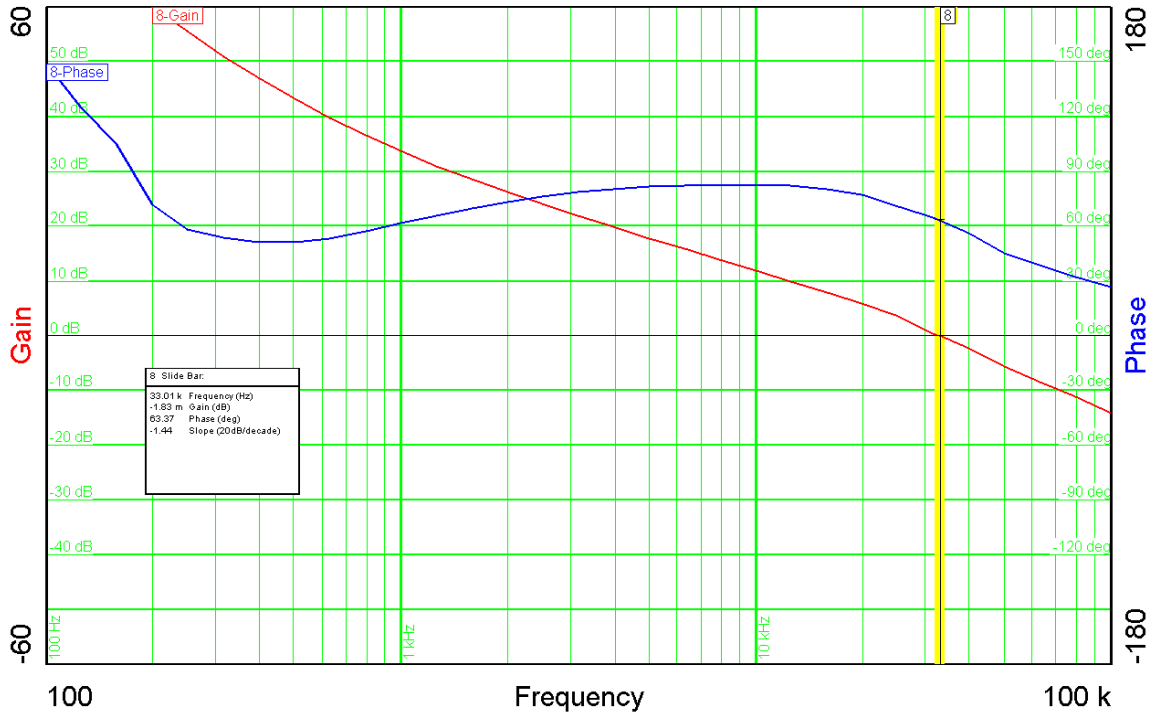
U4:


60
50 dB
40 dB
30 dB
20 dB
4-Gain
0 dB
-10 dB
4-Phase
-20 dB
-30 dB
-40 dB
-60
Gain
100 Hz
1 kHz
10 kHz
4
180
150 deg
120 deg
90 deg
60 deg
30 deg
0 deg
-30 deg
-60 deg
-90 deg
-120 deg
-180
Phase
4 Slide Bar:
5.223 k Frequency (Hz)
802.3 u Gain (dB)
62.25 Phase (deg)
-1.19 Slope (20dB/decade)
100
Frequency
100 k

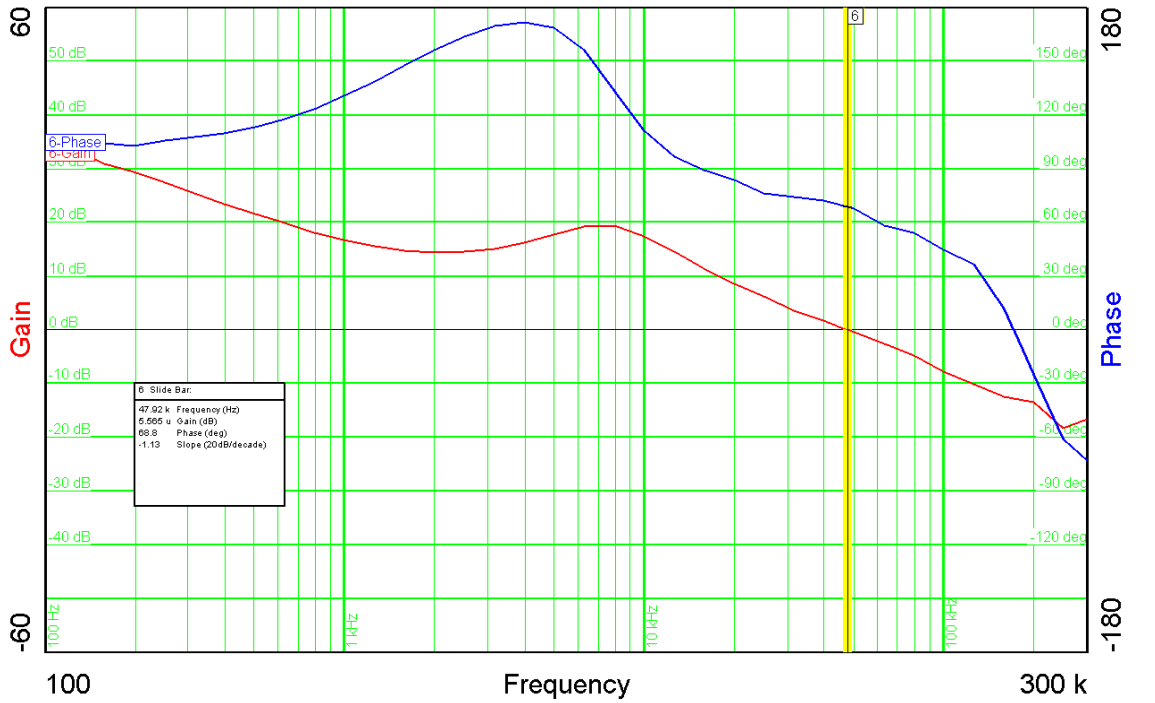
U12:


60
50 dB
3-Gain
40 dB
3-Phase
30 dB
20 dB
10 dB
0 dB
-10 dB
-20 dB
-30 dB
-40 dB
-60
Gain
100 Hz
1 kHz
10 kHz
3
180
150 deg
120 deg
90 deg
60 deg
30 deg
0 deg
-30 deg
-60 deg
-90 deg
-120 deg
-180
Phase
3 Slide Bar:
18.8 k Frequency (Hz)
-2.421 m Gain (dB)
69.16 Phase (deg)
-1.38 Slope (20dB/decade)
100
Frequency
100 k

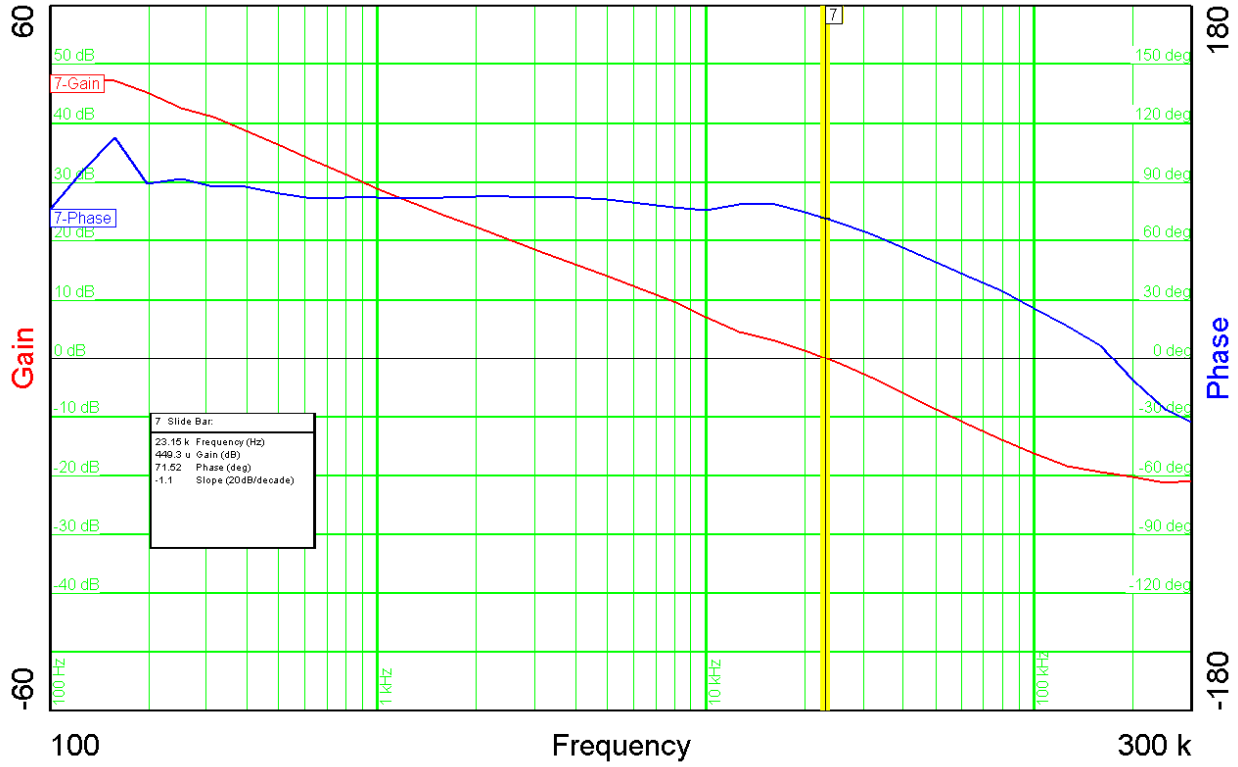
U16:


8-Gain
8-Phase
8
50 dB
40 dB
30 dB
20 dB
10 dB
0 dB
-10 dB
-20 dB
-30 dB
-40 dB
150 deg
120 deg
90 deg
60 deg
30 deg
0 deg
-30 deg
-60 deg
-90 deg
-120 deg
8 Slide Bar:
33.01 k Frequency (Hz)
-1.83 m Gain (dB)
63.37 Phase (deg)
-1.44 Slope (20dB/decade)
100 Hz
1 kHz
10 kHz
60
-60
180
-180
Gain
Phase
100
Frequency
100 k

U19:


6-Phase
6-Gain
6
50 dB
40 dB
20 dB
10 dB
0 dB
-10 dB
-20 dB
-30 dB
-40 dB
150 deg
120 deg
90 deg
60 deg
30 deg
0 deg
-30 deg
-60 deg
-90 deg
-120 deg
6 Slide Bar:
47.92 k Frequency (Hz)
6.565 u Gain (dB)
68.8 Phase (deg)
-1.13 Slope (20dB/decade)
100 Hz
1 kHz
10 kHz
100 kHz
60
-60
180
-180
Gain
Phase
100
Frequency
300 k

U22:


60
50 dB
7-Gain
40 dB
30 dB
7-Phase
20 dB
10 dB
0 dB
-10 dB
-20 dB
-30 dB
-40 dB
-60
Gain
7
180
150 deg
120 deg
90 deg
60 deg
30 deg
0 deg
-30 deg
-60 deg
-90 deg
-120 deg
-180
Phase
7 Slide Bar:
23.15 k Frequency (Hz)
449.3 u Gain (dB)
71.52 Phase (deg)
-1.1 Slope (20dB/decade)
100 Hz
1 kHz
10 kHz
100 kHz
100
Frequency
300 k

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated