User's Guide

BQ7961x-Q1 Design Recommendations for High Voltage Automotive BMS

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ABSTRACT

The BQ79616-Q1 provides high-accuracy cell voltage measurements for 6S to 16S battery modules in <200 µs. The integrated front end filters enable the system to implement simple, low-cost, differential RC filters on the cell input channels. The integrated, post-ADC, low-pass filters enable filtered, DC-like, voltage measurements for better SOC calculation. This device supports autonomous internal cell balancing with temperature monitoring to auto-pause and resume balancing to avoid an overtemperature condition.

The inclusion of the isolated, bidirectional, daisy chain ports supports both capacitor- and transformer-based isolation, allowing the use of the most effective components for centralized or distribution architectures commonly found in the xEV powertrain system. This device also includes eight GPIOs/auxiliary inputs that can be used for NTC thermistor measurements.

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Trademarks

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1 NPN LDO Supply

The device is powered by BAT pin and the LDOIN pin, with which the LDOIN pin is regulated by the pre-regulation circuit form with an external NPN. The device can be powered by a battery module with as low as 9V (without OTP programming) on the BAT pin.

The BAT and LDOIN pins should be filtered separately from the cell. This is to protect against hotplug, in-rush current, and other relevant noise. Recommended filters are R_{BAT} = 30 Ω / .25 W, C_{BAT} = 0.01 µF / 100 V for the BAT pin, two resistors in series for best thermal performance: R_{NPNC1} = 100 Ω / .75W, R_{NPNC2} = 200 Ω / .75 W and capacitor C_{NPNC} = 0.22 µF / 100 V for the collector. LDOIN is the input for the external LDO supply for the BQ79616-Q1. Figure 1-1 shows the typical circuit.

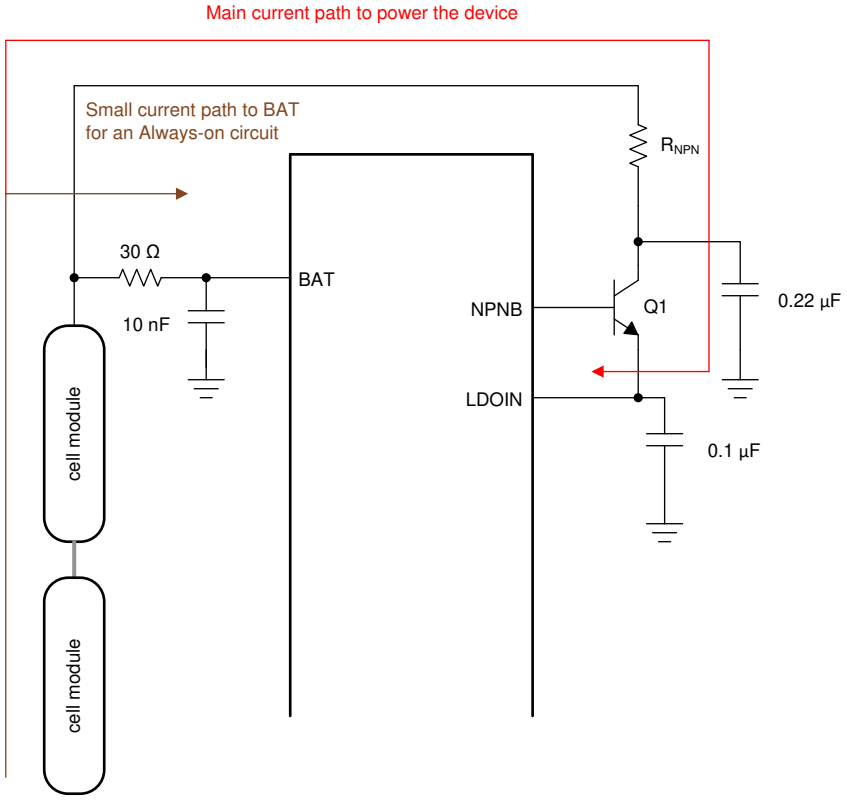


Figure 1-1. Power Supply Schematic

The resistor values and NPN can be further optimized from the reference schematic values based on the min and max module voltages for different projects.

Select the NPN Transistor based on the following criteria:

1. Collector-Emitter Breakdown Voltage (BV_{CEO}) > 80- 100 V (or the module voltage, plus any derating)
2. DC gain (β, or approximately equal to hfe (AC gain)) > 80 at the expected load current
3. Collector-based capacitance < 35 pF at typical base-voltage range
4. Power handling ≥ 1 W
5. Current handling > 100 mA

The resistor R_{NPNB} in Figure 1-1 serves several purposes:

1. Limits inrush current
2. Shares some power dissipation away from the NPN transistor
3. Combine with the C_{NPN} to serve as a filter

$$R_{MAX} = \frac{\left(V_{BAT(min)} - \left(V_{LDOOIN(max)} + V_{CE(SAT)}\right)\right)}{I_{LOAD(max)}} \quad (1)$$

where

- $V_{BAT(min)}$ is minimum battery module voltage which depends on the number of cells in series and minimum voltage per cell
- $V_{CE(SAT)}$ = V_{CE} min at $V_{BE(on)}$, from transistor data sheet
- I_{LOAD} is inrush current during startup or maximum active current and any external loading on CVDD

Connect the filter on the LDOIN supply (C_{LDOIN}) for stability. Use C_{LDOIN} = 0.1 µF with a voltage rating of 10 V.

2 AVDD, CVDD outputs and DVDD, NEG5, REFHP and REFHM

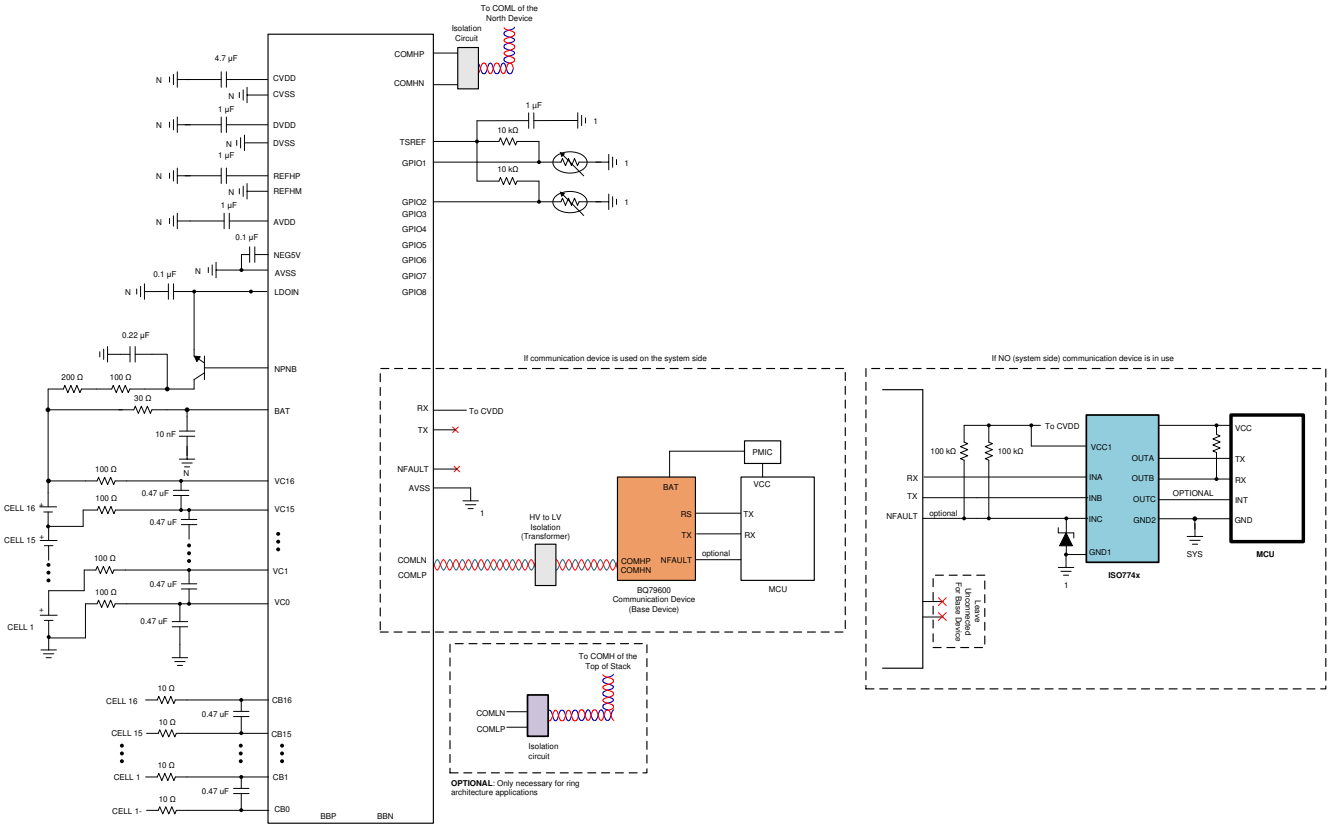
AVDD, CVDD, and DVDD are regulated outputs derived from the LDOIN input. Each of these regulator outputs should have a bypass capacitor to avoid noise with a 10% tolerance due to the fact that a larger capacitance slows startup. REFHP is an internal reference voltage and NEG5V is a regulated voltage provided by an internal charge pump.

Each regulator provides power for delicate internal subsystems. Do not connect external circuitry or additional loads to these regulators beyond those described in the data sheet.

The bypass capacitors of the following pins shall be placed as close to the device pins as possible to ensure proper performance, especially the REFHP capacitor. It is also recommended to help performance with derating and emissions performance to utilize a small capacitor in parallel with each bypass LDO capacitor of 10-22%. For example, on CVDD, we recommend both a 22-nF and 100-nF capacitors in parallel with 4.7-µF decoupling capacitor to help reduce emissions. These need to be designed extremely close to the pins of the IC in the layout for best effect.

2.1 Base Device

- AVDD is a 5-V regulated output which supplies internal circuits. AVDD must be bypassed to AVSS with a 1-µF/10-V capacitor. Do not connect any additional loads to AVDD.
- CVDD is a power supply for stack communication and tied to internally as I/O power supply. CVDD supplies the stack daisy chain communication transceiver circuit. Bypass CVDD with a 4.7 µF / 10 V and 100 nF and 22 nF for improved emissions and performance. capacitor to CVSS.
- DVDD is a 1.8-V regulated output that is used to power the digital logic inside the chip. Connect with a 1-µF/10-V capacitor to DVSS. Do not connect any additional loads to DVDD.
- NEG5V is a -5-V supply provided by an internal charge pump. Connect with a 0.1-µF/10-V capacitor to AVSS.
- REFHP is a precision reference output pin. A 1-µF/10-V bypass capacitor must be connected from REFHP to REFHM directly for proper operation of the part.
- REFHM is the precision reference ground for the internal precision reference. Connect DVSS, CVSS, ADC_AVSS, REFHM, and AVSS externally. All VSS pins must not be left unconnected.



Note

New recommendation to add 470 nF/16 V from CB16 to BAT for hotplug robustness not shown in figure, see data sheet for details.

Figure 2-1. Regulator Connection for Base Device

2.2 Design Summary

- Decouple bypass capacitors on AVDD, CVDD, DVDD, and REFHP pins to the ground plane. (Refer to layout guidelines for details.)
- Bypass the NEG5V pin to AVSS with a 0.1-µF/10-V capacitor.
- Put all capacitors as close to pins as possible.

3 OTP Programming

There are memory locations that are programmable in non-volatile memory (NVM) using OTP (One Time Progammable). The memory space is divided in two groups: factory space and customer space. The factory space stores the device configurations that are essential for normal operation. This space is not accessible by the host. The customer space contains the default device settings that the host system can customize for their application configuration. This space is readable and programmable by the host.

Follow the procedures found below for OTP programming:

1. Unlock the OTP programming.
   a. Write the following data to OTP_PROG_UNLOCK1A to OTP_PROG_UNLOCK1D:
      i. OTP_PROG_UNLOCK1A <- data 0x02
      ii. OTP_PROG_UNLOCK1B <- data 0xB7
      iii. OTP_PROG_UNLOCK1C <- data 0x78
      iv. OTP_PROG_UNLOCK1D <- data 0xBC
   b. Do another write with following data to OTP_PROG_UNLOCK2A to OTP_PROG_UNLOCK2D registers.
      i. OTP_PROG_UNLOCK2A <- data 0x7E
      ii. OTP_PROG_UNLOCK2B <- data 0x12
      iii. OTP_PROG_UNLOCK2C <- data 0x08
      iv. OTP_PROG_UNLOCK2D <- data 0x6F

   Note

   Each block of registers must be written in order (that is A,B,C, then D) with no other writes or reads between. The best practice is to use the same Write command to update. If there is any attempt to update the registers out of sequence or if another register is written/read between writes, the entire sequence must be redone.
2. Check to confirm the OTP unlock procedure is successful.
   a. Read to confirm OTP_PROG_STAT[UNLOCK] = 1.

   Note

   Issuing a Read command after step 1 is allowed, but issuing a [PROG_GO] must be the next write command after the unlock procedures.
3. Select the proper OTP page and start the OTP programing.
   a. To program page1, set OTP_PROG_CTRL[PAGESEL][PROG_GO] = 0x01, OR
   b. To program page2, set OTP_PROG_CTRL[PAGESEL][PROG_GO] = 0x03.
4. Wait $\mathbf{t_{PROG}}$ for the OTP programming to complete.
5. Check to ensure there is no error during OTP programming. The following bits are expected to be ‘1’ after a successful OTP programming.
   a. OTP_PROG_STAT[DONE] = 1, OTP programming is done. No other bit shall be set in this register.
   b. If page 1 is programmed, OTP_CUST*_STAT*[PROGOK], [TRY], [OVOK] and [UVOK] bits shall be ‘1’. Other bits shall be ‘0’.
   c. If page 2 is programmed, OTP_CUST1_STAT[LOADED], [PROGOK], [TRY], [OVOK], and [UVOK] bits shall be ‘1’. Other bits in OTP_CUST*_STAT shall be '0'.
6. Issue a digital reset to reload the registers with the updated OTP values.
   a. CONTROL1[SOFT_RESET] = 1

During the programming procedure, the device performs a programming voltage stability test prior to actually programming the OTP. If a programming voltage fails the stability test, the device does not set the OTP_CUST*_STAT[TRY] bit, giving the customer another attempt to program the page again.

If the host incorrectly selected a page for programming, the OTP_PROG_STAT[PROGERR] bit is set. This indicates that the selected page is not available to be programmed. Select the correct page and retry programming.

4 Cell Voltage Sense (VCn) and Cell Balancing (CBn)

Voltage monitoring is done through the VCn pins while cell balancing is done through the CBn pins. Each of the VCn pins is measured by the main SAR ADC to ensure the most accurate readings. Getting an accurate reading for these connections is critical to achieve maximum performance so the following design recommendations should be followed.

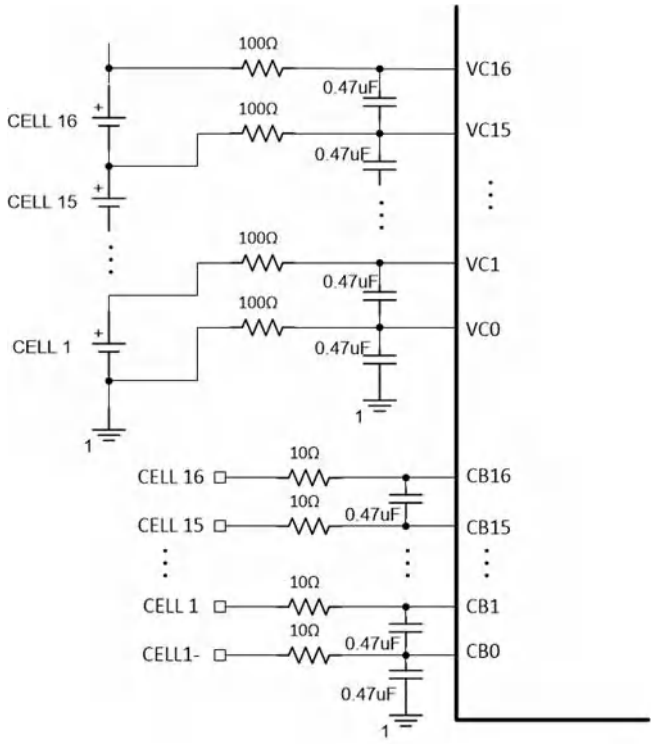
4.1 Cell Voltage Sense (VCn)

The VCn pins are the primary inputs for measuring the cell voltages. VC0 is the low side reference to the negative terminal of the bottom cell and VC16 is the high side reference to the positive terminal of the top cell.

The inputs should be connected to the cells using series resistors to limit current into the pins and protect the IC from system transients. When fewer than 16 cells are used on the BQ79616-Q1, the lower cells must be used in order. Unused cell connections can be found in the scenarios shown in Figure 4-1.

Recommended filter capacitor for VCn pins is 0.47 µF/16 V.

A 100 Ω is recommended as a series filter resistor for VCn pins. A 100 Ω is an optimized value to protect VCn pins from hotplug and provide better filtering. But if another value is considered other than 100 Ω, it should be simulated for selecting the optimized value for the system.



Note

New recommendation to add 470 nF/16 V from CB16 to BAT for hotplug robustness not shown in figure, see data sheet for details.

Figure 4-1. Cell Voltage Monitoring

4.2 Cell Balancing (CBn)

The device integrates internal cell balancing MOSFETs (CBFET) across each CB channel to enable passive cell balancing. The cell balancing control can be configured in two ways: auto and manual - using the *BAL_CTRL2[AUTO_BAL] bit*. To set up cell balancing control, refer to Set Up Cell Balancing section in the BQ79616-Q1 data sheet.

The balancing current is determined by the cell voltage, the external resistor in series with the CB pin, and the internal CBFET $R_{DS(ON)}$. This document will introduce how to select an external resistor to get the desired cell balancing current.

4.2.1 Non-Adjacent Cell Balancing

Auto balancing control is configured by setting [AUTO_BAL] = 1. In auto balancing control mode, CBFETs are enabled in an odd and even sequence.

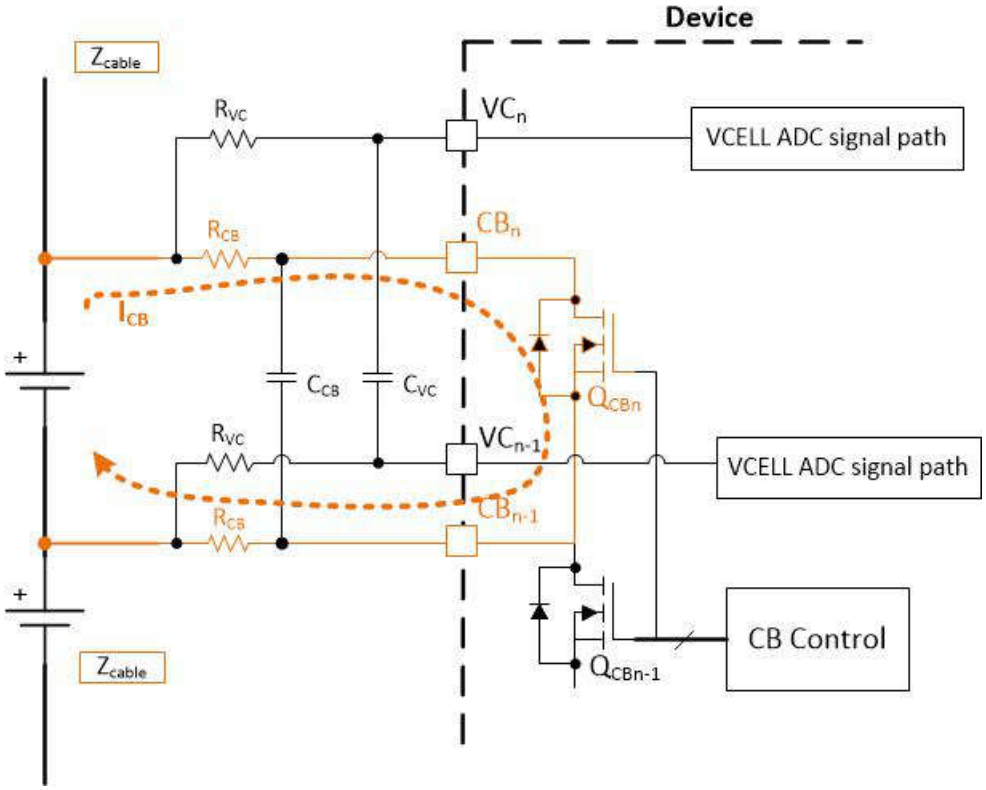


Figure 4-2. Internal CB Diagram (no adjacent cell balancing)

Figure 4-2 shows the cell balancing current path. Cell balancing current (I_{CB}) is dependent on cell voltage (V_{CELL}) and the resistance of the balancing path (2 × R_{CB}+ $R_{DS(ON)}$). The equation is shown in Equation 2. R_{CB} is the series resistor. $R_{DS(ON)}$ is the resistance of the internal FET when it is on. The higher the total resistance of the path, the lower the cell balancing current that flows.

To get a target cell balancing current, R_{CB} can be chosen by following two steps.

Step 1 : Select R_{CB} value

The R_{CB} value can be calculated considering the desired cell balancing current at the highest $R_{DS(ON)}$ at the highest operating temperature using the equation in Equation 3.

Step 2 : Calculate R_{CB} power rating

Power rating for R_{CB} can be calculated with the highest cell balancing current at the minimum $R_{DS(ON)}$. An example calculation for how to select the value of R_{CB} and power rating to get the desired cell balancing current is shown in Figure 4-3.

$$I_{CB} = \frac{V_{CELL}}{R_{DS(ON)} + 2 \times R_{CB}} \quad (2)$$

$$R_{CB} = \frac{1}{2}\left(\frac{V_{BAT}}{I_{CB}} - R_{DS(ON)}\right) \quad (3)$$

Cell Balancing Resistor Calculation Example

Assume desired cell Balancing Current is 240 mA at 80℃ with 4.2 cell voltage.

1. Calculation for Cell Balancing Resistor

$V_{BAT} = 4.2V \rightarrow$ Voltage of Battery

$I_{CB} = 240\ mA \rightarrow$ Desired Cell Balancing Current

$R_{DS(ON)} = 5\ \Omega \rightarrow$ Maximum Resistance of Internal FET at 80℃

$$R_{CB} = \frac{1}{2} \times \left(\frac{4.2\ V}{240\ mA} - 5\ \Omega \right)$$

$$R_{CB} = 6.25\ \Omega$$

2. Calculation for Power rating for R_{CB} at worst case

$V_{BAT} = 4.2V \rightarrow$ Voltage of Battery

$R_{CB} = 6.25\ \Omega \rightarrow$ Cell Balancing Resistor

$R_{DS(ON)} = 1.25\ \Omega \rightarrow$ Minimum Resistance of Internal FET at Cold Ambient

$$I_{CB} = \frac{V_{Cell}}{2 \times R_{CB} + R_{DS(on)}}$$

$$I_{CB} = \frac{4.2\ V}{2 \times 6.25\ \Omega + 1.25\ \Omega}$$

$$I_{CB} = 305\ mA$$

$$R_{CB}\ \text{Power rating} = V_{BAT} \times I_{CB}$$

$$R_{CB}\ \text{Power rating} = 305\ mA \times 4.2V$$

$$R_{CB}\ \text{Power rating} = 0.58\ \text{W}$$

Figure 4-3. Cell Balancing Resistor Example Calculation

Passive balancing dissipates heat to the die, increasing the die temperature as balancing current increases. Refer to the BQ79616-Q1 data sheet for the recommended maximum balancing current according to the ambient temperature.

4.2.2 Adjacent Cell Balancing

Manual balancing control is configured by setting [AUTO_BAL] = 0. In manual balancing control mode, the host can enable two consecutive CBFETs, and a maximum of eight total CBFETs can be enabled (see Figure 4-4).

However, when two adjacent channels are enabled, the balancing current is twice as high or higher than the non-adjacent channel balancing current. The system designer shall take this into account if adjacent cell balancing is used. See Equation 4 to select the right adjacent cell balancing series resistor (R_{CB}).

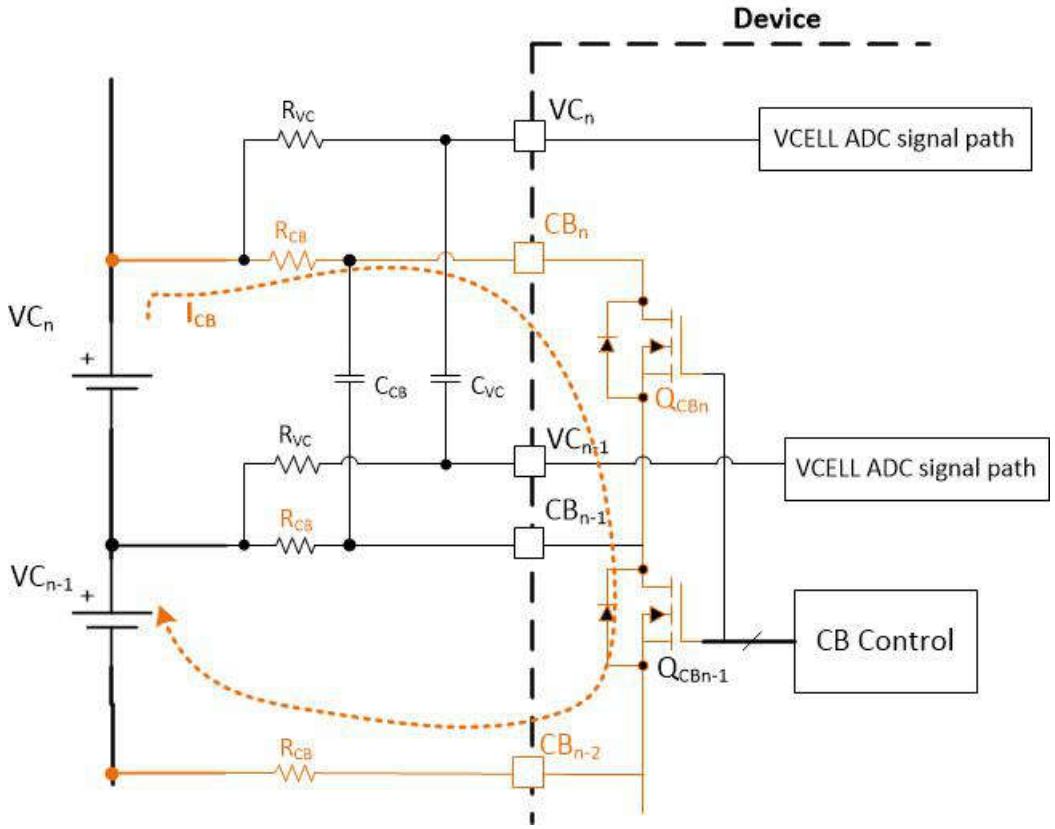


Figure 4-4. Adjacent Cell Balancing

$$I_{CB} = \frac{2 \times V_{Cn}}{(2 \times RCB) + Rdson(Q_{CBn}) + Rdson(Q_{CBn-1})} \quad (4)$$

4.2.3 Cell Balancing With External FET

The BQ79616-Q1 can handle 240 mA max at 105°C. Should more current be needed, the cell balancing pins are able to support an external FET as shown in Figure 4-5. Cell balancing current with external FET can be calculated using equation below. Details for that configuration can be found in the BQ79616-Q1 data sheet.

There are a few things to keep in mind regarding external balancing. First, the series resistors between the FET and pin are there to protect the pins during hot plug and the capacitor is there to ensure that the FET does not turn on during hot plug. Also be aware of the following conditions that should be considered when selecting the FET.

1. The V_{DS} must be selected based on derating requirements determined by the stack voltage.
2. The V_{GS} threshold must be low enough to turn on with the lowest battery voltage planned for balancing. The gate of the MOSFET sees half of the battery voltage, so the V_{GS} of the MOSFET must be selected to provide sufficiently low $R_{DS(ON)}$ at half of the lowest battery voltage.

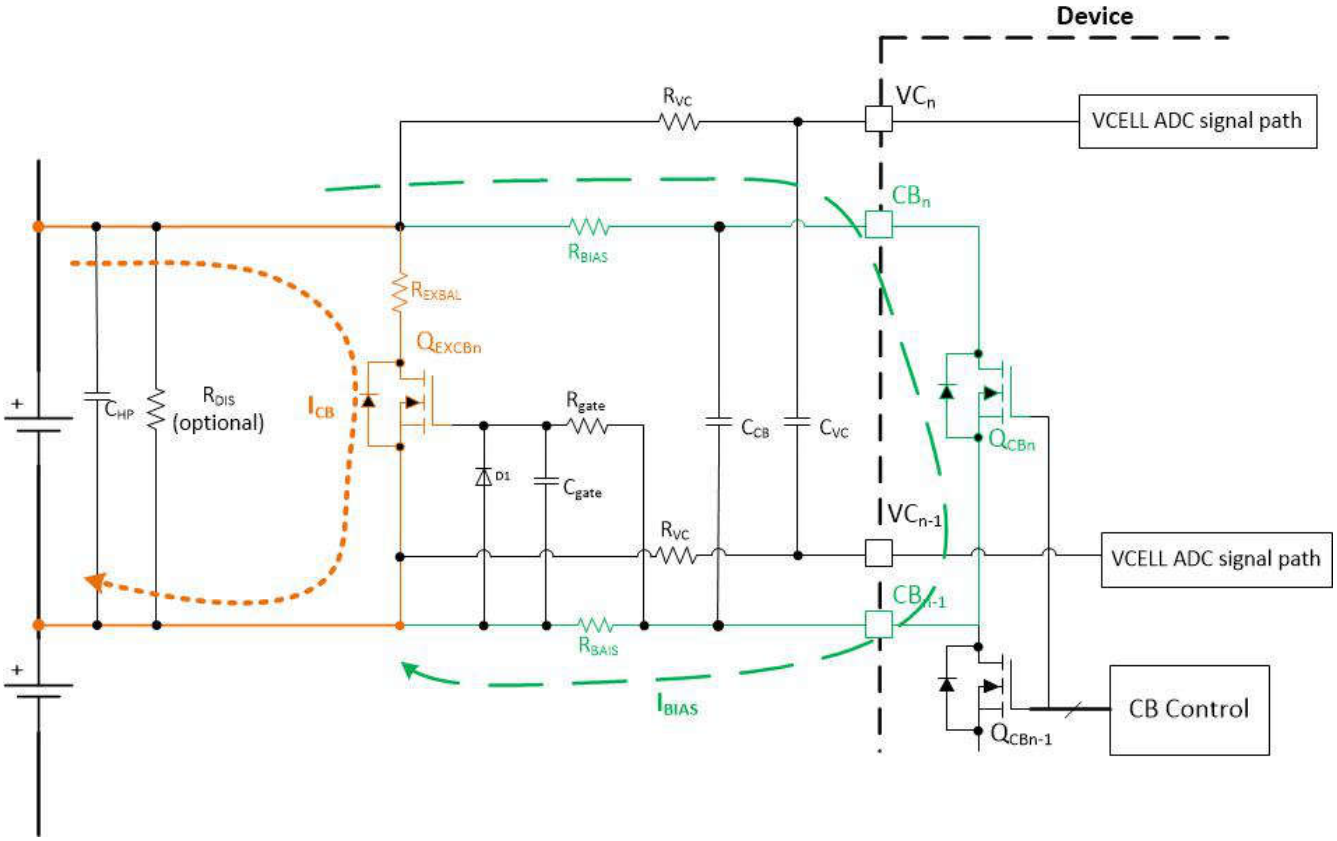
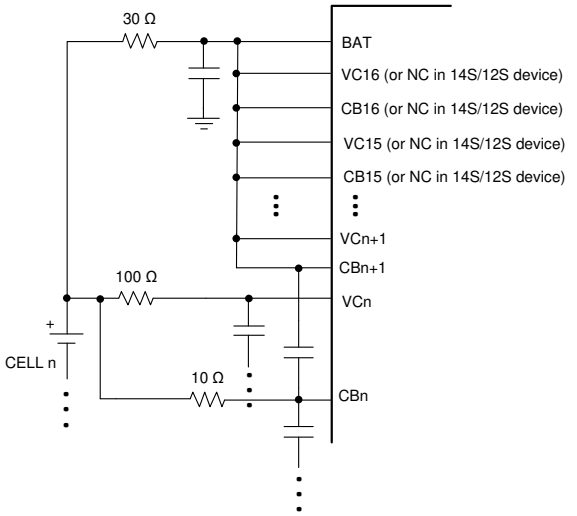


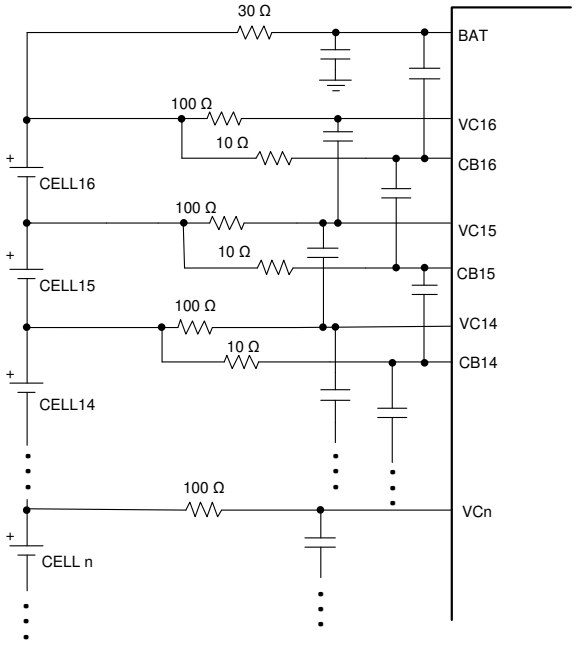
Figure 4-5. External FET Cell Balancing

4.3 Using Fewer Than 16 Cells

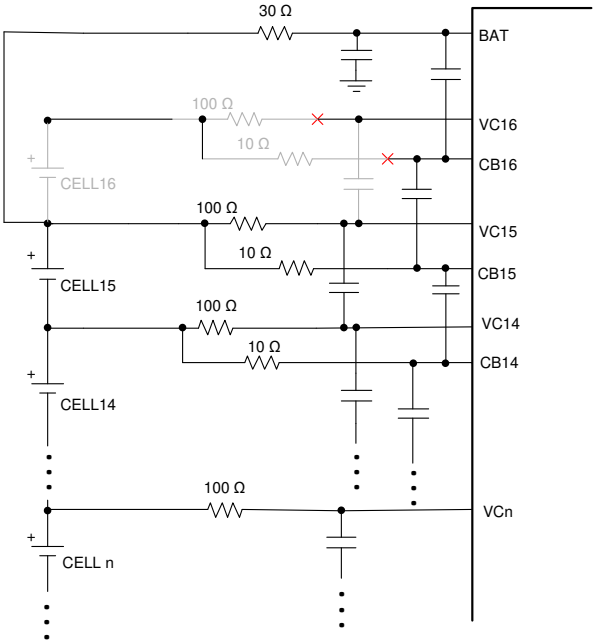
As stated earlier, the BQ79616-Q1 can support between six and 16 cells. The VCn inputs must be used in ascending order starting with VC0. See Figure 4-6 scenarios for more information on connecting fewer than 16 cells.



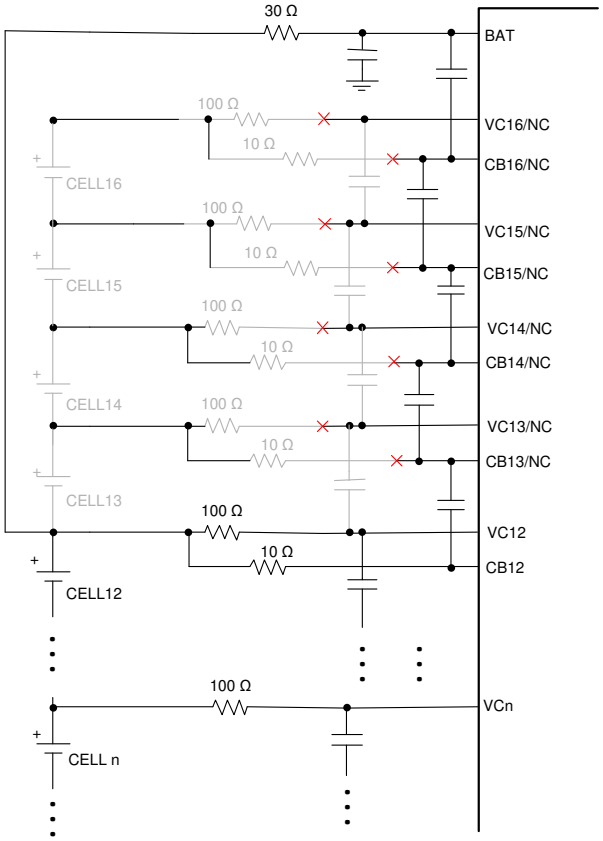
(a) Customized PCB for certain channels applications - Short unused pins to BAT Pin



(b) One PCB for all channels applications – For BQ79616: Configured for 16 VC and CB



(c) One PCB for all channels applications – For BQ79616: Configured for 15 VC and CB
If floating the unused VC and CB pins, capacitors in black corresponding to CB pins need to be populated, but capacitors and resistors in grey corresponding to VC and CB pins need to be unpopulated



(d) One PCB for all channels applications – For BQ79612: Configured for 12 VC and CB
If floating the unused VC and CB pins, capacitors in black corresponding to CB pins need to be populated, but capacitors and resistors in grey corresponding to VC and CB pins need to be unpopulated

Figure 4-6. Connecting Fewer Than 16 Cells

4.3.1 Design Summary

- Cell balancing current, I_{CB}, is dependent on cell voltage and resistance of the path.
- The CBn resistor value must be selected considering desired balancing current at the highest ambient temperature. Use the formula in Equation 3 to calculate the correct resistance.
- A 100-Ω resistor is recommended as a series resistor for VCn pins. A 100 Ω is an optimized value to protect VCn pins and provide accuracy in cell voltage readings.
- VCn input connections must start with the lowest input, VC0, and then be connected in ascending order.
- CBn inputs used must correspond to the VCn used.
- For more than 240 mA of charging current, use an external FET. Details can be found in the BQ79616-Q1 data sheet.

5 Bus Bar Support

The device supports bus bar measurement in two type of connections. First, the bus bar can be connected to a dedicated bus bar channel through the BBP and BBN pins. Alternatively, the bus bar can be connected to a VC channel. This section will introduce both methods of connecting the bus bar and cell balancing handling for each configuration.

5.1 Bus Bar on BBP/BBN

The device provides a dedicated bus bar channel through the BBP/BBN pins for bus bar connection and measurement. It is a “floating” channel allowing the bus bar to be connected to any cell except the bottom cell of a module.

Instead of using the BBP/BBN with the bottom cell (VC1-VC0), the bus bar could be connected to the BBP/BBN of the lower stack device alternatively as shown as Figure 5-1.

Using the bus bar channel maximizes the use of cell channels in the device across different module size. As described in Figure 5-2, 4 x 12 cell can be monitored by 3 CMC without wasting any pins while connecting the bus bar to BBP/BBN.

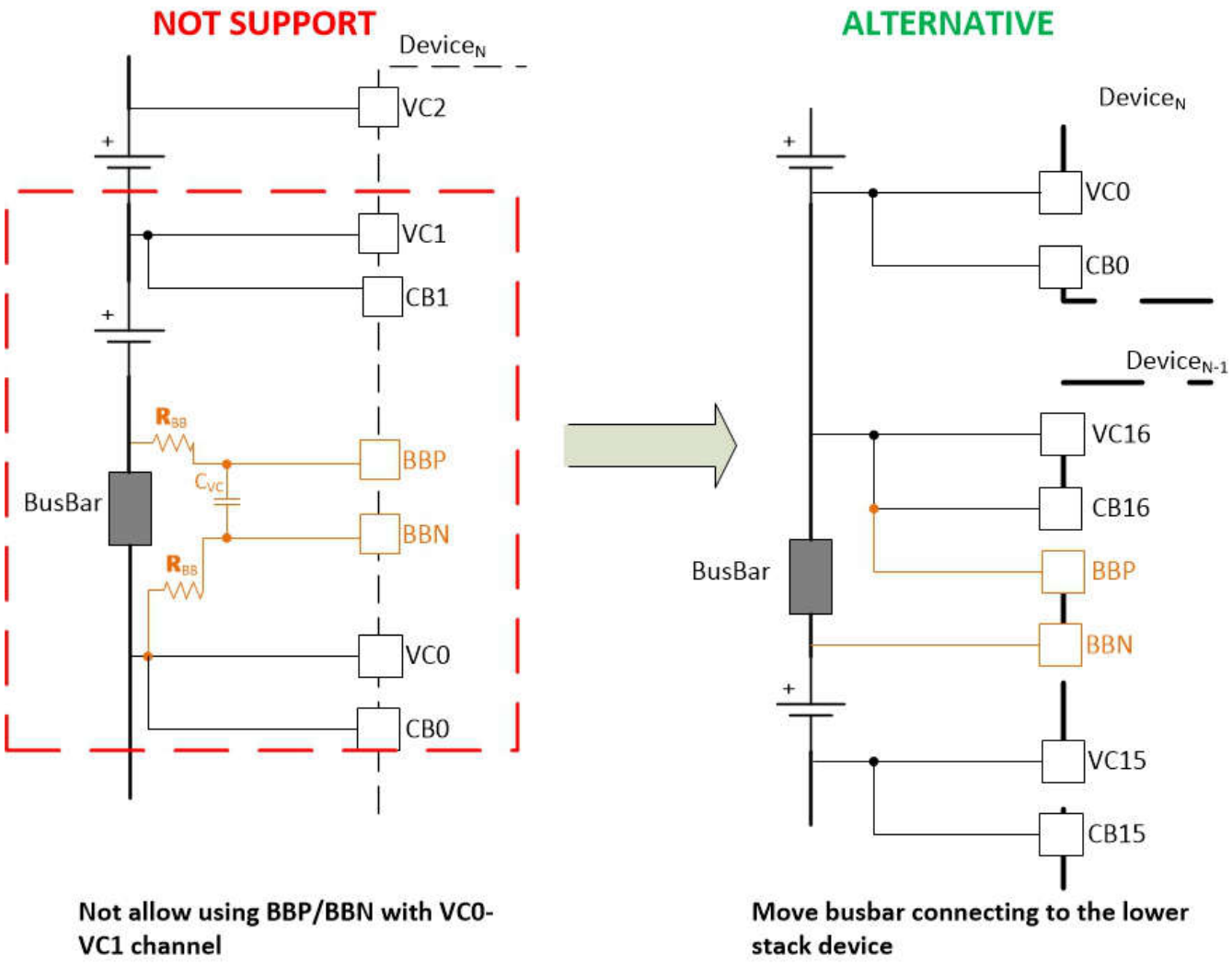
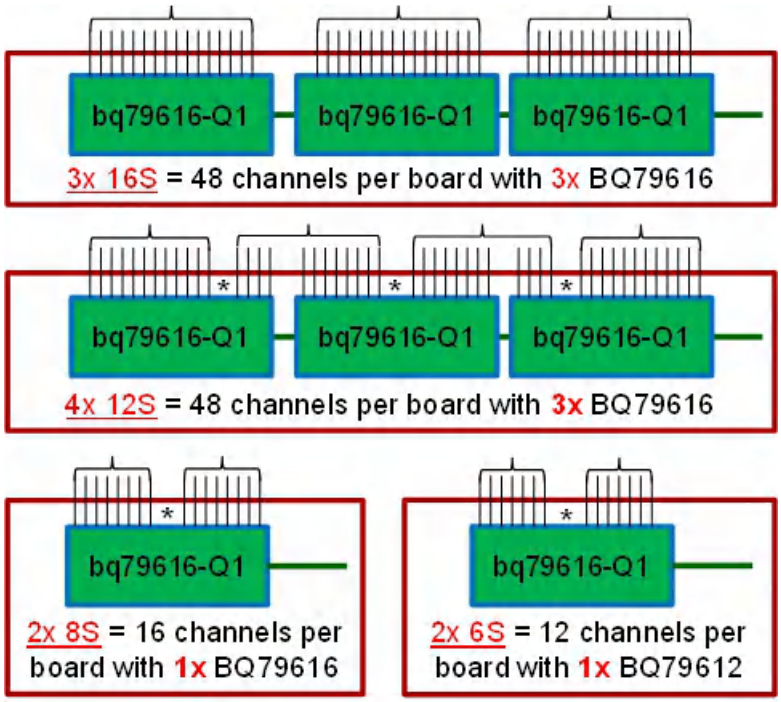


Figure 5-1. Alternative Bus Bar Connection to the Lower Stack Device



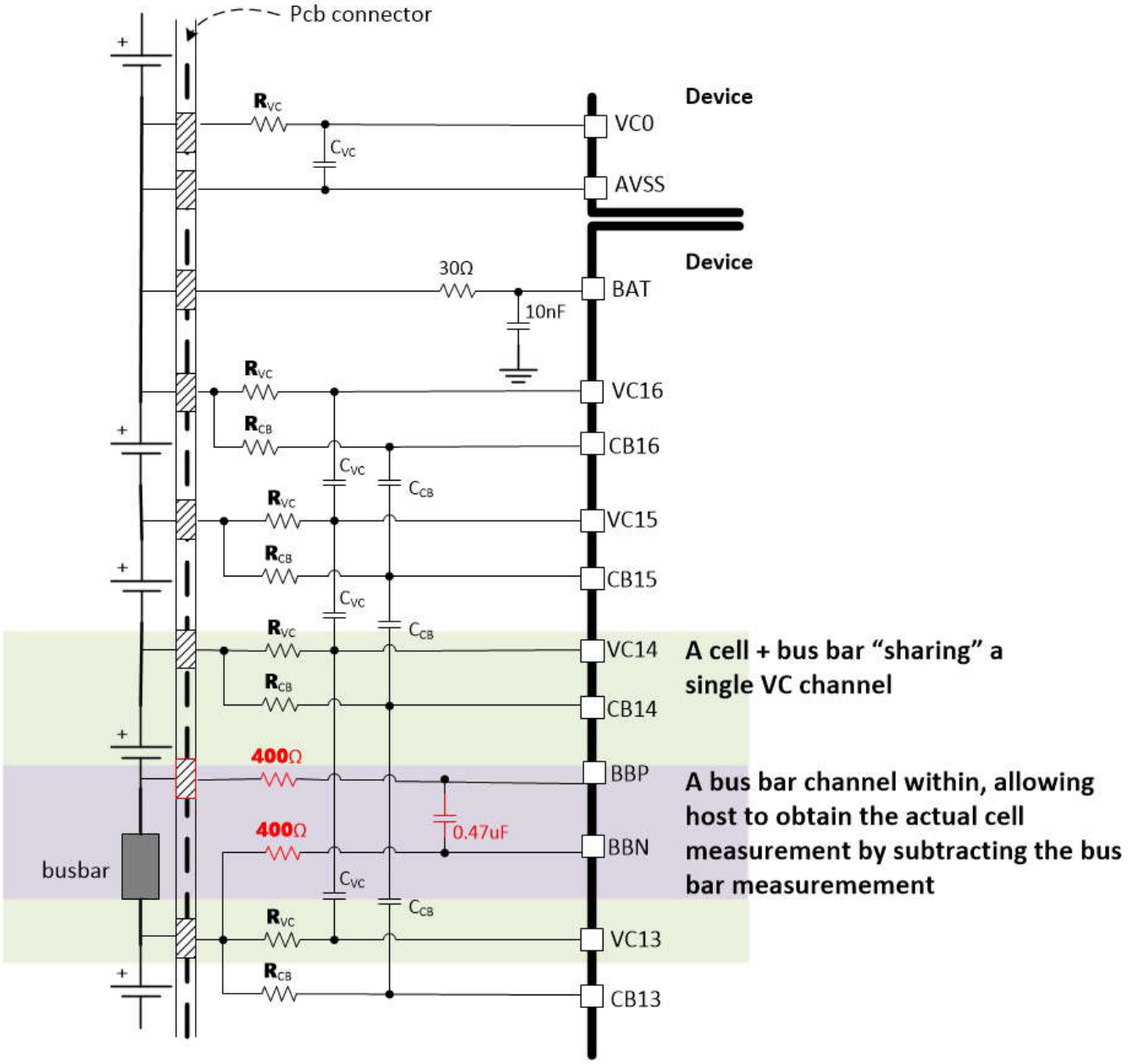
The * represents the bus bar location at each module size example.

Figure 5-2. Example of BBP/BBN Connections at Different Module Size

5.2 Typical Connection

With the bus bar connected to BBP/BBN, it is intended to allow a single cell channel (VC channel) to be shared with a cell + a bus bar (see Figure 5-3 connection). Usually, such a connection introduces additional IR error to the cell measurement to the system. The dedicated bus bar channel through BBP/BBN supported in the device allows the host to measure the bus bar voltage to obtain the actual cell measurement.

The connection in Figure 5-3 applies if the bus bar is connected to any middle VC channel. That is, in a single device, there is a cell connected above and below the BBP/BBN channel. To support hotplug on the bus bar channel, the device only requires a 400-Ω filter resistor each on BBP/N pins and a 0.47-µF/16-V differential capacitor across BBP/N pins.



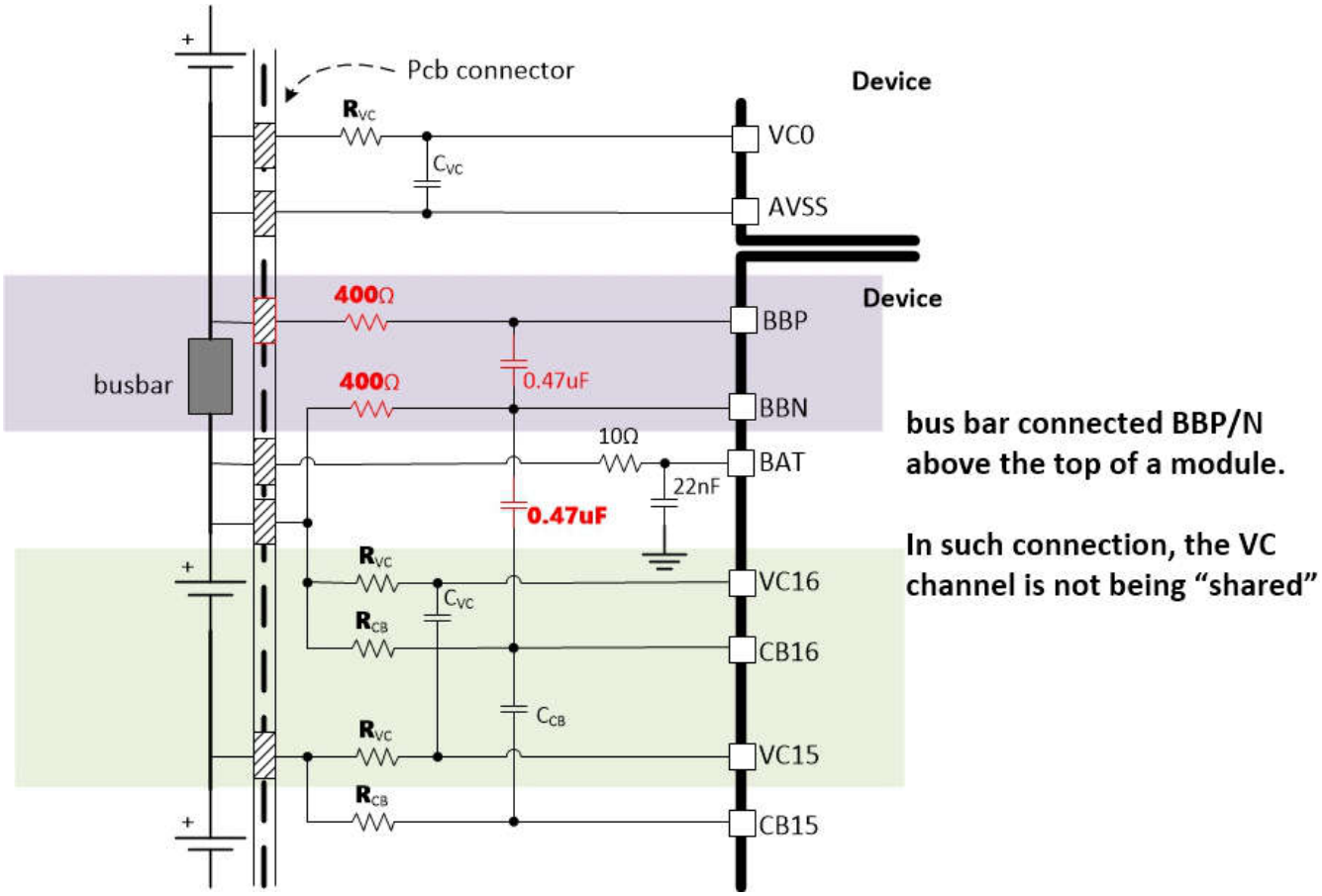
Note

New recommendation to add 470 nF/16 V from CB16 to BAT for hotplug robustness not shown in above figure, see data sheet for details.

Figure 5-3. BBP/N Connection With Bus Bar Connected in any Middle VC Channel

If the bus bar connected to BBP/N is placed at the top of a module (see Figure 5-4 connection), such connection is the exception in the BBP/N case that a cell channel is NOT being shared. In this connection, actual cell measurements are made through the VC channels and the host does not require performed addition calculation.

The connection in Figure 5-4 applies if the bus bar is connected to the top of the module, where in a single device, no cell is connected above the bus bar. To support hotplug on the bar channel, besides the 400-Ω filter resistor each on BBP/N pins and a 0.47-µF/16-V differential capacitor across BBP/N pins. If the bus bar is used above the top cell then also an additional 0.47-µF/16-V differential capacitor is needed to connect from BBN to the top CB pin. This additional capacitor forms a complete capacitor ladder from all the cells in the module to the bus bar, allowing high spike voltage during hotplug to distributor across the capacitor ladder.



Note

New recommendation to add 470 nF/16 V from CB16 to BAT for hotplug robustness not shown in figure, see data sheet for details.

Figure 5-4. BBP/N Connection With Bus Bar Connected Above Top of a Module

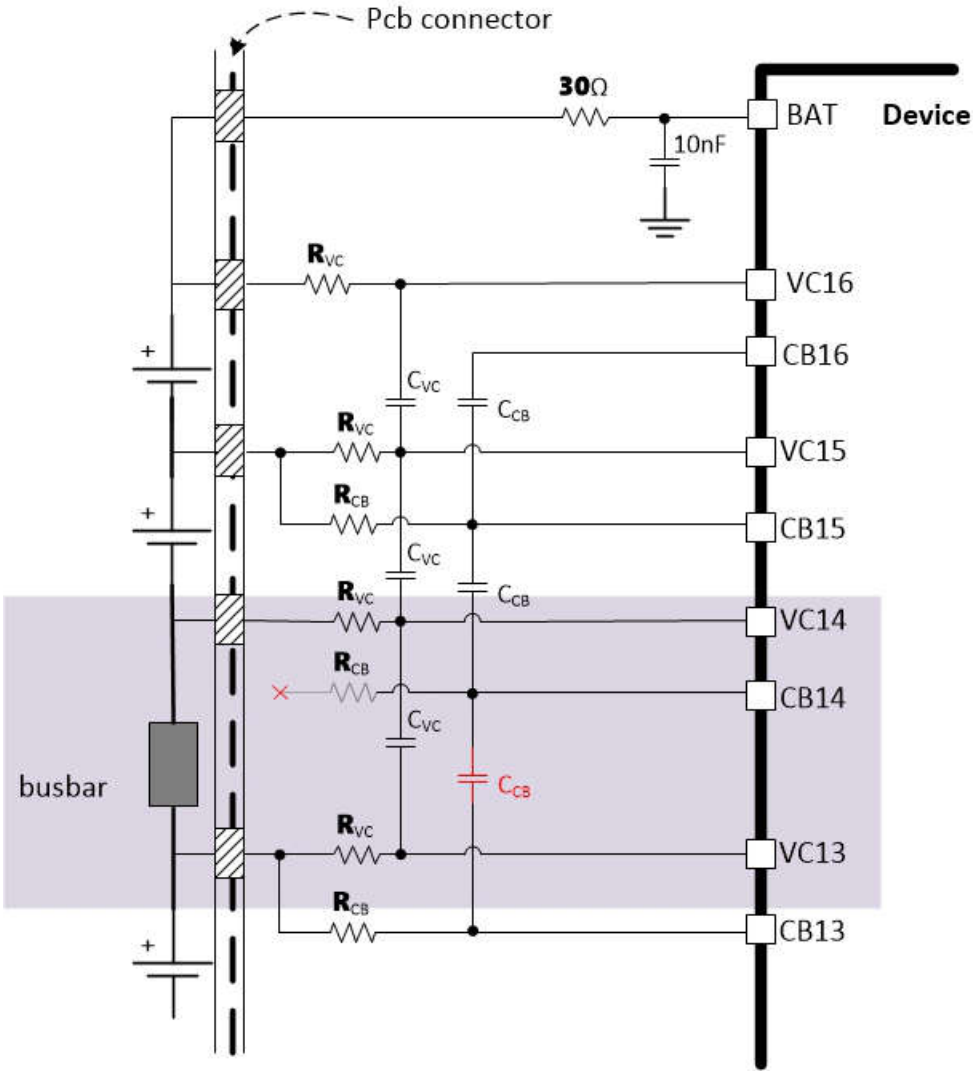
5.2.1 Cell Balancing Handling

Since the bus bar is shared with a cell to a cell channel, there is no special handling on the cell balancing control. The host shall be aware that additional IR error is introduced to the VCB_DONE detection (through VC channel) on the shared channel.

5.3 Bus Bar on Individual VC Channel

With the bus bar connected to a VC channel individually, the upper CB pin on that channel shall be left floating to avoid forward biasing the internal CBFET (see Figure 5-5 connection). This connection applies to the bus bar connecting to any middle VC channel individually. That is, in a single device, there is a cell connected above and below the VC channel with the bus bar connected.

To ensure hotplug performance, the CB channel where the bus bar is connected shall still have the differential capacitor C_{CB} in Figure 5-5 , even if the upper CB pin is floating. This capacitor forms a complete capacitor ladder from all the cells and the bus bar connected to the device, allowing high voltage spikes during hotplug to be distributed across the capacitor ladder.

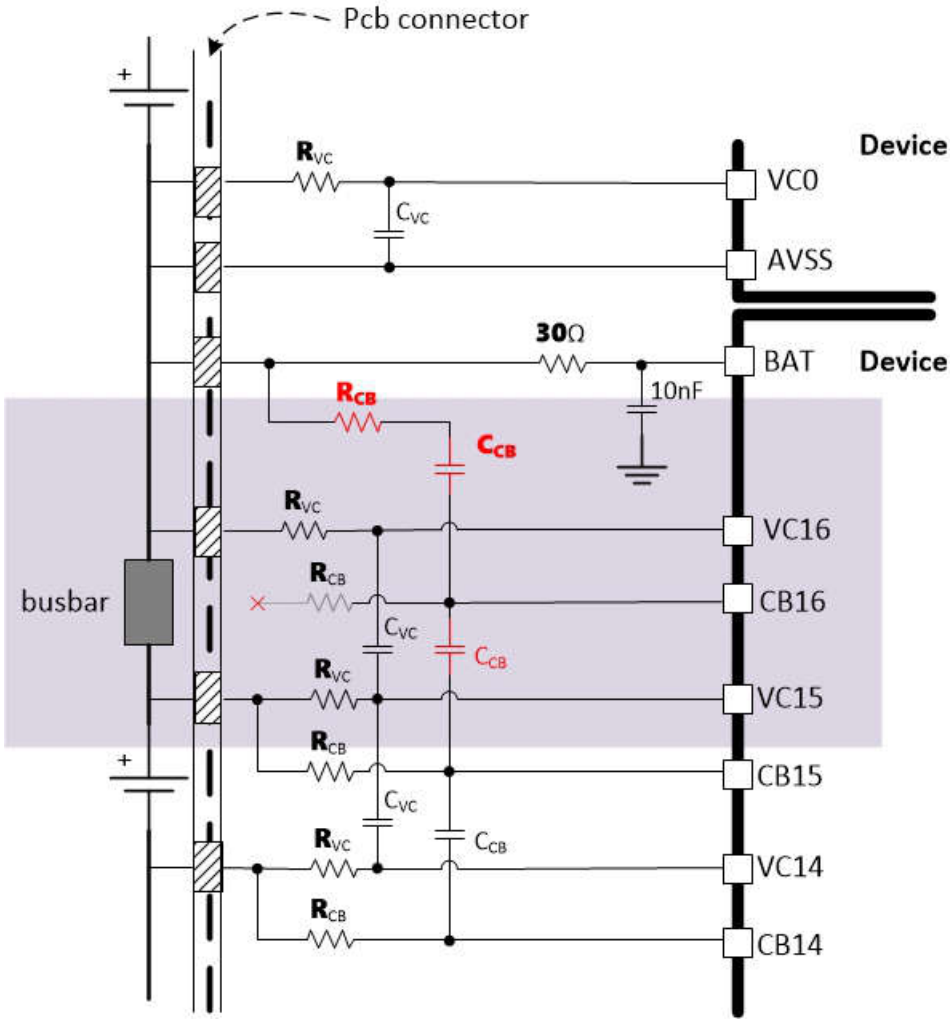


Note

New recommendation to add 470 nF/16 V from CB16 to BAT for hotplug robustness not shown in figure, see data sheet for details.

Figure 5-5. Bus Bar Connected any Middle Individual VC Channel

If the bus bar is connected to above the top of a module to an individual VC channel (see Figure 5-6 connection), the upper CB pin on that channel shall left floating, but the CB differential capacitor (C_{CB} in Figure 5-6) shall still be connected. Additionally, an RC filter shall be connected from the top CB pin to the BAT pin. This additional RC filter (using the same RC values as the other RC filters on the CB pins) is to ensure a complete capacitor ladder. It is used to distribute high voltage spikes with the same RC constant as the rest of the CB pins during a hotplug event.



Note

New recommendation to add 470 nF/16 V from CB16 to BAT for hotplug robustness not shown in figure, see data sheet for details.

Figure 5-6. Bus Bar Connected Individual VC Channel Above the Top of a Module

5.4 Multiple Bus Bar Connections

5.4.1 Two Bus Bar Connections to One Device

Two bus bars can be connected to VC channels individually as shown in Figure 5-7. The first bus bar is connected to the channel VC4-VC3. CB4 is floated for a cell balancing path. Likewise, the second bus bar is connected to the channel VC6 -VC7. CB7 is also floated. Each bus bar must be at least two channels apart.

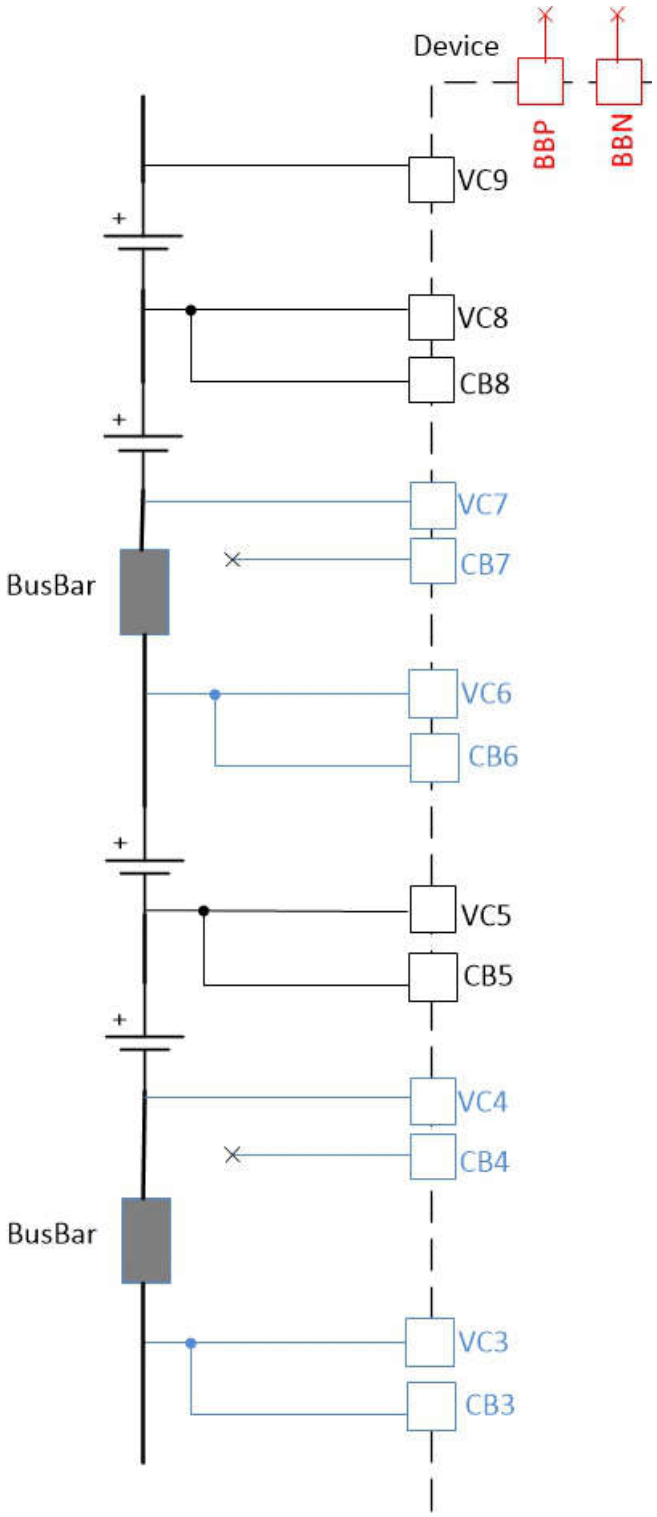


Figure 5-7. Two Bus Bars Connections Using Two Different VC Channel

5.4.2 Three Bus Bar Connections to One Device

A BQ79616-Q1 supports up to three bus bar connections to a single device. An additional bus bar can be connected to dedicated bus bar pins (BBP/N) while connecting two bus bars to each VC channel as described in Figure 5-8. The first and the third bus bars are connected to each channels, VC4-VC3, and VC7-VC6, respectively. The second bus bar is connected to the dedicated bus bar pins, BBP/N.

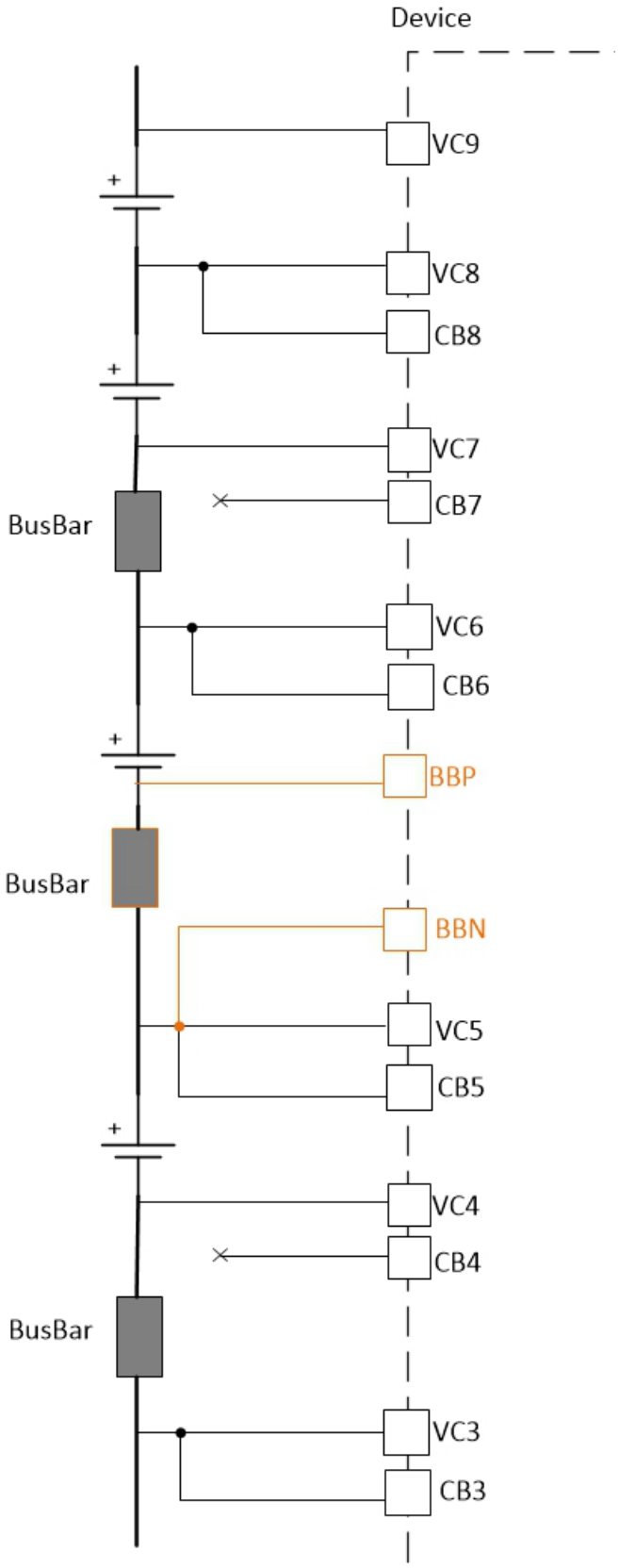


Figure 5-8. Multiple Bus Bar Connections Utilizing the BBP/N Pins

5.4.3 Cell Balancing Handling

When the bus bar is connected to the VC channel, the system must turn on two adjacent internal FETs to balance the cell above the bus bar as shown in Figure 5-9. The system must use manual balancing mode to turn on two adjacent FETs. Since two series CB FETs must be turned on to cell balance, the balancing current is slightly lower. See Equation 5 to calculate cell balancing current when the bus bar is connected to the VC channel.

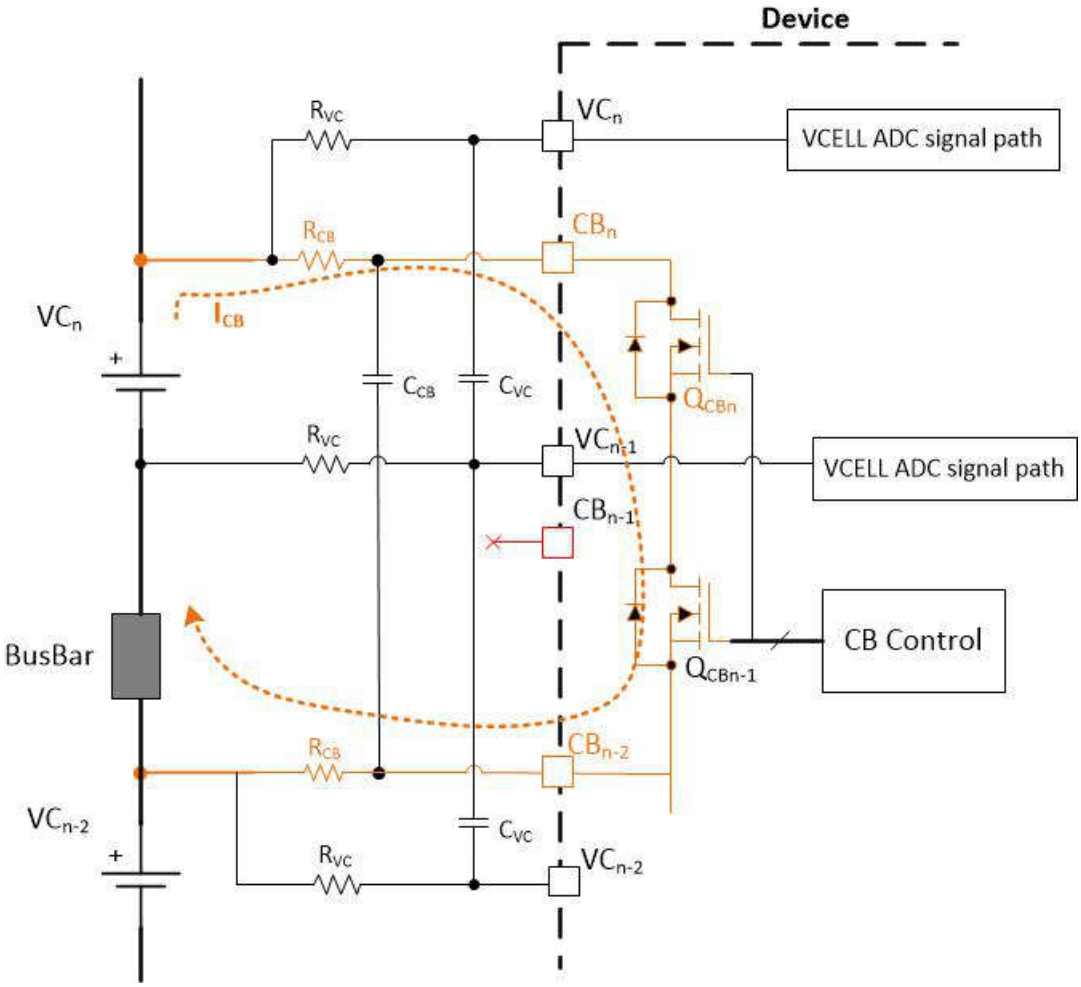


Figure 5-9. Internal CB Diagram With the Bus Bar Connection

$$I_{CB} = \frac{VCn}{(2 \times R_{CB}) + R_{DSon(QCBn)} + R_{DSon(QCBn-1)}} \quad (5)$$

6 TSREF

TSREF is a supply reference to bias external NTCs and should be bypassed to AVSS with a 1-µF/10-V capacitor. When thermistors are used for temperature measurements, connect TSREF to the top of the resistor divider network as described in Section 7.1. The BQ79616-Q1 supports ratiometric measurement through the main ADC. The intergrated OT, UT comparators have a wide range of programmable thresholds to support different R1 and R2 resistor ratios. TSREF should not be connected to other pins for power.

7 General Purpose Input-Output (GPIO) Configurations

There are eight GPIO pins available on BQ79616-Q1. These pins may be used for temperature measurement, measurement of DC analog signals, digital input or output, and SPI. The behavior of the pins may be selected in the non-volatile RAM as described in the data sheet. If the signal goes off the board, the input should be protected using a zener diode at the pin.

Unused GPIO pins should have an external 10-kΩ pulldown resistor to AVSS.

7.1 Ratiometric Temperature Measurement

Ratiometric voltage measurement is most commonly used for external temperature sensing. To measure an external temperature sensor, the GPIO connections must have a resistor divider from TSREF to AVSS with the GPIO connected to the center tap. The NTC can then be connected from TSREF to GPIO or from GPIO to AVSS. Optionally, the GPIO input could be filtered using a low-pass filter (C_{GPIO} and R_{GPIO}) to reduce high-frequency noise as shown Figure 7-1.

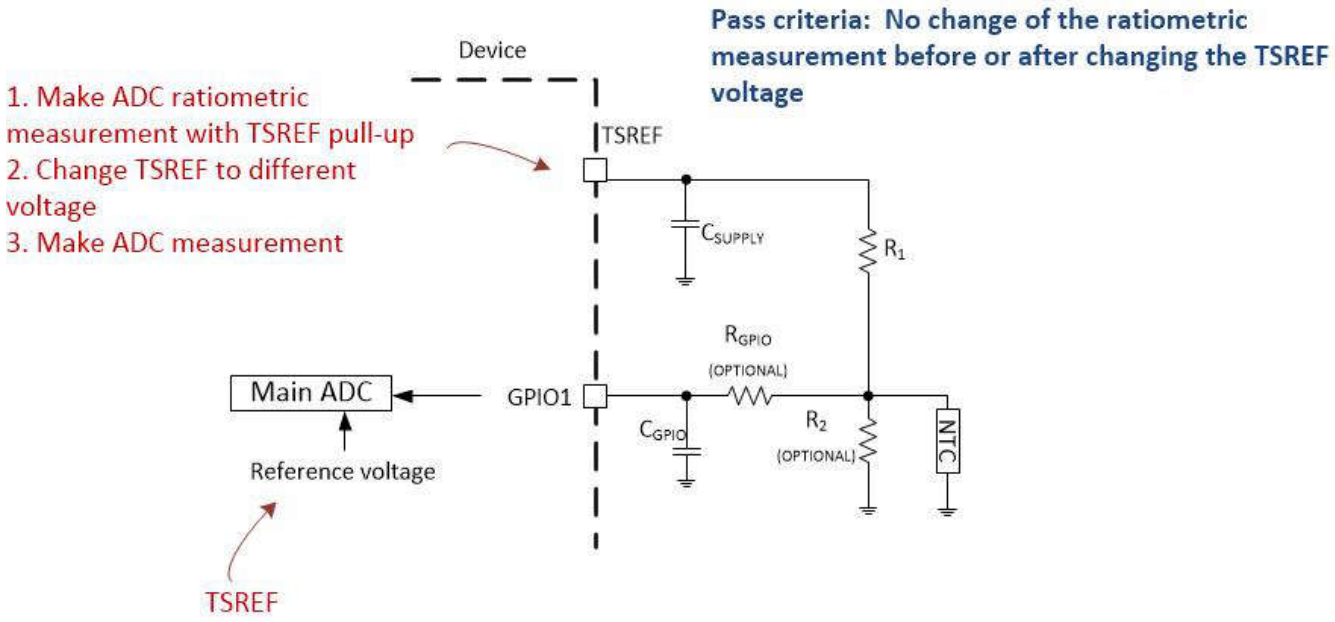


Figure 7-1. GPIO Ratiometric Measurement

The main ADC measures TSREF and GPIO voltages in its round robin. A microcontroller calculates the ratiometric voltage by Equation 6.

$$\frac{V_{GPIO}}{V_{TSREF}} = \frac{R_{NTC}}{R_{NTC} + R_1} \quad (6)$$

Temperature accuracy is affected by ADC measurement error and external component error. Using ratiometric measurement greatly reduces the ADC measurement error. Furthermore, the better the tolerance of the external circuit, the more accurate temperature sensing.

7.2 SPI Mode

One use of GPIO[7:4] is as a SPI master. Connection of the pins in SPI mode is the same as general digital connections, but SPI configuration replaces the GPIO pin configuration. Figure 7-2 shows an example connection of GPIO[7:4] for digital signaling or SPI mode.

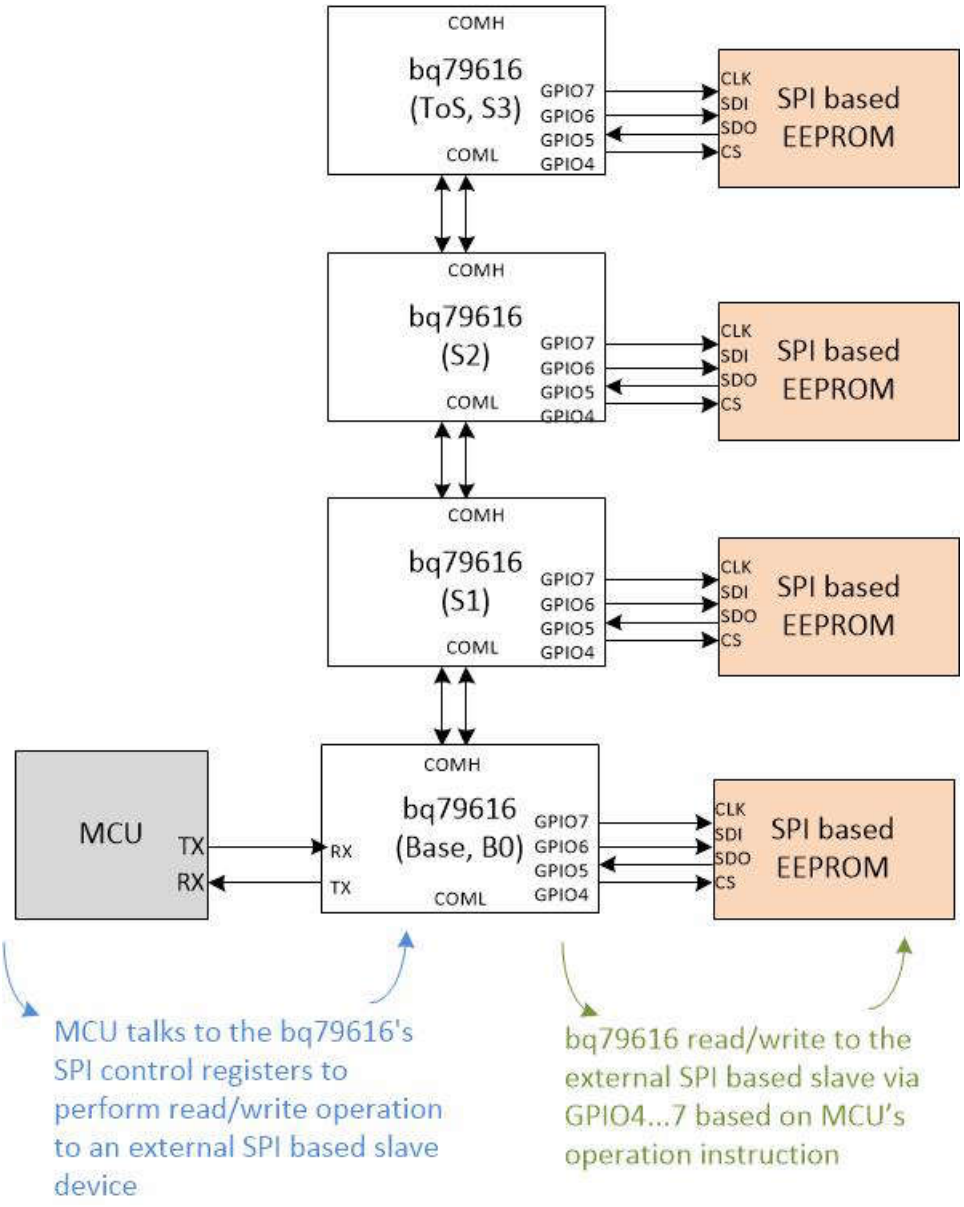


Figure 7-2. Example SPI Master Connections

Unused GPIO pins should be tied to AVSS through a 10-kΩ pulldown resistor. By default, the GPIO pins are configured internally as an input with a weak pulldown resistor, so program the GPIO configuration appropriately to avoid leakage current.

7.2.1 Support 8 NTC Thermistors With SPI Slave Device

A single 4-channel 2:1 switch can be use to switch between SPI and thermistor input. Single switches available at TI and can be powered from CVDD as shown in Figure 7-3.

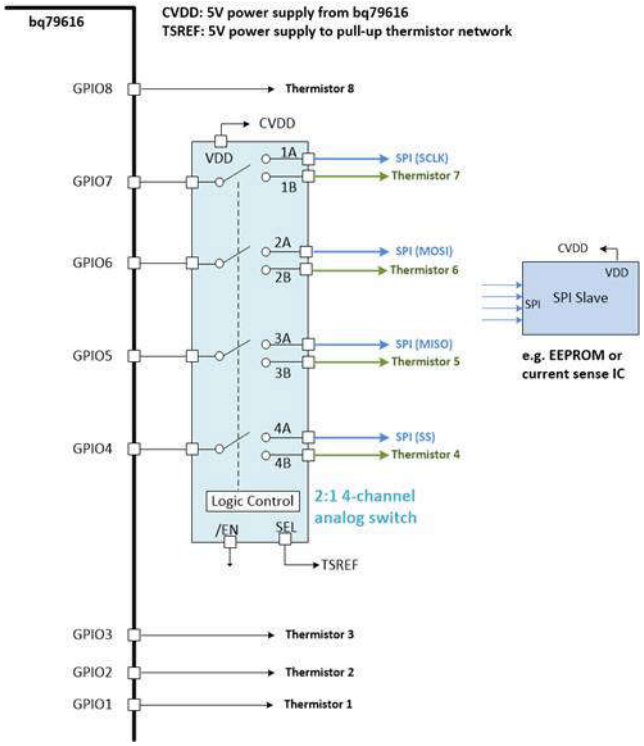


Figure 7-3. 8 NTC Thermistors With SPI Slave Device

Enabling TSREF selects the “B” paths of the switch, which are all connected to NTCs for temperature measurement. Disabling TSREF disables all the thermistor networks, and also selects the “A” paths of the switch to allow SPI communication. This configuration has no impact to the temperature measurement diagnostic and will still have ASIL-D compliance on the temperature measurement.

7.2.2 Design Summary

1. Connect external temperature sensor to GPIOs using a voltage divider network.
2. GPIO pins used for temperature measurement must have a pullup resistor to TSREF equivalent to the resistance of the NTC at nominal temperature. Each input must also have a 1-kΩ resistor and 1-µF capacitor.
3. GPIO pins with signals connecting from off-board must use a zener diode clamp.
4. DC voltage readings need a 1-kΩ resistor and 1-µF capacitor.
5. To use GPIOs in SPI mode, use GPIO4 - GPIO7. Unused GPIOs must be pulled low to GND.
6. GPIO pins are all programmed as inputs with a weak pulldown, leaving the inputs floating. The pins must not be allowed to remain as floating inputs. Reprogram the pins to become outputs or add a pulldown resistor.
7. The BQ79616-Q1 can support 8 NTC thermistors with SPI slave device using 4 channel 2:1 switch and this configuration has no impact to temperature measurement diagnostic.

8 Base and Bridge Device Configuration

Single ended communication lines with the BQ79616-Q1 normally refers to the base device in a stack that communicates with the host microcontroller through SPI and UART (SPI only available using BQ79600-Q1). There are two main ways to configure the base device. The first is using the BQ79600-Q1 as a bridge device as shown in Figure 8-1 and the second utilizes an isolation circuit with the base device as described in Figure 8-2. This document will introduce using BQ79616-Q1 as a base device. Refer to the BQ79600-Q1 data sheet and design considerations to use communication extender, bridge device. An overview of how a bridge device should be configured is shown in Figure 8-1.

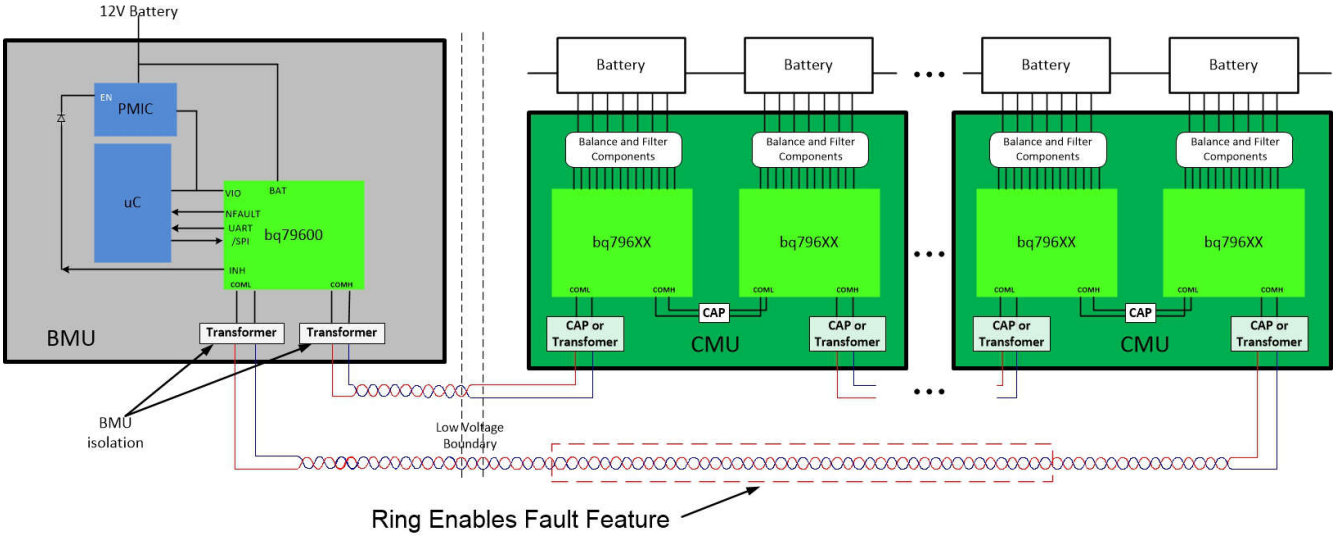


Figure 8-1. Communication With the Bridge Device BQ79600-Q1

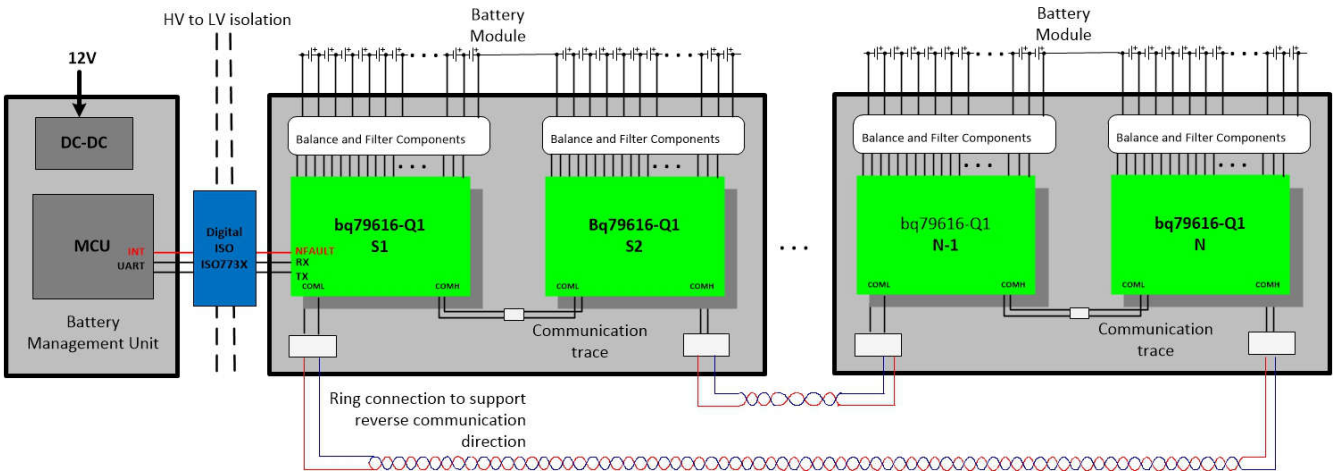


Figure 8-2. Using BQ79616-Q1 as Base Device with Isolation Circuit

8.1 Power Mode Pings and Tones

8.1.1 Power Mode Pings

A ping is a specific high-low-high signal sent from MCU to the base device through the RX pin. Pings are used on the base device as only the base device is connected to the host from which the UART RX is accessible. The device detects the low pulse duration of the ping to differentiate between the different pings. There are total of 4 different pings as shown in Figure 8-3.

- a WAKE ping through RX pin
- a SHUTDOWN ping through RX pin
- a SLEEPtoACTIVE ping through RX pin
- a HW_RESET ping through RX pin

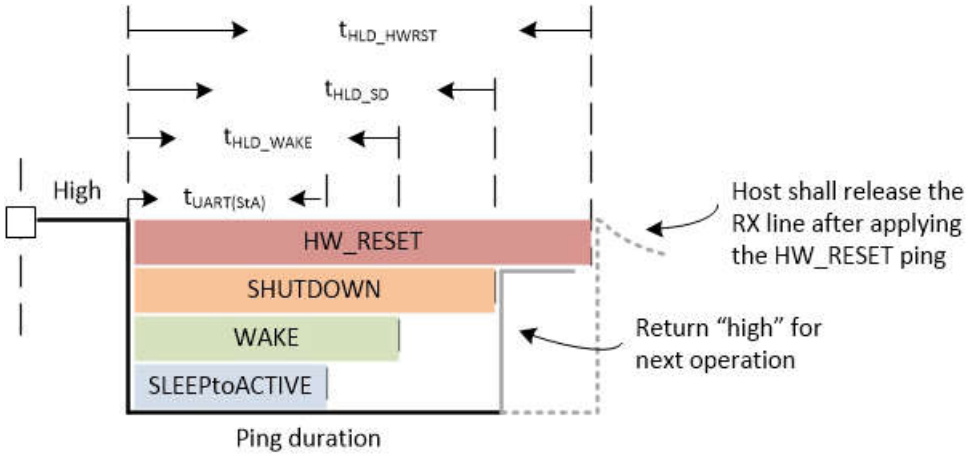


Figure 8-3. Communication Pings

8.1.2 Power Mode Tones

Stack devices are woken up by tones. A tone is a set number of specific couplets sent through the differential communication lines COMH and COML. When a device wakes up by a tone, it is not a base device but must be a stack device. The device will configure the COMH and COML port based on stack or base detection accordingly. There is a total of 4 different power modes related to tones as seen in Figure 8-4. In addition, there are two extra tones related to FAULT. See Device Fault Summary, Fault Tone, and Heartbeat sections in the BQ79616-Q1 data sheet for details.

- a WAKE tone through COMH/L
- a SLEEPtoACTIVE tone through COMH/L
- a SHUTDOWN tone through COMH/L
- a HW_RESET tone through COMH/L

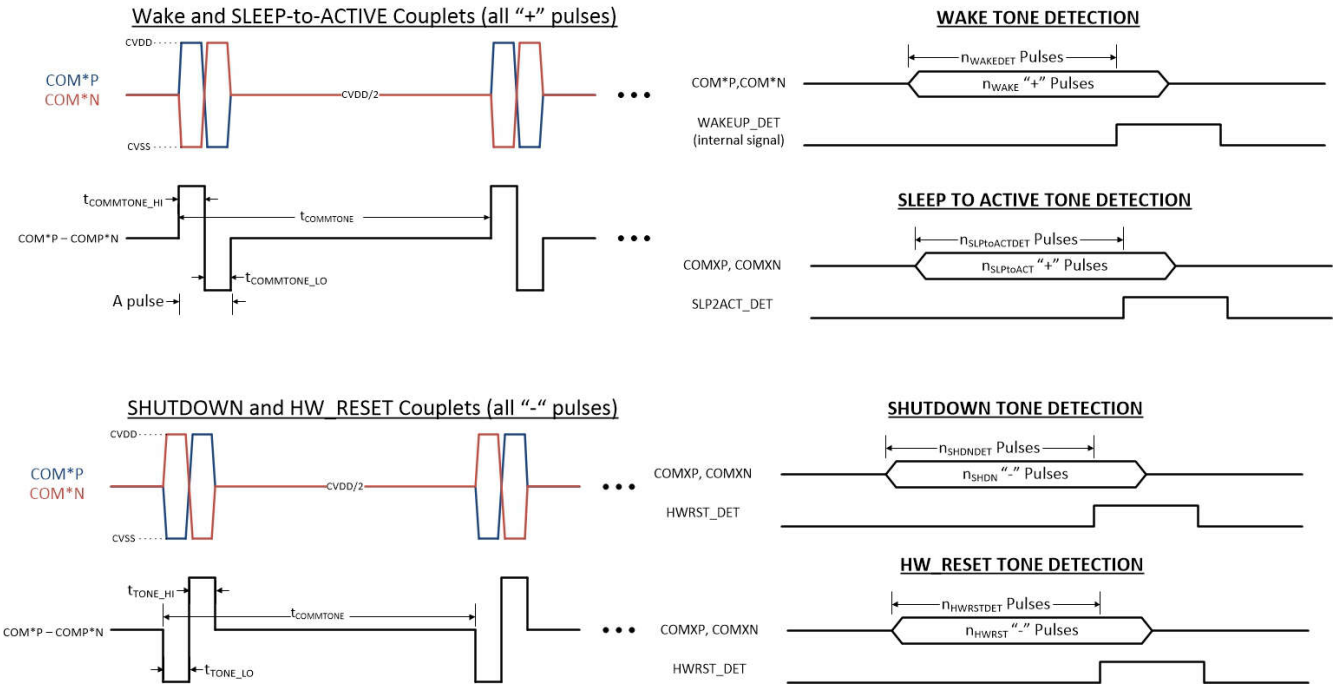


Figure 8-4. Communication Tones

8.1.3 Ping and Tone Propagation

During normal operation, host can simply send a WAKE or SLEEPtoACTIVE ping to the base device and the corresponding tone will be generated to the rest of the stack devices as seen in Figure 8-5. During system development, if there is a need to send WAKE or SLEEPtoACTIVE to only some of the devices in the daisy chain, host can use the CONTROL1[SEND_WAKE] or CONTROL1[SEND_SLPTOACT] bits. The SHUTDOWN and HW_RESET ping or tone are mostly used as a communication recovery attempt. Hence these pings/tones are non-propagable.

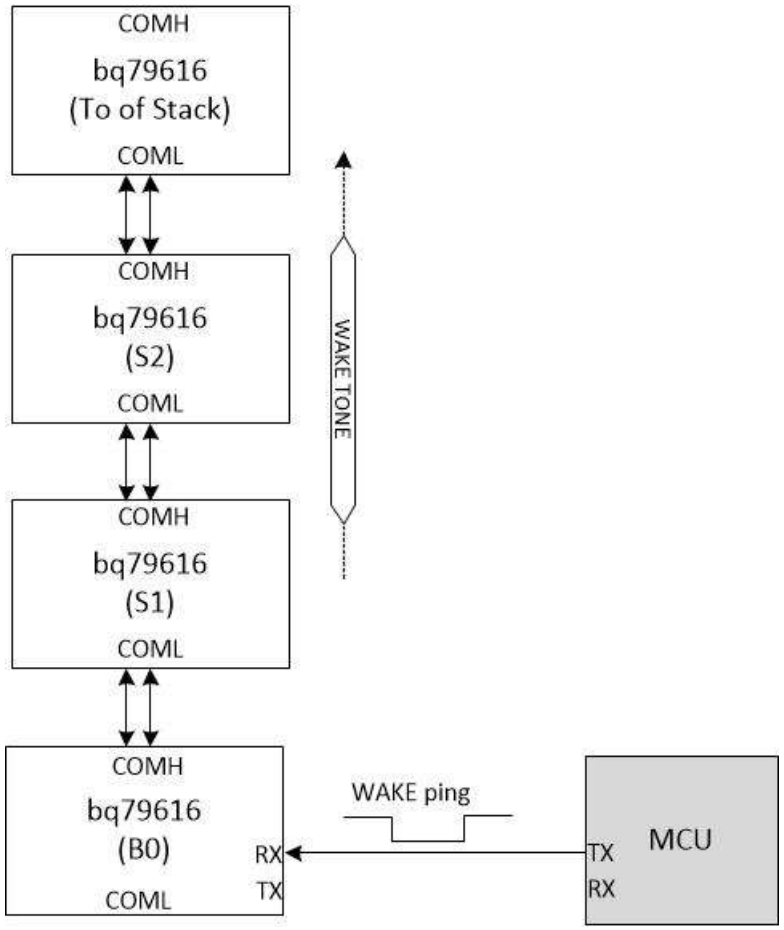


Figure 8-5. Diagram for Ping/Tone Propagation

8.2 UART Physical Layer

The device can operation as a standalone device such as in a multidrop configuration (DEV_CONF[MULTIDROP_EN] = 1) or as a base/stack device in a daisy chain configuration (DEV_CONF[MULTIDROP_EN] = 0). In multidrop configuration, the daisy chain communication is disabled and the host communicates only with a single device through the UART interface. This chapter will introduce UART interface configuration focusing on daisy chain communication.

The UART sends data on the TX pin and receives data on the RX pin. When idle, the TX and RX are high. The UART interface requires that RX is pulled up to CVDD through a 100-kΩ resistor on the base device. The RX shall be pulled up on the BQ79616 side. Do not leave RX unconnected. Ensure RX is connected directly to CVDD for stack devices.

TX is disabled in stack devices, but must be pulled high through a 100-kΩ resistor on the host side on the base device to prevent triggering an invalid communication frame when the communication cable is not attached, or during power-off or SHUTDOWN state when TX is high impedance. TX is always pulled to CVDD internally while in ACTIVE or SLEEP mode, whether enabled or disabled. Leave TX unconnected if not used in stack devices. NFAULT is an active low fault indicator that, in the event of a fault, will pull low to signal to the host that a fault

has occurred. Due to this fact the NFAULT pin should have a 100-kΩ pullup resistor to CVDD. If the device is a stack device then NFAULT can be left unconnected.

Refer to Table 8-1 for information on base device communication using a digital isolator.

Table 8-1. UART Physical Layer Check List

List	Pin	Base Device	Stacked Devices	Top of Stack Device
1	RX	100 kΩ pullup to CVDD, 51 pF to GND	CVDD	CVDD
2	TX	100 kΩ pullup on Host side	Float	Float
3	COMML+	COMMH+ of Top of Stack	COMMH+ of lower device	COMMH+ of lower device
4	COMML–	COMMH+ of Top of Stack	COMMH– of lower device	COMMH– of lower device
5	COMMH+	COMML+ of upper device	COMML+ of upper device	COMML+ of Base Device
6	COMMH–	COMML– of upper device	COMML– of upper device	COMML- of Base Device
7	NFAULT	100 kΩ pullup to CVDD	Float	Float

8.2.1 Design Considerations

- For the base device, provide a 100-kΩ pullup resistor for RX and NFAULT to CVDD and RX on the host side.
- For stacked devices leave NFAULT and TX floating
- For stacked devices tie RX to CVDD
- When BQ79600-Q1 is used as a bridge device, also pull up RX and TX with a 100-kΩ resistor, and NFAULT with a 100-kΩ resistor to CVDD.

9 Daisy-Chain Stack Configuration

In the stacked configuration, the main microcontroller first communicates through a BQ79616-Q1 base device using the UART communications interface. Communication is then relayed up the chain of connected slave BQ79616-Q1 devices using a proprietary differential communications protocol over AC-coupled differential links interconnected by the COMMH± and COMML± pins. A high level diagram of this can be seen in Figure 9-1.

In the case of BQ79616 -Q1 working with a BQ79600-Q1 communication extender, the host microcontroller first communicates through a bridge device by UART or SPI. A command is then moved up the chain of connected slave BQ79616-Q1 devices through COML and COMH pins vertically as described in Figure 9-2.

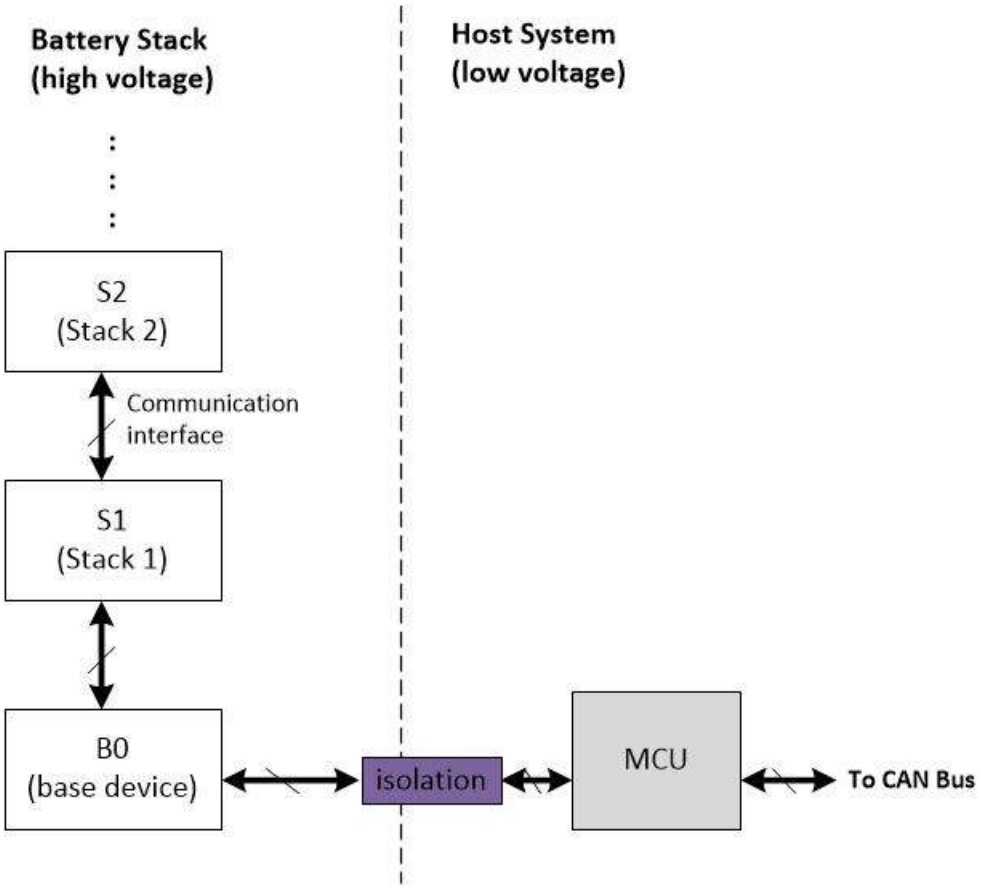


Figure 9-1. Daisy Chain Structure With a Base Device

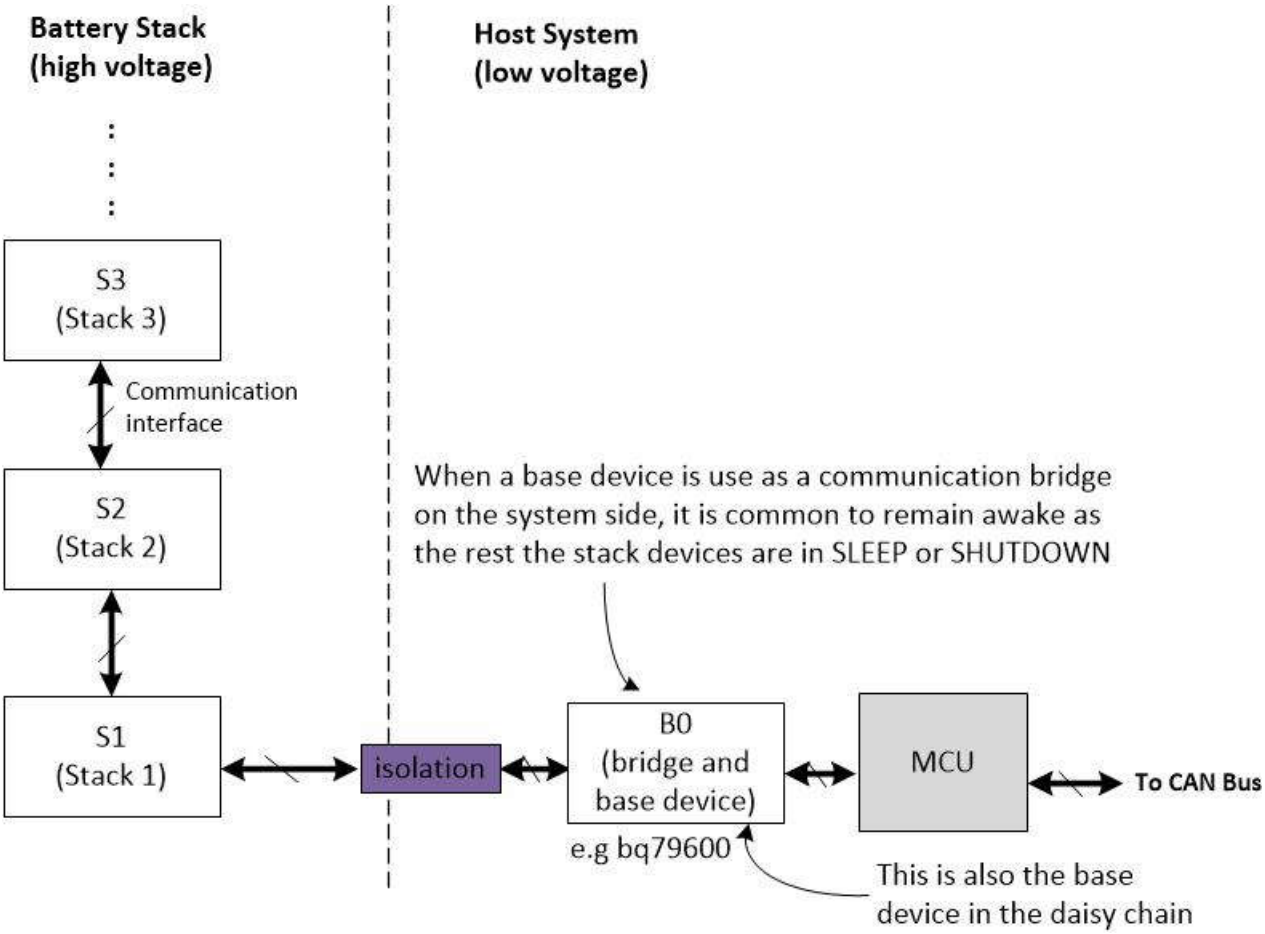


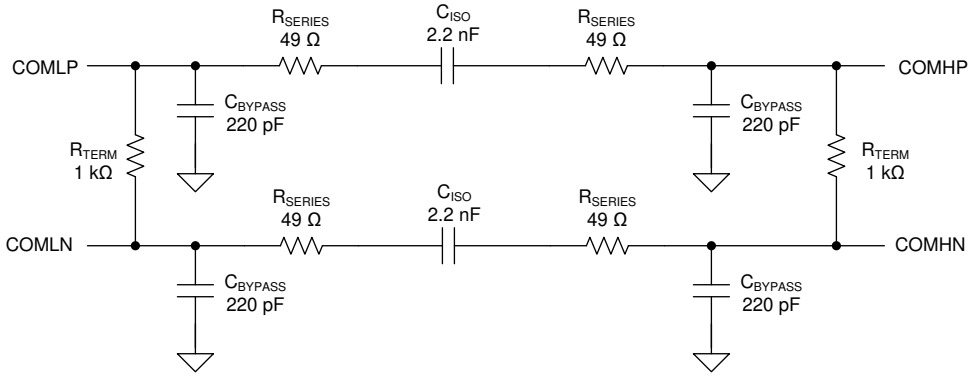
Figure 9-2. Daisy Chain Structure With a Bridge Device

9.1 Communication Line Isolation

Many applications require multiple, daisy-chained BQ79616-Q1 devices that are separated by cables or located on the same PCB. The cables can introduce additional challenges and additional components are needed for noisy environments. There are 3 different solutions to this noise problem: capacitor only isolation, capacitor and choke isolation, and transformer isolation. Each of these solutions will be discussed in the following sections.

9.1.1 Capacitor Only Isolation

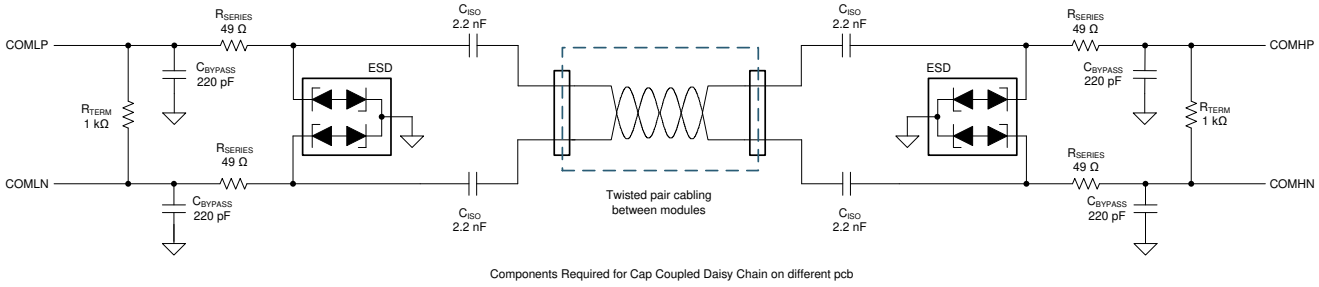
The first solution, capacitor isolation, is best suited for reducing noise and providing voltage isolation for ICs that are located on the same PCB. Figure 9-3 shows how this configuration would look for two ICs connected on the same PCB. A 10-kΩ termination resistor must be added at the high and low sides. In addition a 49-Ω resistor and 220-pF capacitor must be added on each line on both the high and low side to proved additional filtering. The capacitor must be 2.2 nF with a voltage rating twice that of the local cell stack. For example, for a 400-V system, a 800-V capacitor is needed. This configuration must be done on both the COMM± lines.



Components Required for Cap Coupled Daisy Chain on the same PCB

Figure 9-3. Components Required for Cap Coupled Daisy Chain in the Same PCB

Figure 9-4 shows capacitive coupling isolation between two separated PCB. The capacitor needs to be 2.2 nF with a voltage range twice that of the local cell stack. One capacitor is sufficient, but if additional safety is needed then two can be used, one at each end of the cable. In this case a 220-pF capacitor must be used. Capacitance has a direct effect on performance, so all intended and parasitic capacitance must be taken into account when choosing components.

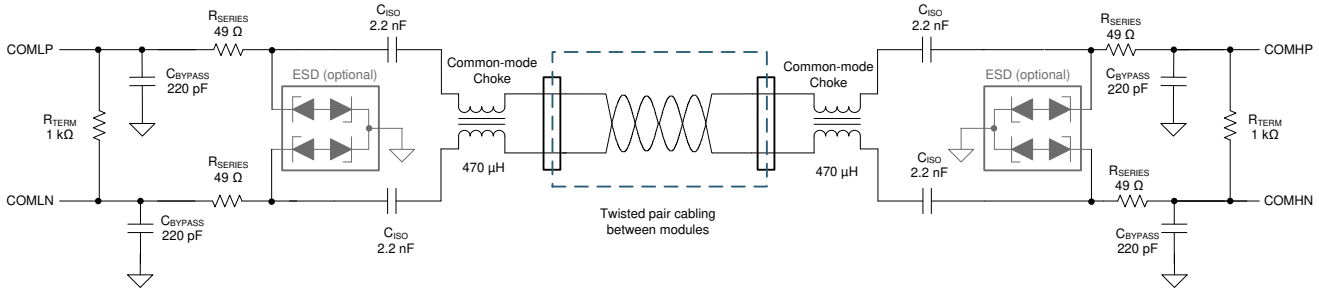


Components Required for Cap Coupled Daisy Chain on different pcb

Figure 9-4. Components Required for Cap Coupled Daisy Chain in Different PCB

9.1.2 Capacitor and Choke Isolation

If the cable length is greater than 2 m, the recommendation is that the capacitor only isolation be implemented. Instead a common mode choke must be added. A single or dual choke can be used. In the dual common-mode filter, a 100 µH and 470 µH must be used. In a single filter mode then the line must have TDK 51-µH 2.8-kΩ choke (part number ACT45B-510-2P-TL003).



Components Required for cap-choke Daisy Chain with Cabling

Figure 9-5. Components Required for Cap-Choke Daisy Chain With Cabling

9.1.3 Transformer Isolation

Transformer isolation is the most effective method for removing common mode noise from the system. The two options for this implementation can be seen in Figure 9-6. The following parameters are recommended for the transformer selection:

- Inductance = 150-600 µH
- Isolation Voltage = 2500 V, AC

The HMU1228 transformer is recommended and is recommended to be center tapped with a 100-pF capacitor. PESD2CAN can be added optionally for ESD protection.

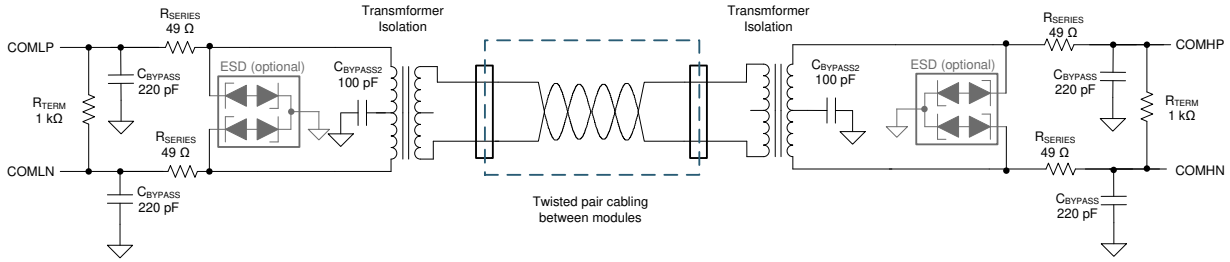


Figure 9-6. Components Required for Transformer Coupled Daisy Chain

Regardless of which isolation method is chosen, there are a few things that are common among all of them. First is the 220-pF capacitor and 49-Ω resistor before the ESD isolation on both the high and low side on both the positive and negative lines.

Lastly, each design has a termination resistor. The purpose of this resistor is to prevent reflected signals from interfering in the communication. The recommendation is that a 1 kΩ be used.

In all of these situations, the recommendation is based off how long the cable between boards is, and in all cases, twisted pair cabling is used between modules. The main purpose of these noise isolation methods is to remove common mode noise from the signal. More details can be found in Section 15.

The recommendation is that with any design that is chosen, that additional ESD protection is added. The PESD2CAN is shown in the following sections to provide ESD isolation on the communication lines.

9.1.4 Design Summary

- For devices located on the same PCB there must be a 2.2-nF isolation capacitor on each COMM± line with a voltage rating twice that of the cell stack.
- In addition to the isolation method there must be a termination resistor at each end of the connection for devices located on the same PCB and for between PCBs.
- There are three types of noise isolation methods that can be employed when communicating through a cable:
  1. Capacitor Only Isolation
     a. Only recommended for cables less than 2 m
  2. Capacitor and Choke Isolation
     a. Cables longer than 2 m
     b. Part number: ACT45B-510-2P-TL003 for single mode choke
  3. Transformer Isolation
     a. HMU1228 and HM2147 transformer is recommended
- PESD2CAN is recommended between communication lines to add ESD isolation
- *Any* capacitance present on the communication line can have an effect on the performance. All intentional and parasitic capacitance must be calculated and taken into effect.

9.2 Ring Communication

The daisy chain communication for the device allows for the use of a *ring* architecture. In this architecture, a cable break between two devices does not prevent communication to all upstream devices as in a normal non-ring scheme. When the host detects a broken communication interface, the device allows the host to switch the communication direction to communicate with devices on both sides of the break. This allows for safe operation until the break in the lines is repaired.

The *CONTROL1[DIR_SEL]* controls the communication direction. The devices will reconfigure the COMH and COML ports depends on the *[DIR_SEL]* and the *[TOP_STACK]* setting. The auto addressing procedure is needed to re-address the device addresses for the reverse communication direction.

Following is an example on how to change the communication direction to *[DIR_SEL] = 1* to the entire daisy chain.

1. Host clears the previous *Top of Stack* device
   - In this step, the previous TOS device will re-enable its COMH.
2. Host sends single device write to change the base device *[DIR_SEL] = 1* (see figure (a) in Figure 9-7)
   - The base device will disable its COMH and enable its COML
3. Host sends broadcast write reverse direction to change the rest of the devices' *[DIR_SEL] = 1* (see figure (b) in Figure 9-7)
   - In this step, the entire daisy chain is set up to communicate in the [DIR_SEL] = 1 direction (i.e. each device set up to transmit command frames sent by host from its COMH to its COML)
4. Host performs auto addressing procedure to set up device address in the DIR1_ADDR register (see figure (c) in Figure 9-7)
   - Unless the devices have been reset, host can skip the dummy read/write steps to synchronize the DLL in the auto addressing procedure
5. Host sets up the new *Top of Stack* device (see figure (c) in Figure 9-7)
   - In this step, the new ToS device disables the COML transmitter

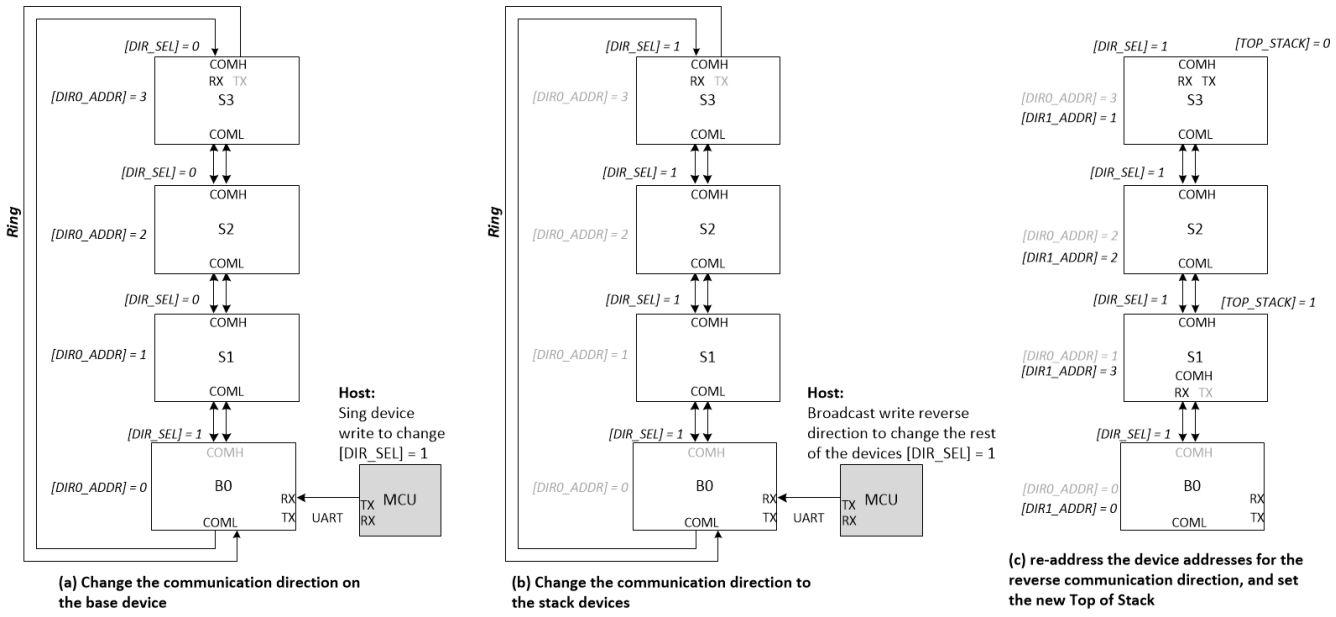


Figure 9-7. Example of Changing Communication Direction in Daisy Chain

Ring architecture also enables fault status transmitting in sleep. In SLEEP mode, the following fault detections are still active.

- Customer and Factory OTP shadowed registers CRC check
- Device thermal warning
- Power supplies OV, UV, oscillation detection
- If OVUV protectors are enabled, cell OV and UV detection

- If OTUT protectors are enabled, thermistors OT and UT detection

Since communication is not available in SLEEP, the device provides an option to transmit the fault status through Heartbeat (device in no fault state) and Fault Tone (device in fault state). These tones are transmitted in the same direction as a communication command frame, which is based on the CONTROL1[DIR_SEL] setting. In order for the tone signal to return back to the base device (so NFAULT can be triggered if needed), a ring architecture must be used in order to support transmitting the fault status in SLEEP mode.

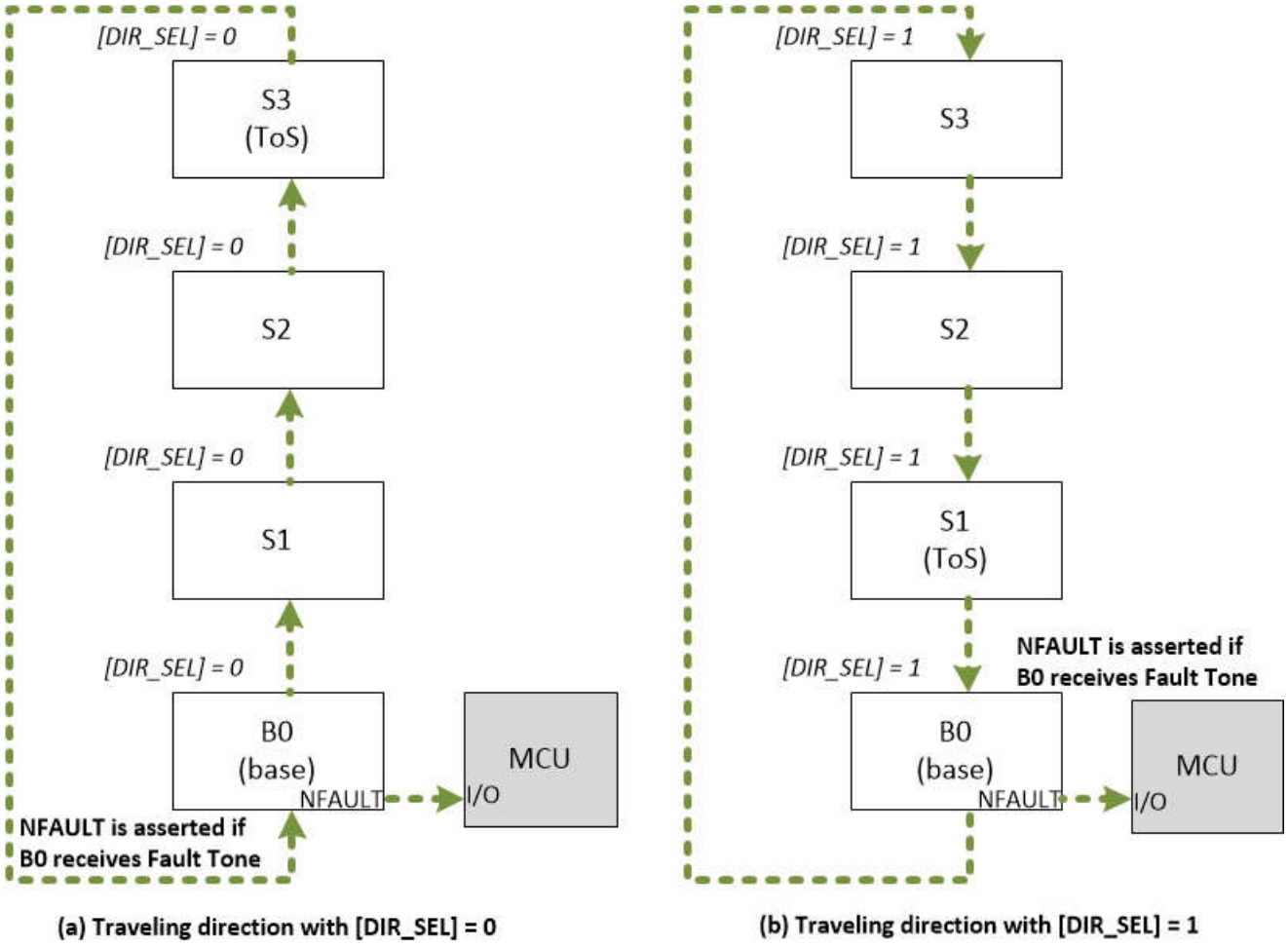


Figure 9-8. Heartbeat or Fault Tone Traveling Direction

9.3 Re-Clocking

The BQ7916-Q1 regenerates each communication signal before BQ7916-Q1 sends the signal on to the next device. This feature is to prevent compression of a signal as it moves up the stack. Re-clocking generates the ideal waveform but also adds about 4 µs of delay.

Figure 9-9 shows images from an experiment in which 18 BQ79606-Q1 EVMs were daisy chained together to observe the bit compression. As it can be seen there is almost no difference in the bit-width between the base and top of stack board. This is due to the re-clocking feature. Re-clocking allows for a longer daisy chain cable between board and also increased the number of stack-able devices in the system.

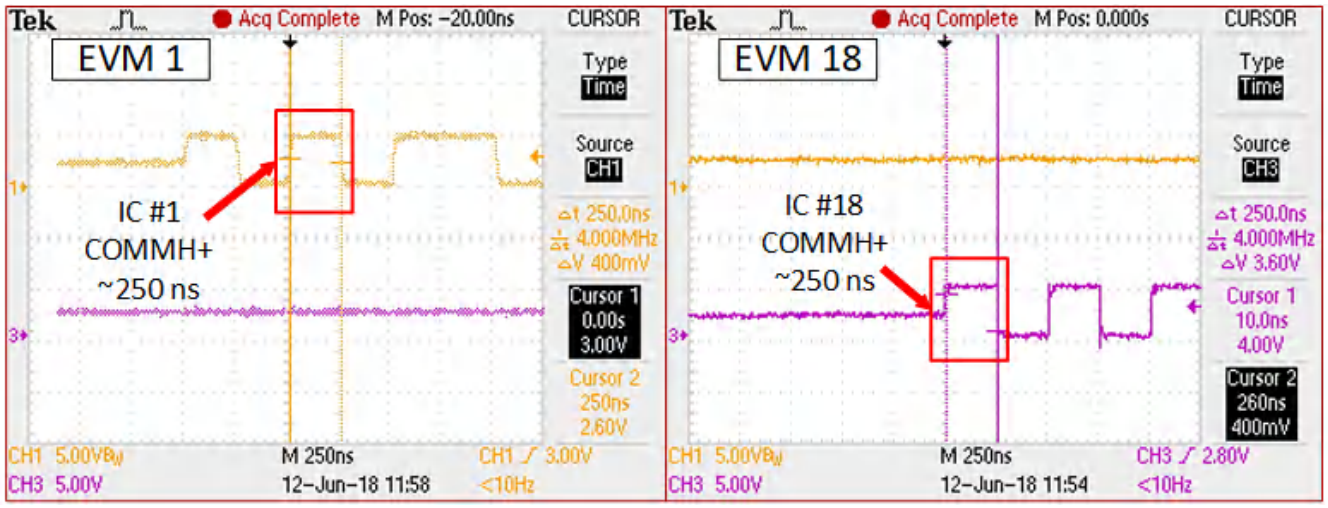


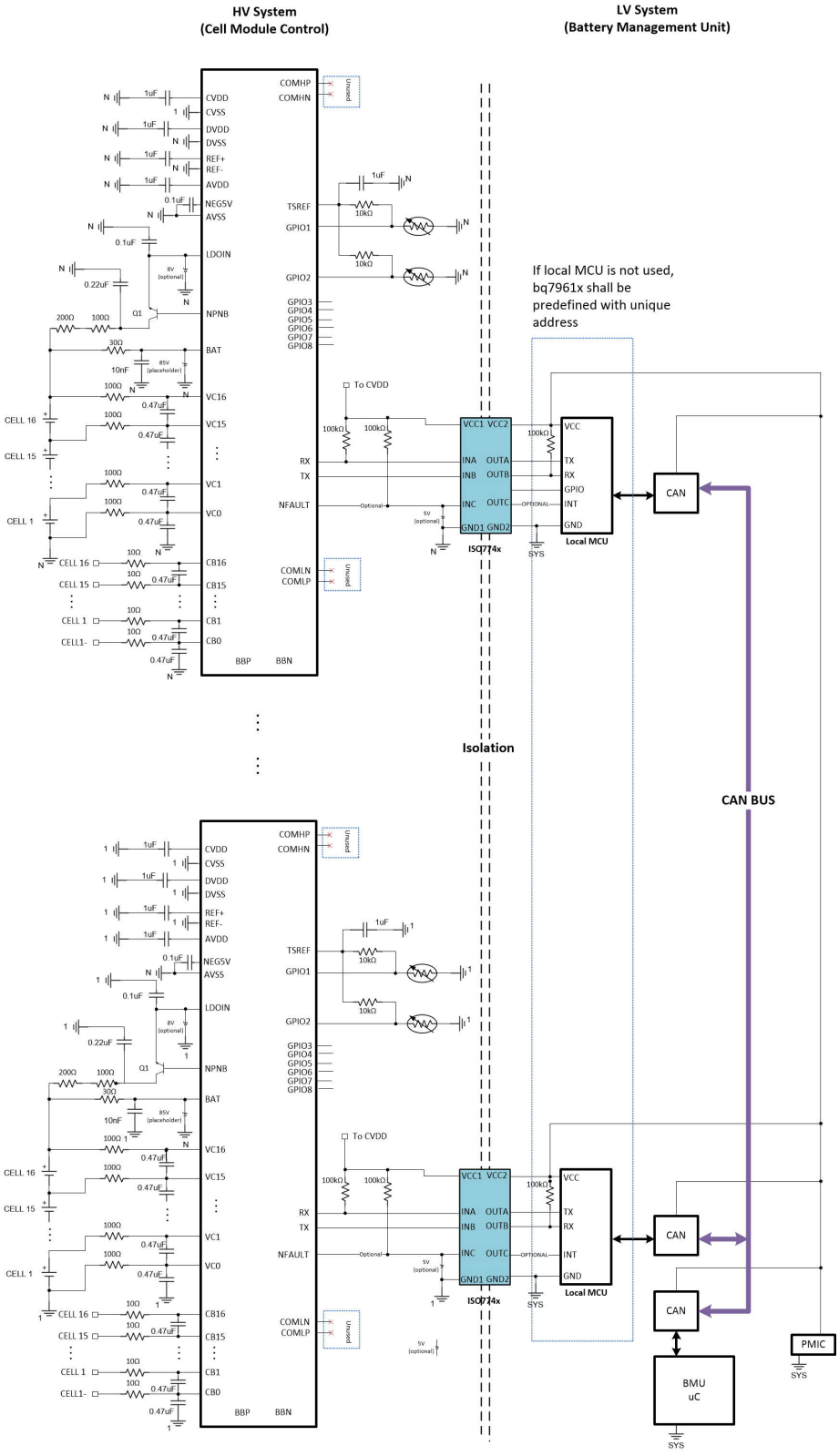
Figure 9-9. Re-Clocking Bit Compression Example

9.3.1 Design Summary

- Ring architecture allows for the host to continue communication to all devices in the event of a break.
- Re-clocking the communication signals preserves the signal integrity but adds delay into the design.

10 Multi-Drop Configuration

An alternative to the daisy-chain configuration is multi-drop. Here all of the BQ79616-Q1 devices are seen as base devices and connected in parallel. This configuration does not support auto-addressing. Figure 10-1 shows a high level representation of this set up. For more information, refer to the BQ79616-Q1 data sheet.



Note

New recommendation to add 470 nF/16 V from CB16 to BAT for hotplug robustness not shown in above figure, see data sheet for details.

Figure 10-1. Multi-Drop Configuration

11 Main ADC Digital LPF

Each differential VC channel measurement is equipped with a post-ADC LPF. The LPFs have much lower cutoff frequency (f_{cutoff}). There are 7 f_{cutoff} options: 6.5 Hz, 13 Hz, 26 Hz, 53 Hz, 111 Hz, 240 Hz, and 600 Hz, configurable through the *ADC_CONF1[LPF_VCELL2:0]* setting. Once an f_{cutoff} value is selected and the LPFs are enabled by setting *ADC_CTRL1[LPF_VCELL_EN] = 1*, the same f_{cutoff} setting applies to all VC channel measurements. Configure the post ADC low-pass filter cut-off frequency for VCELL measurement as shown in Table 11-1.

The differential BBP and BBN measurement also has its own digital LPF, enabled by the *ADC_CTRL1[LPF_BB_EN]* bit. The LPF for the BB channel has the same seven f_{cutoff} options as for the VC measurements. Since the signal across the bus bar may be noisier than the VC measurement and may need a different f_{cutoff} setting than the VC channel, the device provides a separate LPF configuration parameter, *ADC_CONF1[LPF_BB2:0]*, for the BB channel, allowing the host to set a different f_{cutoff} for the BB and VC measurements. Configure the post ADC low-pass filter cut-off frequency for bus bar measurement by refering to Table 11-1.

Table 11-1. Main ADC LPF f_{cutoff} for VCELL and Bus Bar Measurement

ADC_CONF1[LPF_VCELL 2:0], ADC_CONF1[LPF_BB 2:0]	Cut-Off Frequency	Settling Time
0x0	6.5 Hz	154ms
0x1	13 Hz	77ms
0x2	26 Hz	38ms
0x3	53 Hz	19ms
0x4	111 Hz	9ms
0x5	240 Hz	4ms
0x6	600 Hz	1.6ms
0x7	240 Hz	4ms

12 AUX Anti Aliasing Filter (AAF)

The AUX ADC path serves as a redundancy path to the main ADC measurement on cell voltage measurements and the bus bar measurement. It also has the front end filters of a BCI filter and an AAF filter in the AUX ADC path. However, unlike the main ADC path with an individual front end filter for each channel, the cell voltages (taken from the CB0 to CB16 pins) and bus bar (taken from BBP and BBN pins) inputs in the AUX path are multiplexed to share the same BCI filter and AAF filter.

Because the front end filters are shared, the device has to wait for the AAF filter to settle before making any valid CB channel or BB channel measurement. The default AAF f_{cutoff} is 1.3 kHz as in the main ADC path, which translates to additional 4-ms settling time to complete a single CB or BB channel measurement. As this AUX path is intended for diagnostic use as an option for the MCU to reduce the diagnostic time, the device provides four AAF settling time options seen in the Table 12-1. The settling time is configured by the ADC_CONF1[AUX_SETTLE1:0] bits. Configure the AUX CELL settling time as listed in Table 12-1. If a longer settling time is allowed, the measurement will be more accurate.

Table 12-1. AAF Settling Time

ADC_CONF1[AUX_SETTLE 1:0]	Settling Time
00	4.3 ms
01	2.3 ms
10	1.3 ms
11	300 µs

13 Layout Guidelines

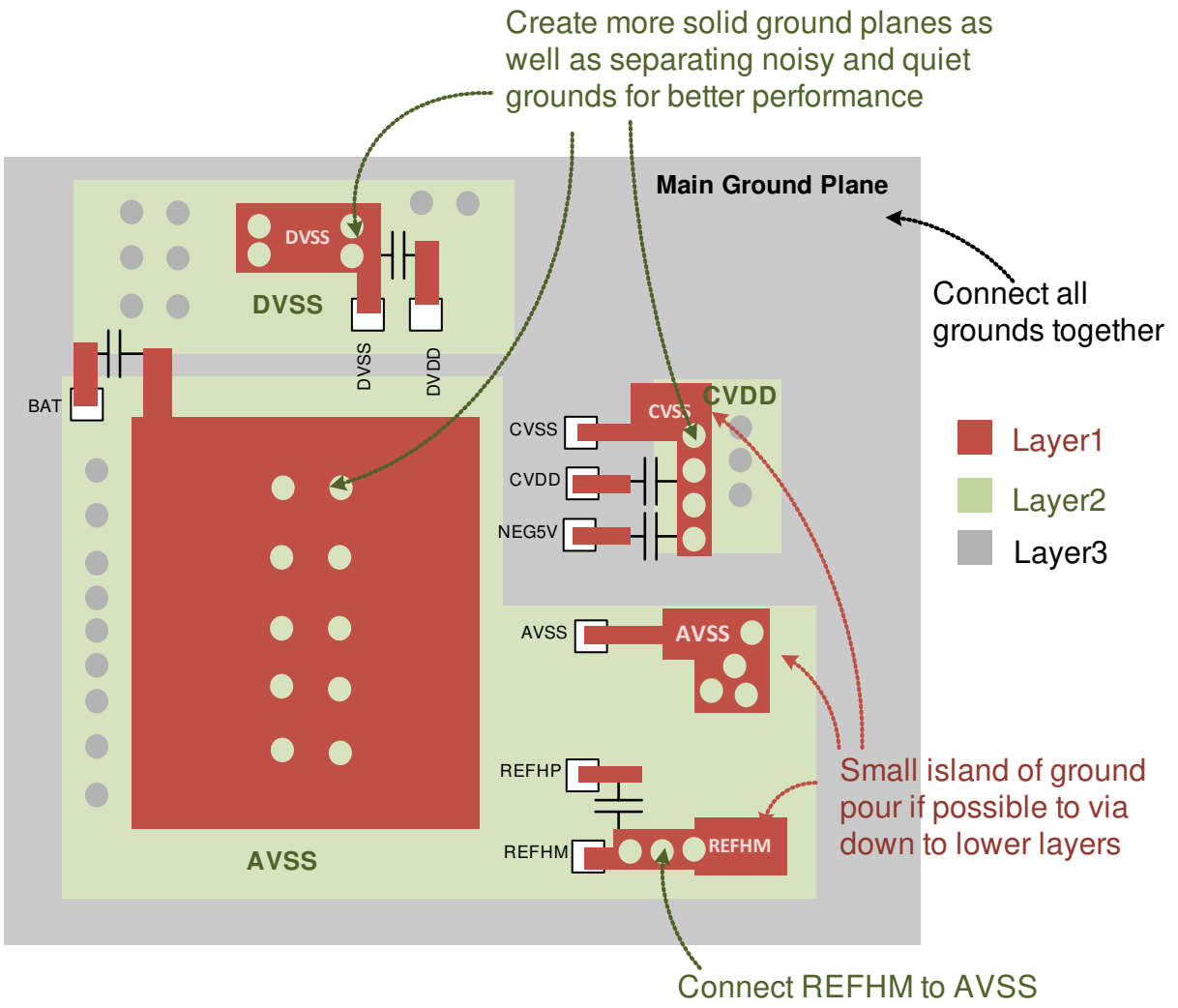
The layout for this device must be designed carefully. Design outside these guidelines can affect the ADC accuracy and EMI performance. Care must be taken in the layout of signals to and from the device to avoid coupling noise onto sensitive inputs. The layout of ground and power connections, as well as communication signals should also be made carefully.

13.1 Ground Planes

It is very important to establish a clean grounding scheme to ensure best performance of the device. There are 3 ground pins (AVSS, DVSS, CVSS) for the device's internal power supplies and 1 ground reference (REFHM) for the precision reference. There are noisy grounds and quiet grounds that shall be separated in the layout initially and re-joint together in a lower PCB layer. The external components (e.g. bypass capacitors) shall be tied to the proper grounding group if possible to keep the separation of noisy and quiet grounds apart.

- AVSS ground:
  - Bypass capacitor for these pins: BAT, VC0, CB0, LDOIN, TSREF
  - Package lower pad
- DVSS ground:
  - Bypass capacitor for DVDD
  - GPIO filter capacitor (if used). It can also connect to AVSS ground plane if needed
- CVSS ground:
  - Bypass capacitor for CVDD
  - The bypass capacitors for COMHP/N and COMLP/N
- REFHM ground:
  - Bypass capacitor for REFHP
  - If possible, separate out REFHM from AVSS on the signal connection layer and reconnect REFHM to the AVSS ground plane on a lower layer

Even on a PCB layer that is mainly for signal routing, it is good practice to have as small an island of ground pour as possible to provide a low impedance ground, rather than simply via down the ground trace to an lower ground plane.



Note

The vias shown above are on all 4 layers. Layer 4 is not shown but should include any traces needed for bottom layer components and a solid ground plane otherwise.

Figure 13-1. Grounding Layout Consideration

There is a strong recommendation to have a minimum of four layers in the PCB, with one fully dedicated as an unbroken VSS plane (except thermal reliefs). Avoid placing tracks on this layer to maintain the unbroken integrity of the plane structure.

If multiple devices are placed on the same PCB, each device should have its own ground plane with proper layout clearance.

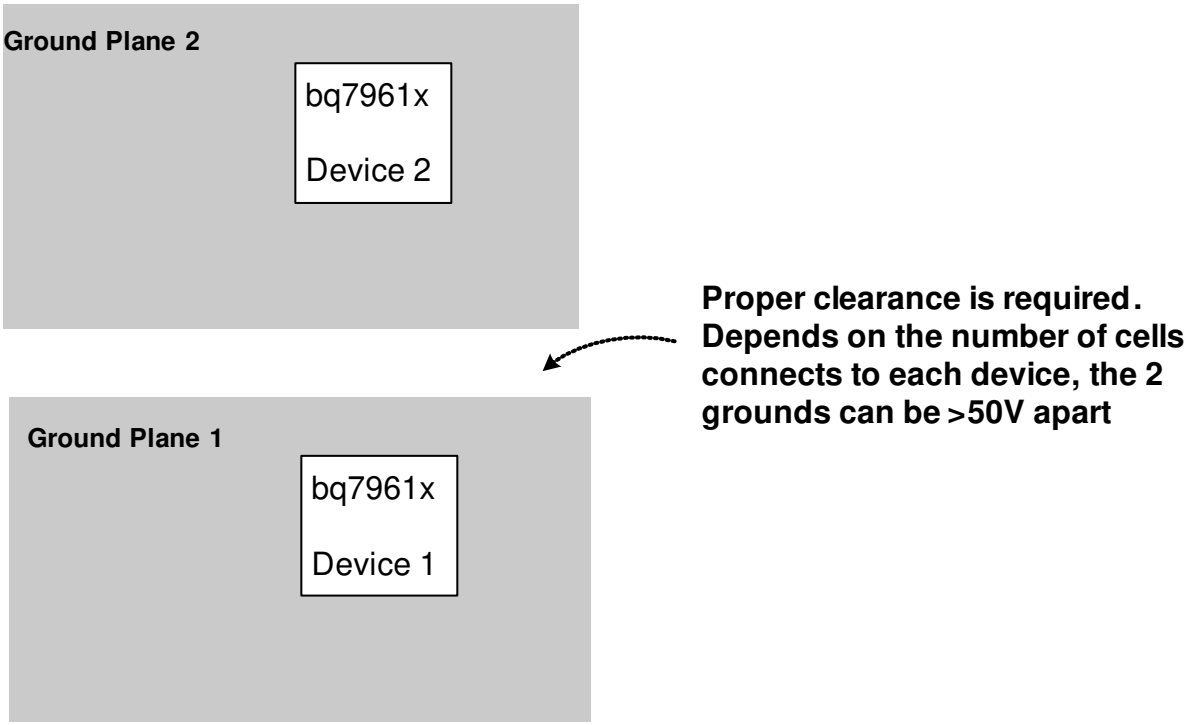


Figure 13-2. Separate Ground Plane per Device on the Same PCB

13.2 Bypass Capacitors for Power Supplies and References

The bypass capacitors of the following pins shall be placed as close to the device pins as possible to ensure proper performance, especially the REFHP capacitor. It is also recommended to help performance with derating and emissions performance to utilize a small capacitor in parallel with each bypass LDO capacitor of 10-22%. For example, on CVDD, we recommend both a 22-nF and 100-nF capacitors in parallel with 4.7-µF decoupling capacitor to help reduce emissions. These need to be designed extremely close to the pins of the IC in the layout for best effect.

- REFHP, BAT, LDOIN, AVDD, DVDD, CVDD, TSREF, NEG5V

13.3 Cell Voltage Sensing

Cell voltage sensing traces (VC pins and CB pins) shall be placed in parallel with impedance matching.

The balancing traces (CB pins) shall be sized properly to carry the maximum balancing current and ensure proper thermal performance for the application.

It is recommended to use separate cables, connector tabs, and PCB traces for the BAT pin and top VC pin connection. The same applies to the AVSS and VC0 connections. This is to avoid the device current impacting the top and bottom cell voltage measurements.

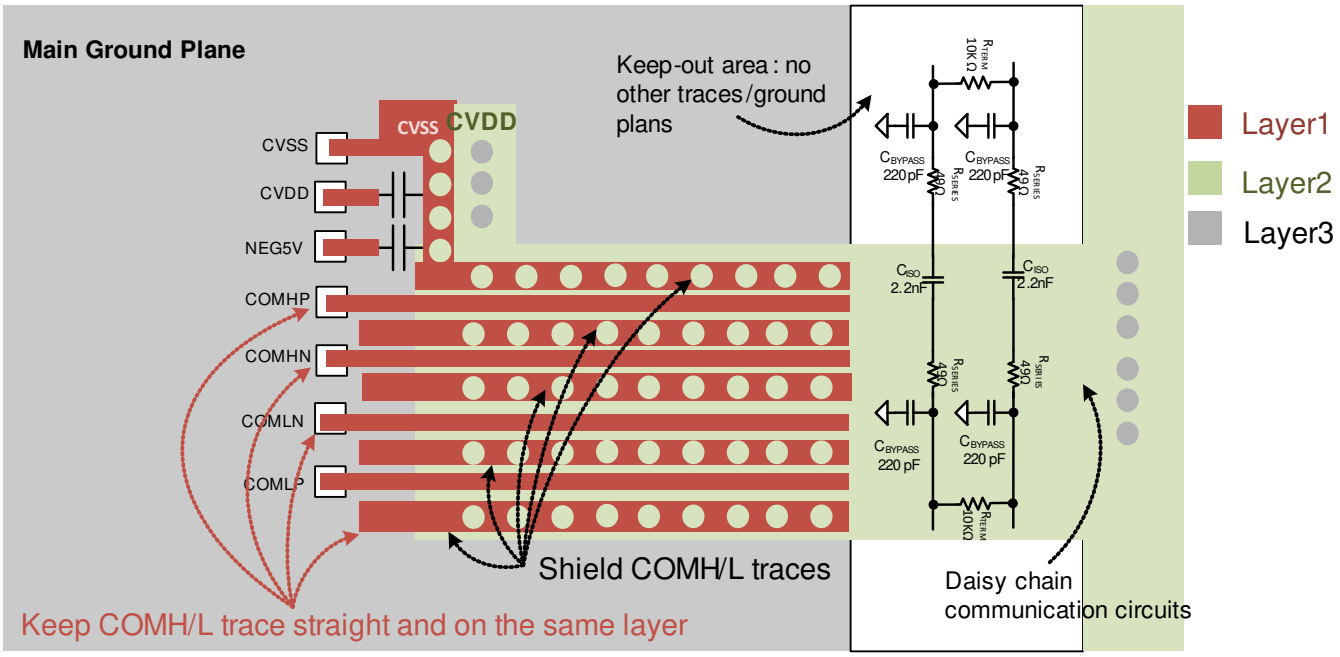
If the same cable and connector tab are used for the BAT/top VC pins connections and AVSS/VC0 pins connections, the PCB trace going to the BAT/top VC pins and AVSS/VC0 pins shall be separated at the connector tabs. Note the device current will still go through the cell to the PCB cable, which may introduce IR error across the cable connection to the top and bottom cell measurements.

13.4 Daisy Chain Communication

Maintaining signal integrity while in a stacked configuration is critical to the success of this part. To maximize immunity from interfering signals, there are a couple design choices that need to be made. For transformer based communication, be sure to select a transformer that provides adequate isolation.

1. Keep differential traces as short as possible and as straight as possible. Minimize turns and avoid any looping on the traces.

2. Keep the differential traces on the same layers. Run the trace in parallel with shielding and matching trace impedance.
3. Place the isolation components close to the connectors.
4. When using capacitive isolation, place the high voltage capacitor of the COMxP/N pair (where x = H, L) close to each other along the parallel traces.
5. Create a keep-out area (no other traces and no ground plane) around the daisy chain components in all PCB layers.



Note

The vias go through all 4 layers. Layer 4 is not shown as the bottom layer can include traces for any bottom side components and a solid ground plane otherwise.

Figure 13-3. Daisy Chain Layout Considerations

14 BCI Performance

Bulk Current Injection (BCI) was performed according to the ISO 11452-4 standard. The cable length was 1.7 m with a baud rate of 1 Mbps. The BCI noise was injected on the communication lines. There were 3 different isolation methods that were tested: capacitive only, cap and choke, and transformer. Contact your local TI sales representative for further information on BCI performance.

15 Common and Differential Mode Noise

X-Y caps are commonly used and may be required for extremely noisy environments.

- Differential mode noise goes out one wire and returns back on another wire. An X capacitor is placed between two lines to suppress the noise.
- Common mode noise goes out from both wires and returns back to the chassis through stray capacitance to ground. A Y capacitor is placed between the chassis as Figure 15-1 illustrates.

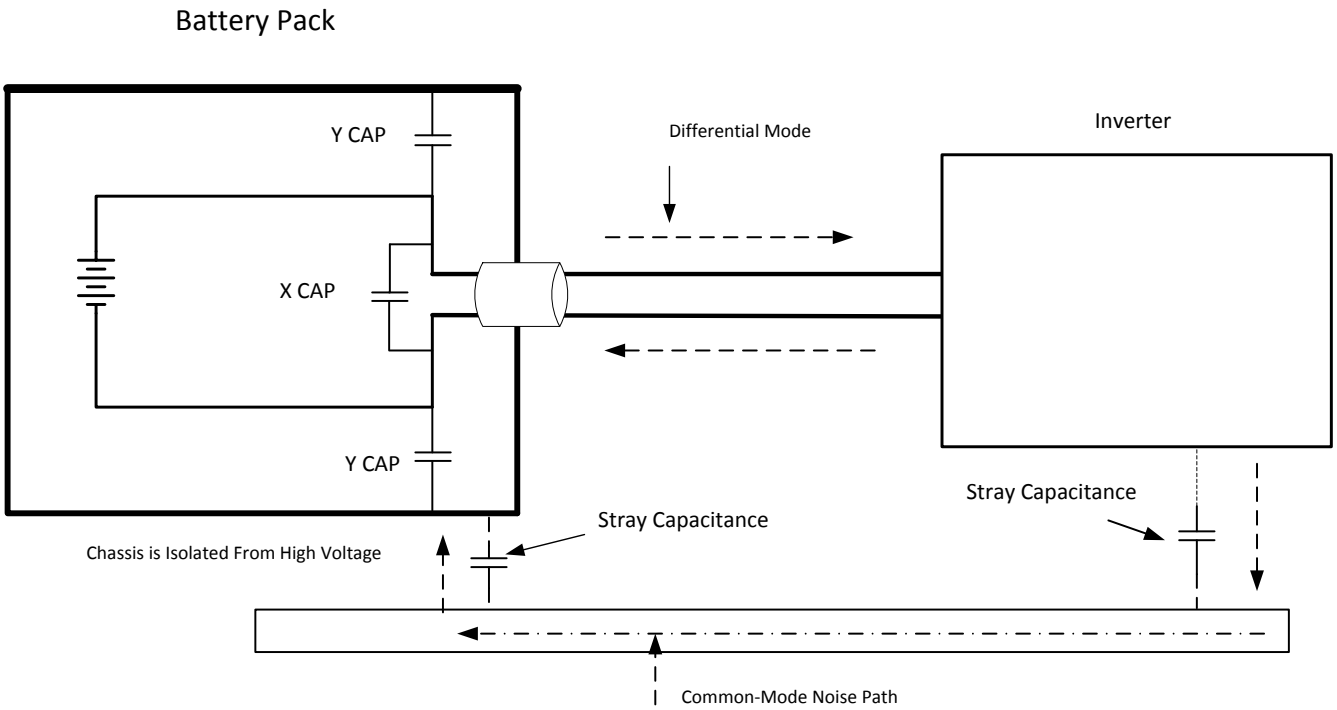


Figure 15-1. XY Caps

15.1 Design Consideration

- Device placement is important. The daisy-chain cable must not be resting on the bus bar or metal enclosure surface.

16 Revision History

Changes from Revision * (December 2020) to Revision A (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated document title	1
• Changed from *application note* to *user's guide*	1

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