Application Report
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Reducing Radiated EMI in TPS61088 Boost Converter

Helen Chen *Low-Power DC/DC Converters*

ABSTRACT

In switching power supplies, EMI noise is an unavoidable issue because of the high frequency switching actions of the semiconductors and the resulting high di/dt pulsating current. EMI control is a big challenge in SMPS design. This application note describes the basic operation of the boost converter, and provides some practical tips on how to reduce the radiation EMI in the TPS61088 boost converter design.

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1 Introduction

The synchronous boost converter TPS61088 is an easy-to-use step-up DC-DC converter which provides a high-efficiency and small-size solution in the portable systems. It is widely used in the quick charge power bank, blue-tooth speaker, portable POS terminal, and so forth. Some customers fail the EN55022 and CISPR22 Class B radiated emission test, though they have already used multi-layer PCB, added RC snubber, and used enough decoupling caps in the circuit. By study, we found that almost all of the failures are caused by poor layout.

This application note describes the basic operation of the boost converter, and provides some practical tips on how to reduce the radiation EMI in the TPS61088 boost converter design.

2 Design Process

2.1 Identify Critical Current Path

EMI starts off from high di/dt loops. So we should differentiate the high di/dt critical path at the beginning of the design. To achieve these, it is important for us to understand the current conduction paths and signal flows in the switching power supply.

Figure 1 shows the topology and critical current path of the Boost converter. When S2 closed and S1 opens, the AC current flows through the blue loop. When S1 closed and S2 opens, the AC current flows through the green loop. So the current flows through input capacitor Cin and inductor L is a continuous current, while the current flows through the S2, S1 and the output capacitor Cout is a pulsating current (red loop). The red loop is defined as the critical current path. This path has the highest EMI energy. Minimize the area enclosed by it during the layout.

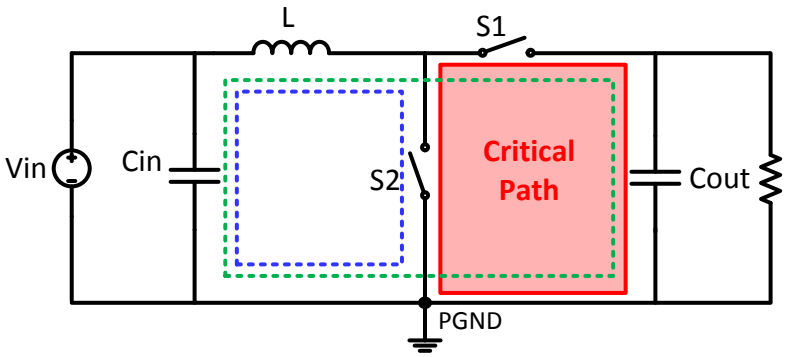

Figure 1. Critical Current Path of Boost Converter

2.2 Minimize High di/dt Path Loop Area

Figure 2 shows the pin configuration of the TPS61088.

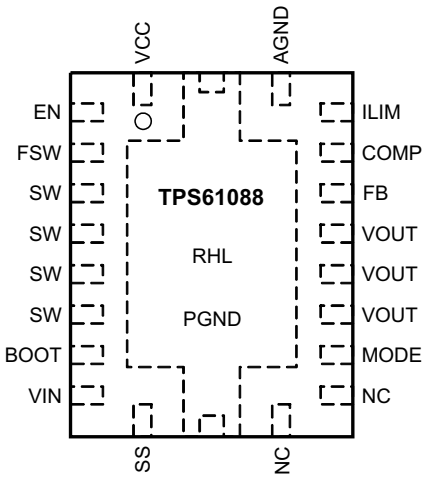

Figure 2. TPS61088 Pin Configuration

Figure 3 shows the TPS61088 critical current path layout example. The NC pin means no connection inside the device, so they can be connected to PGND. From the electrical point of view, connecting the two NC pins to the PGND ground plane is good for thermal dissipation and can reduce the impedance of the return path. From the EMI point of view, connecting the two NC pins to the PGND ground plane makes the VOUT and PGND plane of the TPS61088 much closer to each other and this makes the placement of the output capacitors much easier.

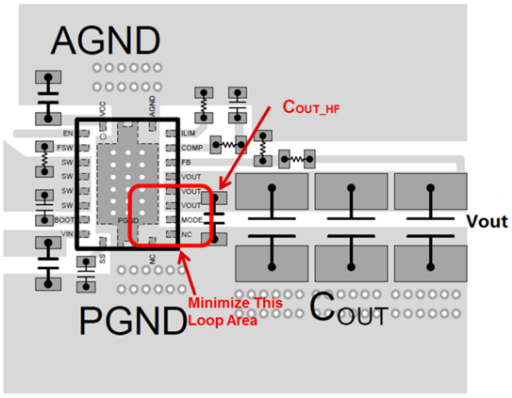

Figure 3. TPS61088 Critical Path Layout Example

Figure 3 illustrates that placing one 0603 1-µF (or 0402 1-µF) high frequency ceramic capacitor, C_{OUT_HF}, as close to the VOUT pin as possible results in minimum area of the high di/dt loop.

The maximum electric field strength from such a high di/di loop over a ground plane at a 10-meter distance is calculated using Equation 1:

$$E = 263 \times 10^{-12} \times (f^2 \times A \times I_S) \quad (1)$$

where

- A is the loop area in cm^2
- I_s the current flowing in the loop at an interested frequency in mA. (For square waves, the Fourier Spectrum must be used to get I_s)
- f is the interested frequency of I_s

Figure 4 shows the critical path area with and without C_{OUT_HF}. It is apparent that the critical path area will get much bigger if we remove this capacitor.

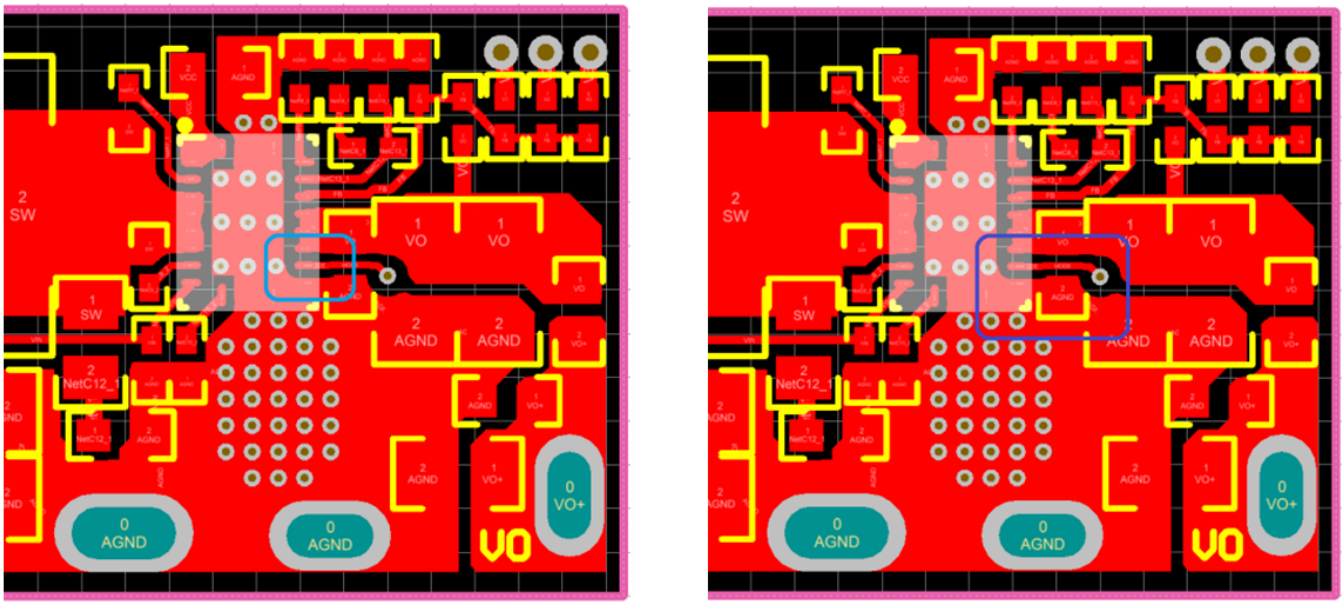

Figure 4. Critical Path Area With and Without C_{OUT_HF}

Figure 5 shows the SW voltage ringing with and without C_{OUT_HF}. Because of the higher self-loop inductance and parasitic inductance without C_{OUT_HF}, the SW voltage spike is much higher in this condition.

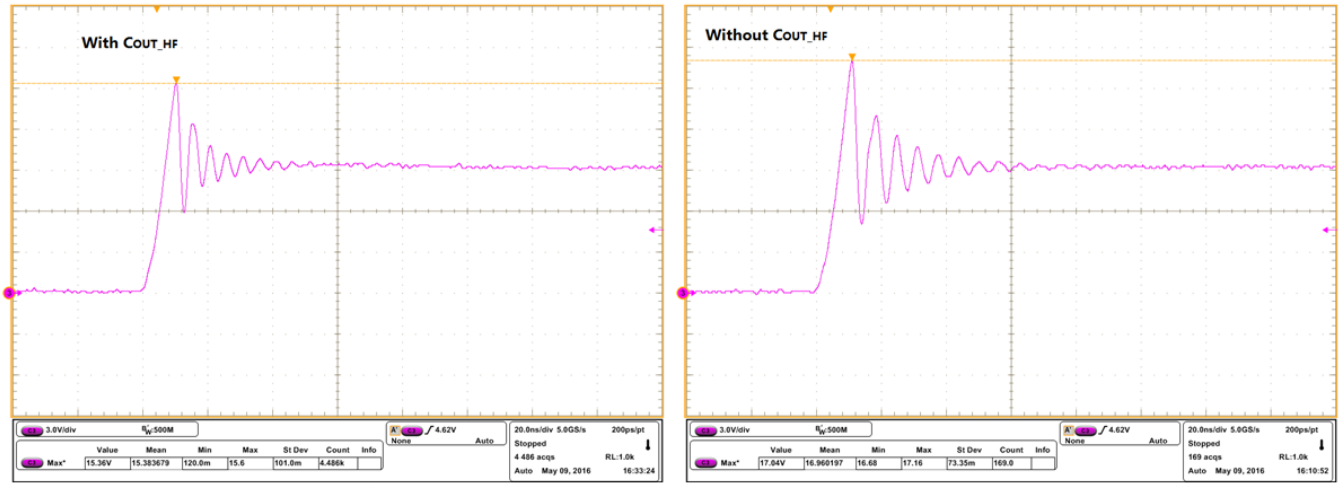

Figure 5. SW Voltage Spike With and Without C_{OUT_HF}

Figure 6 shows the radiated EMI result with and without C_{OUT_HF}. Under the same test condition, the radiated EMI is improved by 4 dBuV / m with C_{OUT_HF}.

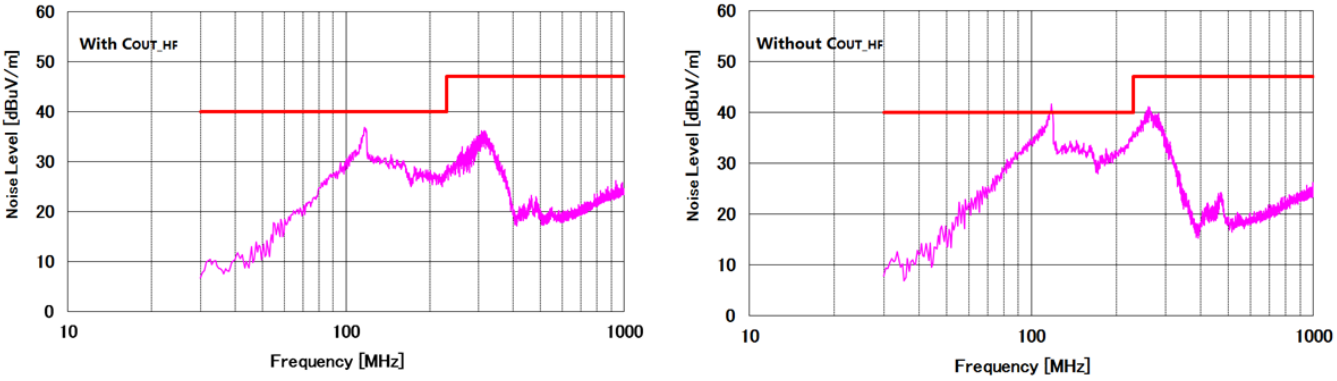

Figure 6. Radiated EMI Result With and Without C_{OUT_HF}

2.3 The Importance of Ground Plane

The inductance of a PCB trace is firstly a function of its length, and secondarily a function of its width. For a single-layer PCB trace with width W_{trace} and length l in cm, its inductance is calculated with Equation 2:

$$L = 0.002 \times l \times \left[\ln\left(\frac{2l}{W_{trace}}\right) + 0.2235 \times \left(\frac{W_{trace}}{l}\right) + 0.5 \right] \mu H \quad (2)$$

So the total inductance of a 2.5 cm × 2.5 cm rectangular loop with 0.5-mm trace width is about 130 nH. Increase the trace width to 1 mm, the total loop inductance is 116 nH. So doubling the trace width does not produce a 50% decrease in inductance. The inductance is mainly determined by the trace length.

High trace inductance leads to poor radiation EMI. Because the magnetic field strength is in direct proportion to the inductance. Placing a solid ground plane on the next layer of the critical trace can solve this problem. In a multi-layer PCB with ground planes, the approximation inductance of a given trace can be calculated using the following equation:

$$L = \frac{\mu_o \times h}{2 \times W_g} \approx \frac{6 \times h}{W_g}\left(\frac{nH}{cm}\right) \quad (3)$$

where

- $\mu_0 = 4\pi \times 10^{-7}$
- h is the insulation thickness between the signal layer and the ground plane
- W_g is the width of the ground plane.

Equation 3 shows that wider and bigger ground planes result in smaller signal trace inductance. Thinner insulation thickness between the ground plane and the signal traces also results in smaller inductance.

Table 1 gives out the inductance of a given trace on different PCB boards. We can see that for a 4-layer PCB with 0.4-mm insulation between the signal layer and the ground plane, the trace inductance is much smaller than that of a 1.2-mm thick 2-layer PCB. Putting a solid ground plane with minimum distance to the critical path is one of the most effective ways to reduce the EMI.

Table 1. Trace Inductance (Trace Length = 5 cm)

PCB	h (mm)	W_g (mm)	L (nH)
Single-Layer PCB	--	--	52
2-Layer PCB	1.2	10	3.6
4-Layer PCB	0.4	10	1.2

Figure 7 shows the radiated EMI result of a 2-layer PCB and a 4-layer PCB. Under the same layout and same test condition, the radiated EMI is improved by more than 10 dBuV / m with a 4-layer PCB.

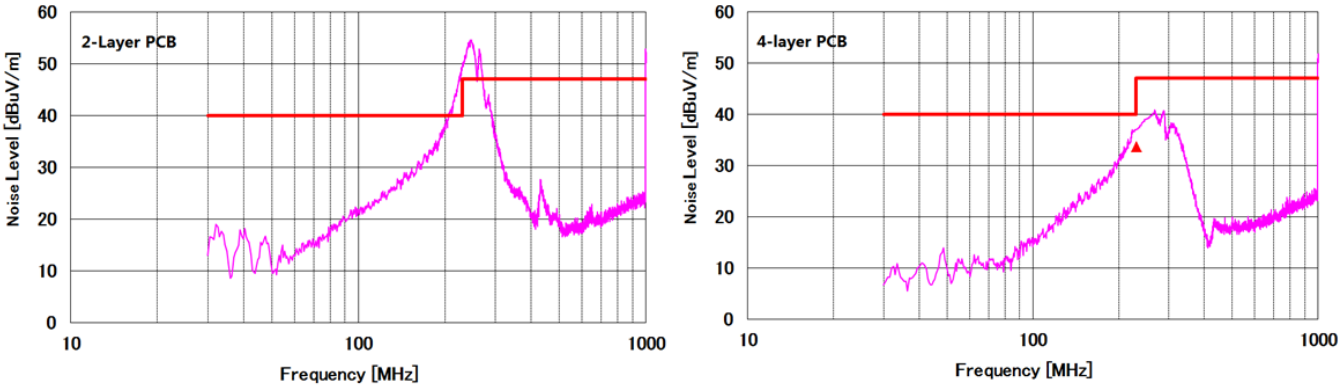

Figure 7. Radiated EMI Result of a 2-Layer PCB and a 4-Layer PCB

2.4 Benefits of the RC Snubber

If the radiation level still exceeds the requirement level and the layout cannot be improved anymore, then adding an RC snubber across the SW pin and the power ground of the TPS61088 can help reduce the radiation EMI levels. The RC snubber should be placed as close as possible to the switching node and the power ground (Figure 8).

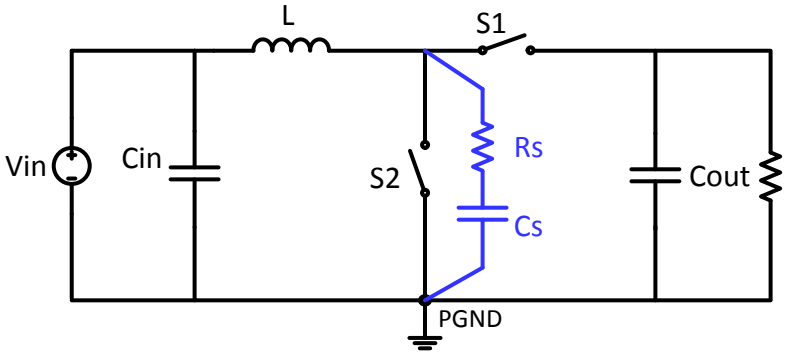

Figure 8. Placement of RC Snubber

Adding a RC snubber can effectively damp out SW voltage ring (Figure 9), which means the radiated EMI at the ringing frequency can be improved.

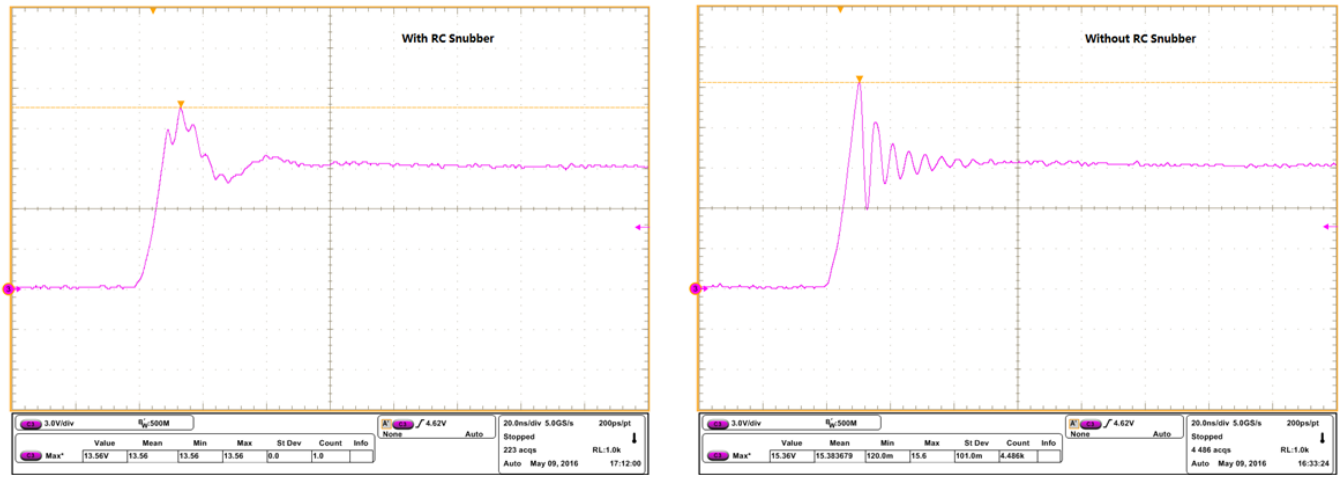

Figure 9. SW Voltage Comparison With and Without RC Snubber

The aim of the snubber resistor RS is to add sufficient damping to the parasitic resonant circuit. The value of RS depends on the desired damping factor and the parasitic inductor L_P and parasitic capacitor CP of the circuit. It is calculated with Equation 4:

$$R_S = \frac{1}{2\xi} \times \sqrt{\frac{L_P}{C_P}} \quad (4)$$

where

- ξ is the damping factor. Normally ξ can range from 0.5 to 1.

The values of the parasitic parameters L_P and C_P can be measured in the following way:

1. Measure the original ringing frequency f_{RING} without the RC snubber
2. Add some small capacitance from switch node to ground. Keep increasing capacitance until the ringing frequency is 50% of the original ringing frequency f_{RING}.
3. A 50% reduction in ringing frequency means that the total resonance capacitance is four times the original capacitance. The original capacitance, C_P, is one-third of the added capacitance C_S.
4. The parasitic inductance L_P can be calculated using $$L_P = \frac{1}{C_P \times (2\pi \times f_{RING})^2}$$

Normally C_S is chosen 3 to 4 times larger than the circuit parasitic capacitance C_P. Large C_S results in high power loss due to charging and discharging of the capacitor each switching cycle. The power loss across the RC snubber can be calculated with Equation 5:

$$P = C_S \times V^2 \times f_{SW} \quad (5)$$

where

- V is the peak SW voltage
- f_{SW} is the switching frequency

Besides resonance damping, the RC snubber will also slightly increase the rise and fall times of the switching waveform.

The left side of Figure 10 shows a simplified trapezoidal current waveform with period T, pulse width t_W, rise time t_R and fall time t_F. The right side of Figure 10 shows the frequency domain which consists of fundamental frequency and many upper harmonics. The relation with the pulse period, pulse width, rise/fall times, and amplitude of the upper harmonics can be derived via Fourier analysis.

Figure 10 is based on a 500 kHz switching signal with 1 µs pulse width, 5 ns rise time and 8 ns fall time. When $t_R \neq t_F$, only the smaller one is considered. So the band width f_R is determined by t_R. Radiated EMI problems often occur in the 50 MHz–300 MHz range. It can be seen that increasing rise (or fall) time will shift the f_R point to a lower frequency. Thus the high frequency harmonic content will roll-off more quickly with 40 dB / dec.

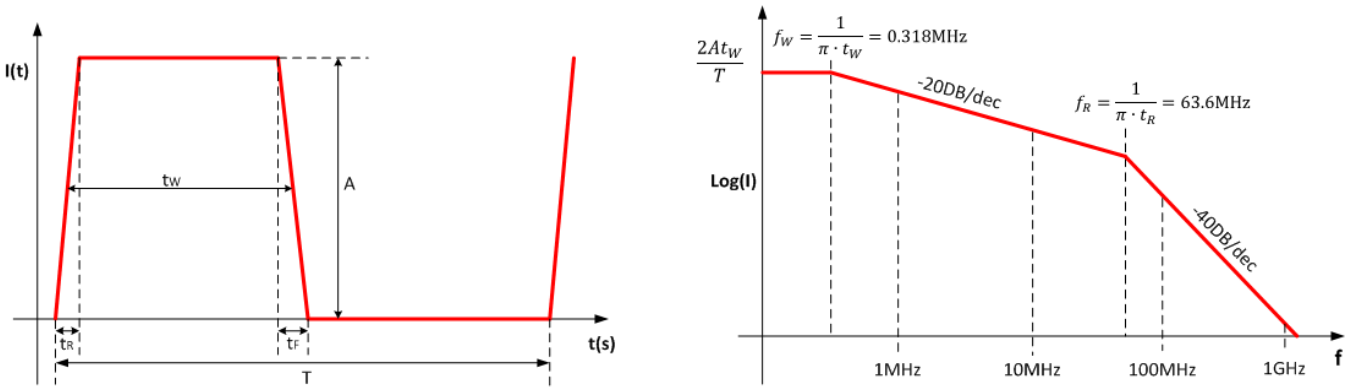

Figure 10. Harmonic Content of a Pulsed Current Waveform

Figure 11 shows the radiated EMI results with and without an RC snubber. Under the same test condition, the radiated EMI is improved by 4 dBuV / m with R_S = 1 Ω and C_S = 2200 pF.

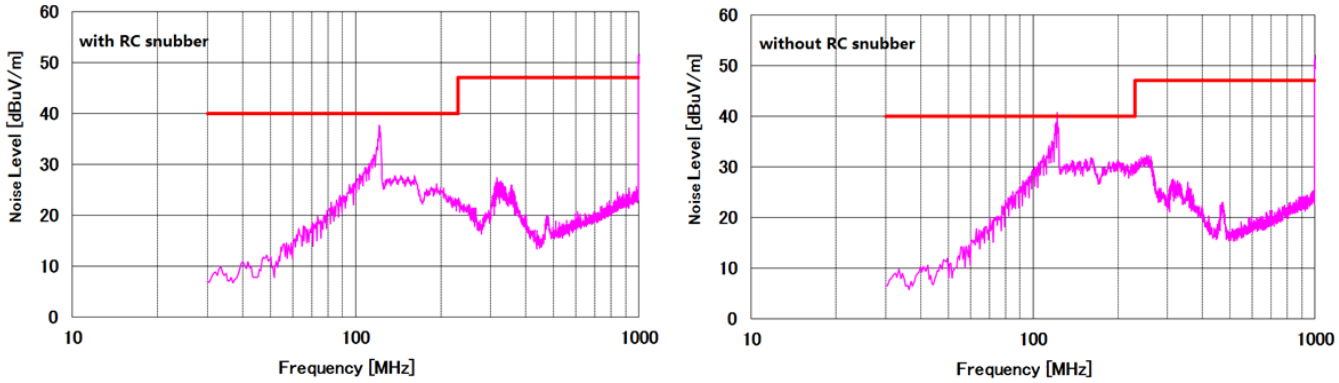

Figure 11. Radiated EMI Result With and Without RC Snubber

2.5 Radiation from Cables

If the switching frequency noise is not properly decoupled, the noise can be conducted out through input cables or output cables. Sometimes, the noise signal can directly couple to the cables through capacitive or inductive coupling.

The maximum field strength of a cable in a 10-m semi-anechoic chamber can be calculated using Equation 6:

$$E = 1.26 \times 10^{-4} \times f \times I_{cable} \times I_{CM} \quad (6)$$

where

- I_{cable} is the cable length in meters
- I_{CM} is the common mode current at the interested frequency f
- f is the interested frequency

From Equation 6, we can see that longer input or output cables result in poor radiation EMI. In the power bank application, the battery's electrodes are directly soldered on the PCB, so the input cable is very short. The output cable is about 20 cm. So during the test, make the length of the input cable and output cable very close to the real application or the radiated EMI test result is meaningless.

Figure 12 shows the radiated EMI results with different input cable lengths (the output cable length is the same). Under the same test condition, the radiated EMI is improved by about 4 dBuV / m with a short input cable.

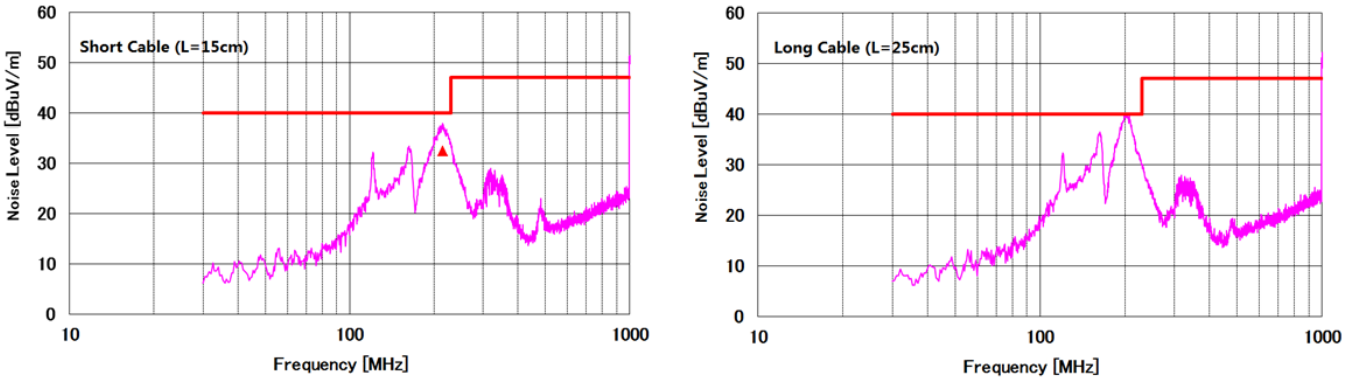

Figure 12. Radiated EMI Result with Different Input Cable Length

2.6 Ferrite Bead Selection

The ferrite bead is one of the most effective and simplest filters that can be directly mounted on the PCB like a SMD capacitor. But unlike the bypass capacitor, the ferrite bead is used in series with the power line, so it must be selected carefully. An improper ferrite bead cannot improve the radiation EMI and may even degrades the circuit performance.

Firstly, the noise frequencies must fall within the resistive band of the bead. That is, the impedance versus frequency characteristics must be carefully studied when choosing a ferrite bead. Make sure the resistive impedance of the bead is much higher than the reactive impedance in the noise frequency range. Figure 13 shows the impedance versus frequency characteristic of the Murata part BLM21PG300SN1. Figure 13 illustrates that this bead can provide optimum performance at noise frequencies from the 100 MHz to 3 GHz range.

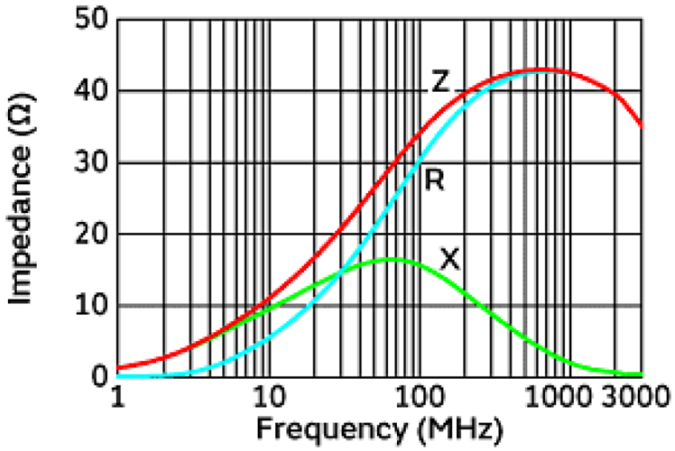

Figure 13. Impedance VS. Frequency Characteristics (BLM21PG300SN1)

Secondly, the rated current of the ferrite bead should be at least 30% higher than the expected maximum current because the ferrite bead will saturate in high current conditions.

Thirdly, the DC resistance of the ferrite bead should be as low as possible, because the DC current flowing through it will create a voltage drop proportional to the DC resistance. So high DC resistance may lead to poor load regulation and low efficiency.

3 Radiated EMI Result of the TPS61088 Boost Converter

Figure 14, Figure 15, and Figure 16 show the TPS61088 boost converter radiated EMI results performed on a reference design board (PMP9778). These tests were performed in a third party certified 3 meter EMI chamber. It is clearly illustrated that all the tests passed the EN55022 and CISPR22 Class B limit, with more than 6-dB margin.

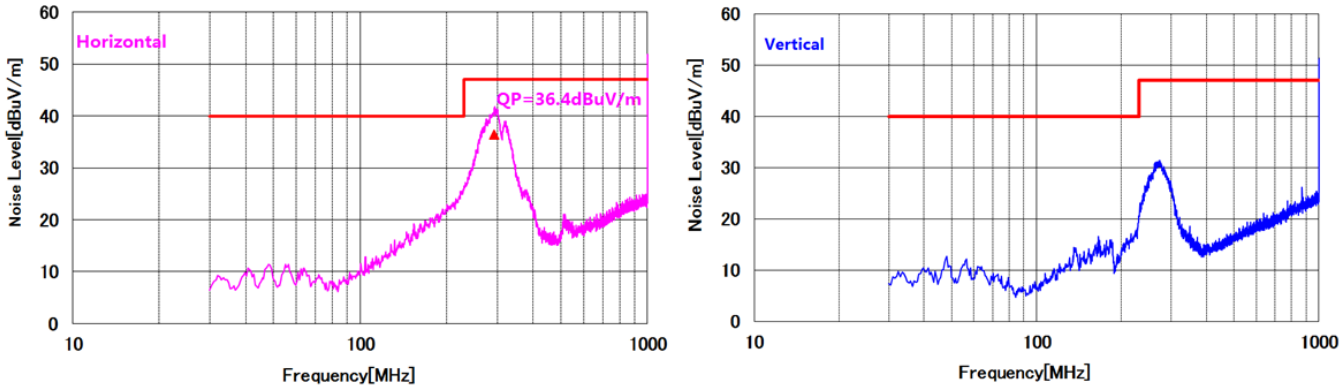

Figure 14. Radiated EMI Result (V_{IN} = 3.3 V, VO = 5V / I_O = 3A)

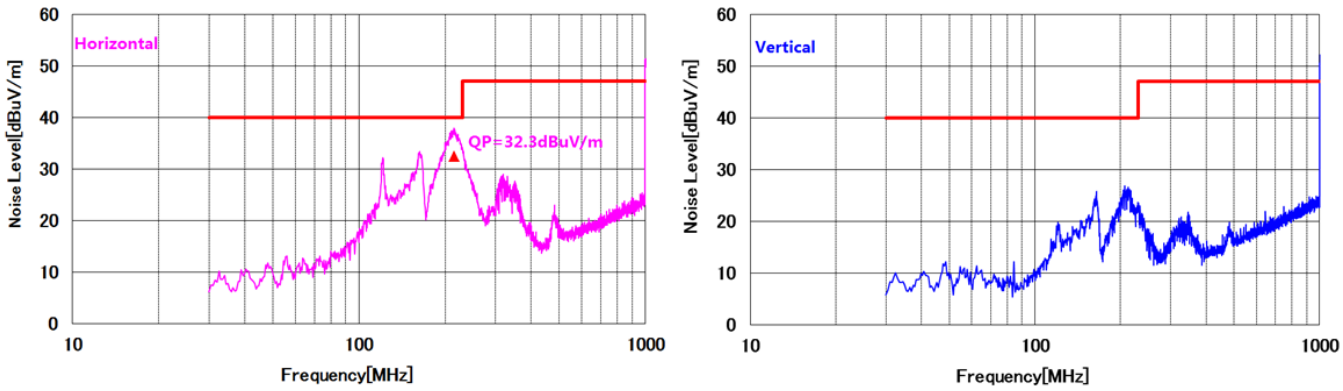

Figure 15. Radiated EMI Result (V_{IN} = 3.3V, VO = 9 V / I_O = 2A)

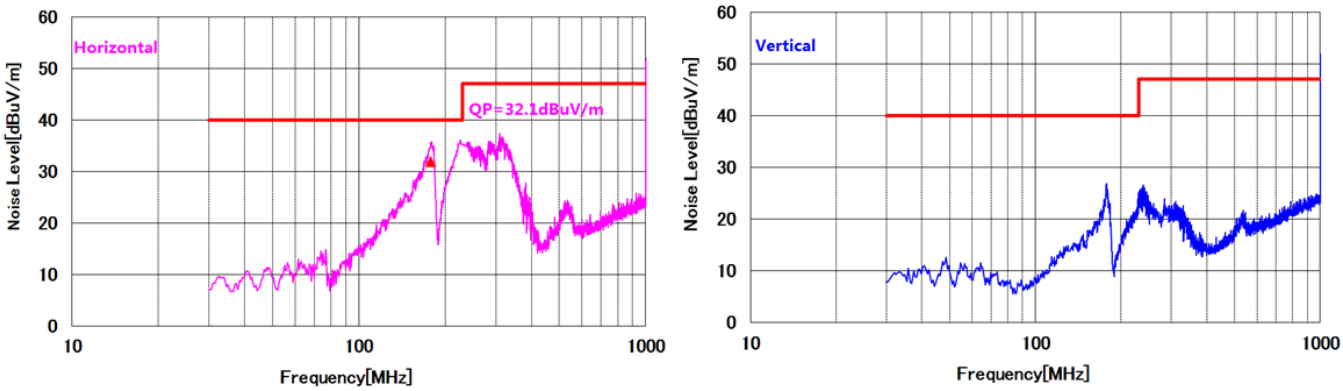

Figure 16. Radiated EMI Result (V_{IN} = 3.3V, VO = 12V / I_O = 1.5 A)

4 Conclusion

The major radiation source in a boost converter is the output switching loop. This critical loop should be as small as possible. Because of the good pin configuration, the output switching loop of the boost converter TPS61088 is very small.

Putting a solid ground plane with minimum dielectric thickness under the critical loop can further reduce the critical loop inductance. Under the same placement and same test condition, the radiated EMI improves by more than 10 dBuV / m with a 4-layer PCB compared to that of a 2-layer PCB.

Adding a RC snubber can effectively damp out the SW voltage ring. The radiated EMI at the ringing frequency can be improved.

Ferrite bead can help to suppress the high frequency EMI noise in the circuit. It is in series with the power line, so it must be selected carefully.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to A Revision	Page
• Updated Introduction section	1

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