User's Guide

TPS62869EVM-118 Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of TI's evaluation module (EVM) for the TPS628691, TPS628692, TPS628681, TPS628682 devices. The TPS62869EVM-118 (BSR118) facilitates the evaluation of the TPS62869 family of 6-A, step-down converter with DCS-Control™in a small 1.5-mm by 2.5-mm QFN package solution. The EVM creates output voltages between 0.4V and 1.675V with 1% accuracy output voltages from higher input voltages between 2.4 V and 5.5 V, to a regulated 0.9V output voltage. The TPS62869 family is a highly efficient and tiny solution for point-of-load (POL) converters for space-constrained applications, such as artificial intelligence chips, camera modules, solid state drives (SSDs), and optical modules.

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1 Introduction

The TPS62869 is a family of synchronous, step-down converter, coming in a 1.5-x2.5-x1.0-mm QFN package.

1.1 Performance Specification

Table 1-1 provides a summary of the TPS62869EVM-118 performance specifications.

Table 1-1. Performance Specification Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		2.4	5	5.5	V
Output voltage setpoint			0.9		V
Output current		0		6000	mA

1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate the different adjustable output voltage versions of this integrated circuit (IC). On the EVM, additional input and output capacitors can be added.

2 Setup

This section describes how to properly use the TPS62869EVM-118.

2.1 Input/Output Connector Descriptions

J1, Pin 1 and 2 – VIN Positive input connection from the input supply for the EVM

J1, Pin 3 and 4 – S+/S- Input voltage sense connections. Measure the input voltage at this point.

J1, Pin 5 and 6 – GND Input return connection from the input supply for the EVM

J2, Pin 1 and 2 – VOUT Output voltage connection

J2, Pin 3 and 4 – S+/S- Output voltage sense connections. Measure the output voltage at this point.

J2, Pin 5 and 6 – GND Output return connection

J3, Pin 5 – VBUS The VBUS pin of this header is used to bias the SCL and SDA nodes of I²C interface via a resistor.

J3, Pin 6 – GND The GND pin of this header is used to connect the grounds of the IC and the I²C interface.

J3, Pin 9 – SCL The pin of this header should be connected to the SCL of the I²C interface.

J3, Pin 10 – SDA The pin of this header should be connected to the SDA of the I²C interface.

JP1 – VID/PG VID/ PG pin jumper. Place the jumper across VID/ PG and LOW pins before start-up. This sets the output voltage and device address. After startup, VOUT reflects the value set on V_{OUT} Register 1 if the jumper is placed across VID/ PG and LOW pins. VOUT follows the value set on V_{OUT} Register 2 if the jumper is placed across VID/ PG and HIGH pins.

JP2 – EN EN pin input jumper. Place the jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.

2.2 Hardware Setup

To operate the EVM, set jumpers JP1 and JP2 to the desired position per Section 2.1. Connect the input supply to J1 and connect the load to J2.

3 TPS62869EVM-118 Test Results

The TPS62869EVM-118 was used to take the typical characteristics in the TPS62869 data sheet (SLVSFS3). See the device data sheet for the performance of this EVM.

4 Board Layout

This section provides the TPS62869EVM-118 board layout and illustrations in Figure 4-1 through Figure 4-7. The Gerbers are available on the EVM product page: TPS62869EVM-118

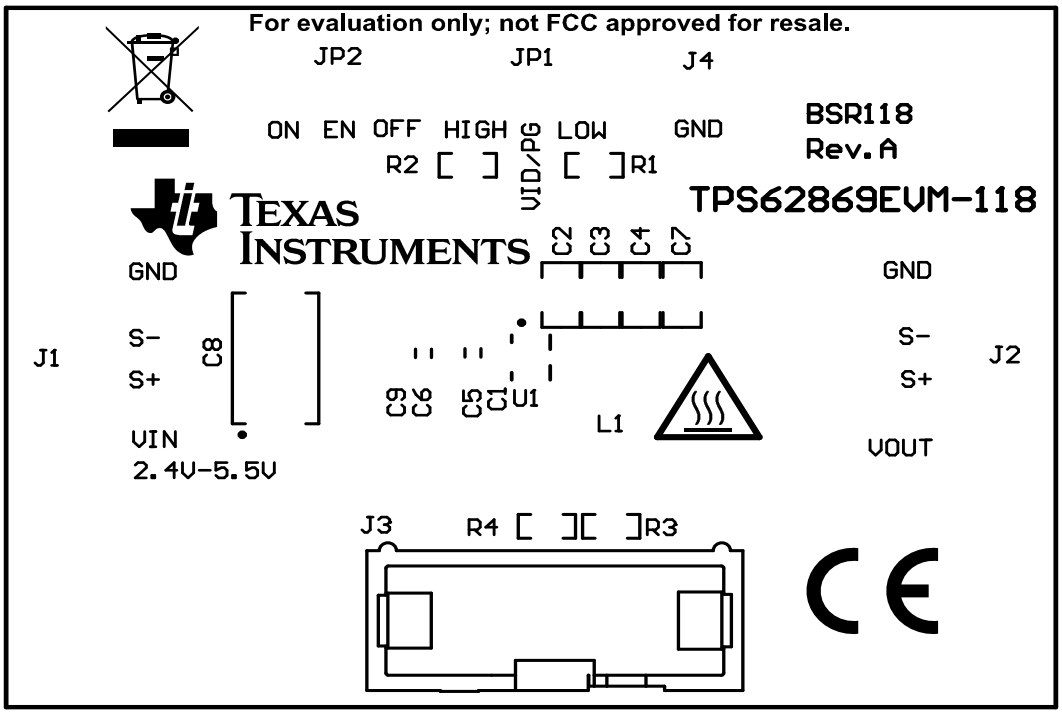

Figure 4-1. Top Assembly

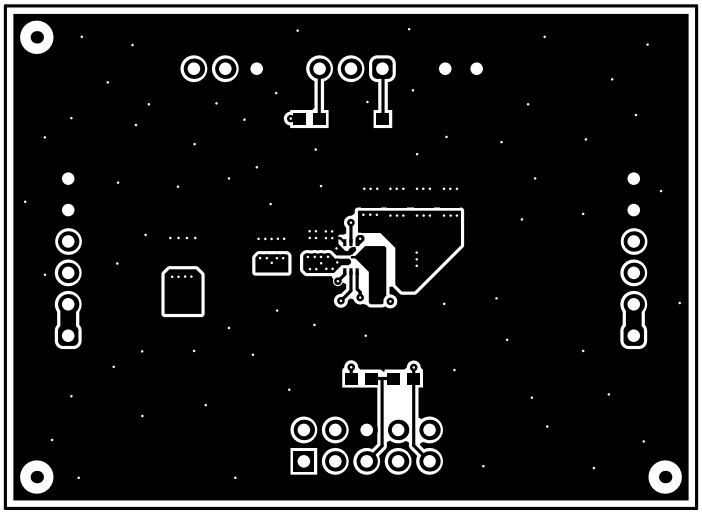

Figure 4-2. Top Layer

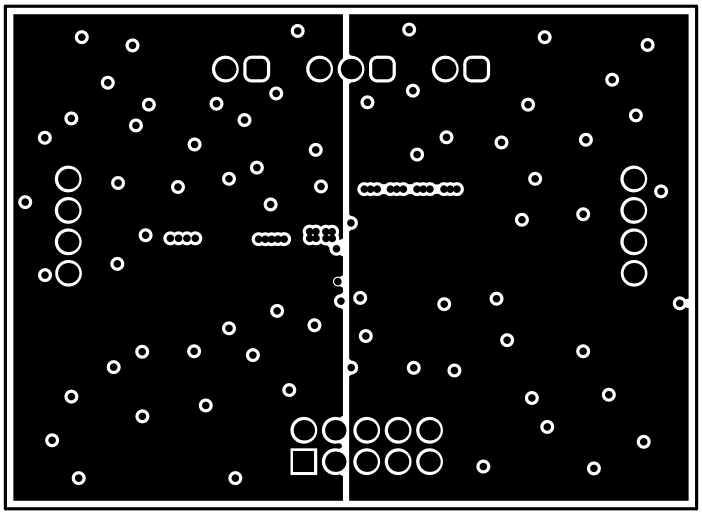

Figure 4-3. Signal Layer 1

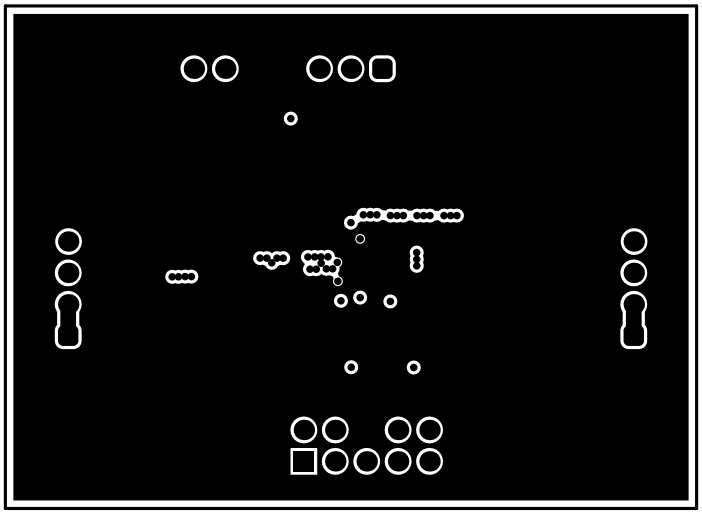

Figure 4-4. Signal Layer 2

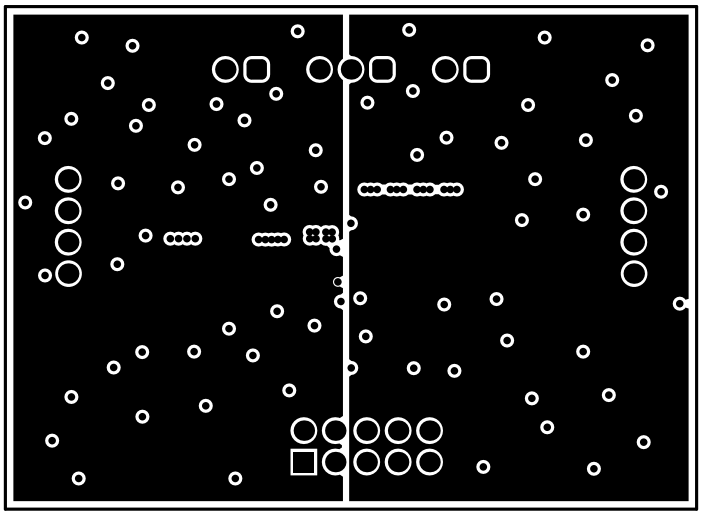

Figure 4-5. Signal Layer 3

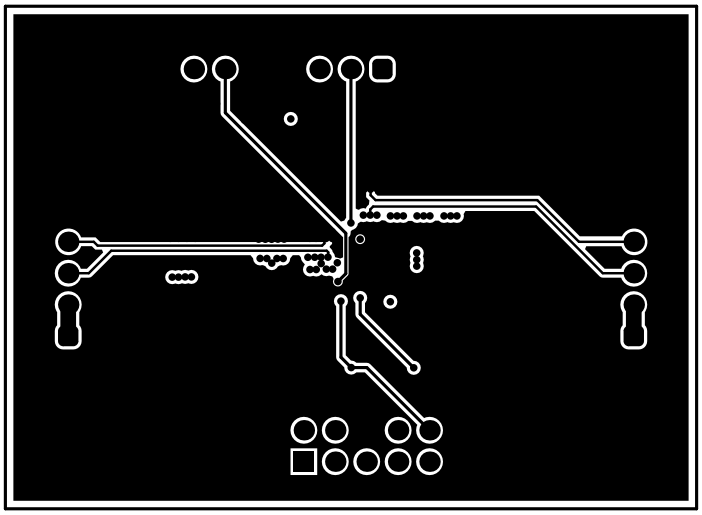

Figure 4-6. Signal Layer 4

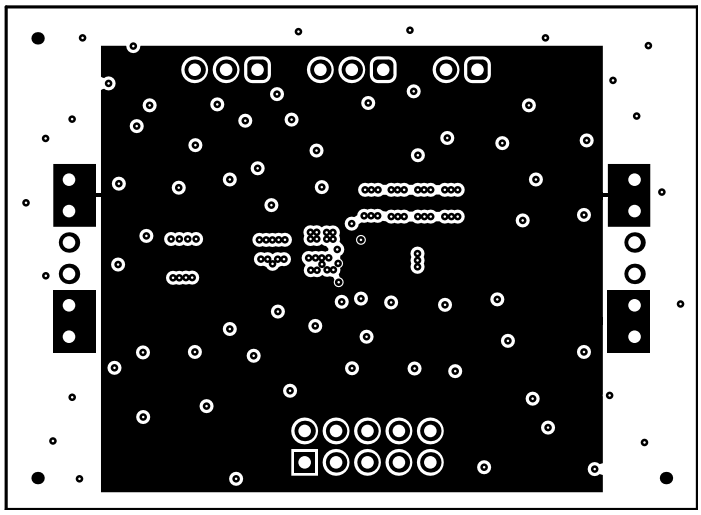

Figure 4-7. Bottom Layer

5 Schematic and List of Materials

This section provides the TPS62869EVM-118 schematic and list of materials.

5.1 Schematic

Figure 5-1 illustrates the EVM schematic.

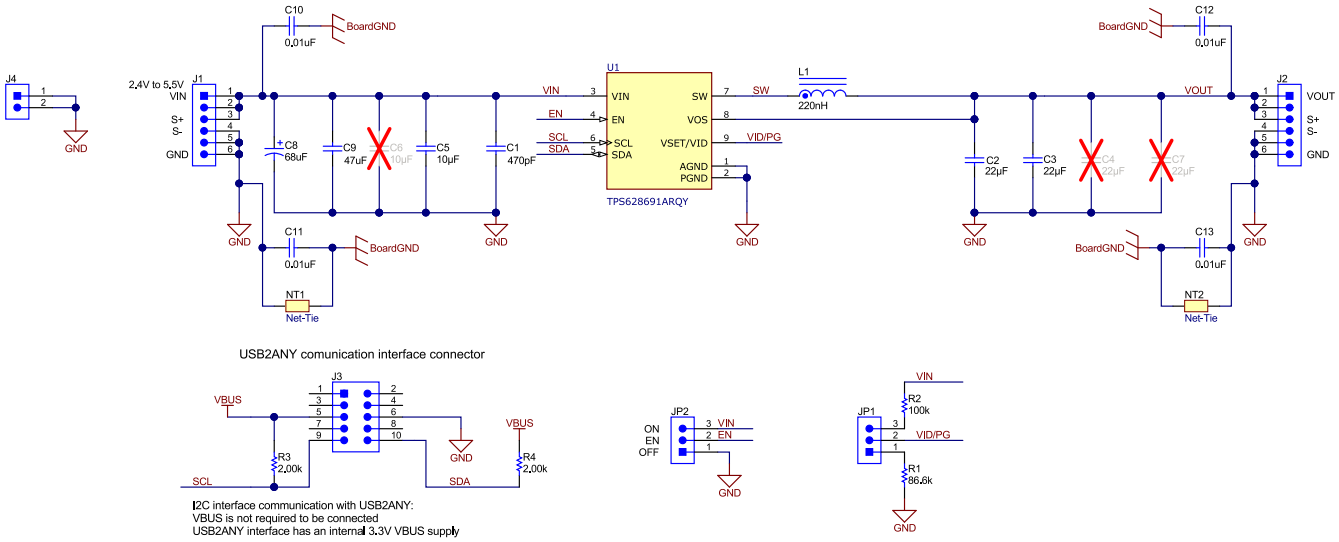

Figure 5-1. TPS62869EVM-118 Schematic

5.2 List of Materials

Table 5-1 lists a list of materials for this EVM.

Table 5-1. TPS628691ARQY List of Materials

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C1	1	Capacitor, Ceramic, 470 pF, 50 V, ±5%, C0G/NP0, 0603	GRM1885C1H471JA01D	Murata
C5	1	Capacitor, Ceramic, 10 µF, 10 V, ±10%, X7R, 0603	GRM188Z71A106KA73D	Murata
C2, C3	2	Capacitor, ceramic, 22 µF, 6.3 V, ±20%, X7R, 0805	GRM21BZ70J226ME44L	Murata
C9	1	Capacitor, Ceramic, 47 µF, 6.3 V, ±20%, X5R, 0603	GRM188R60J476ME15D	Murata
C8	1	Capacitor, tantalum, 68 µF, 20 V, ±10%, 7343	T495D686K020ATE150	Kemet
L1	1	Inductor, 220 nH, 16.8 A, 5.8 mΩ, SMD, 4040	XAL4020-221MEB	Coilcraft
R1	1	Resistor, 86.6 kΩ, 1%, 0.1 W, 0603	Std	Std
R2	1	Resistor, 100 kΩ, 1%, 0.1 W, 0603	Std	Std
R3, R4	2	Resistor, 2.0 kΩ, 1%, 0.1 W, 0603	Std	Std
U1	1	6-A Step-Down Converter with I²C Interface and Wide Output Voltage Range, QFN - 9 Pins	TPS628691ARQY	Texas Instruments

6 Software User Interface

6.1 Software Setup

A graphical user interface (GUI) is available from the TPS62869 tools and software page, which allows simple and convenient programming of the device through the TI USB2ANY interface board. Alternatively, you can use any I²C-standardized programming tool or I²C host to configure the device. Mind the I²C pins specification, such as timing parameters and proper pullup resistors, specified in the TPS62869 2.4-V to 5.5-V Input, 6-A Synchronous Step-Down Converter Data Sheet

6.2 Interface Hardware Setup

Connect the USB2ANY adapter to your PC using the supplied USB cable. Connect the EVM connector J3 to the USB2ANY adapter using the supplied 10-pin ribbon cable. The connectors on the ribbon cable are keyed to prevent incorrect installation. Figure 6-1 shows a quick adapter connection overview.

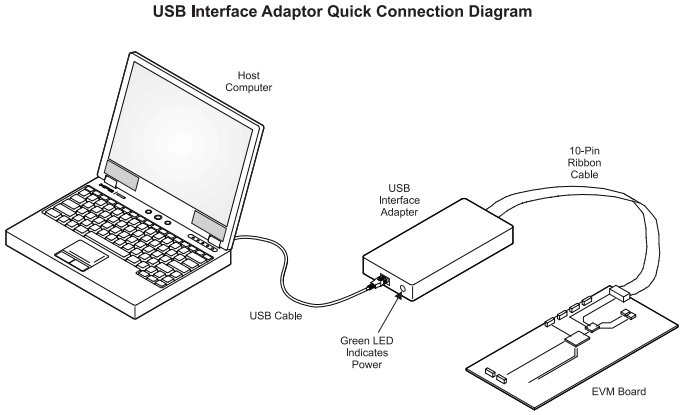

Figure 6-1. Quick Connection Overview

6.3 User Interface Operation

Upon start-up, the GUI automatically connects to the EVM. If not, click on the Connect button in the upper right corner of the GUI window. Ensure the I²C Slave Address is correct. The following sections give a short overview of the two main GUI screens.

6.3.1 Home Screen

The Home screen gives a short overview of the TPS62869 devices. To start evaluating the device, click on the Start button or on the Settings icons on the left side of the GUI window.

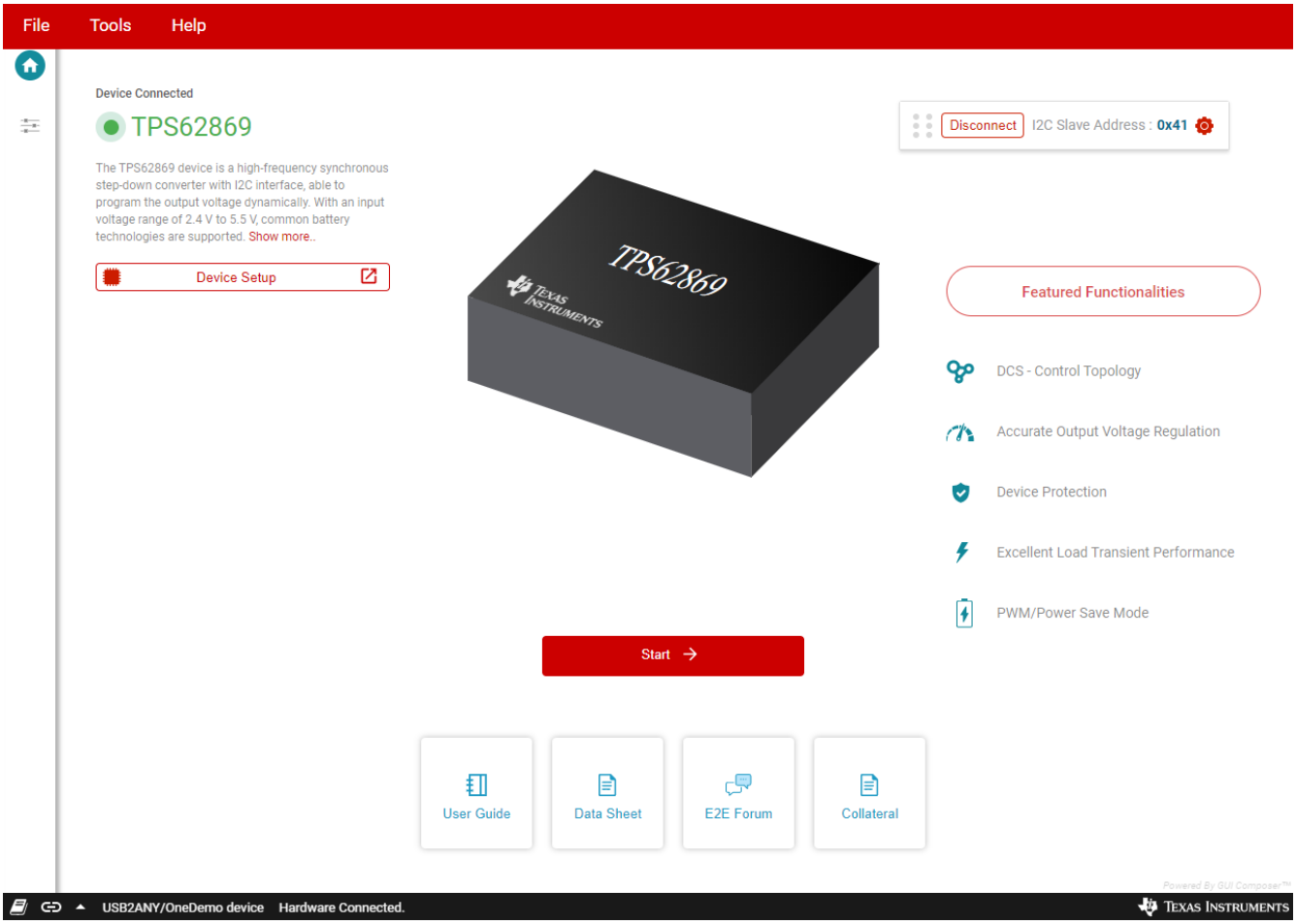

Figure 6-2. GUI Home Screen

6.3.2 Settings Screen

The Settings screen provides control over the output voltage and operating modes of the TPS62869. The Register Map at the bottom shows a register-wise view of all parameters. Here, single registers can be read or written to the device (if applicable). Refer to the register map in the TPS62869 2.4-V to 5.5-V Input, 6-A Synchronous Step-Down Converter Data Sheet for a detailed description of the TPS62869 registers.

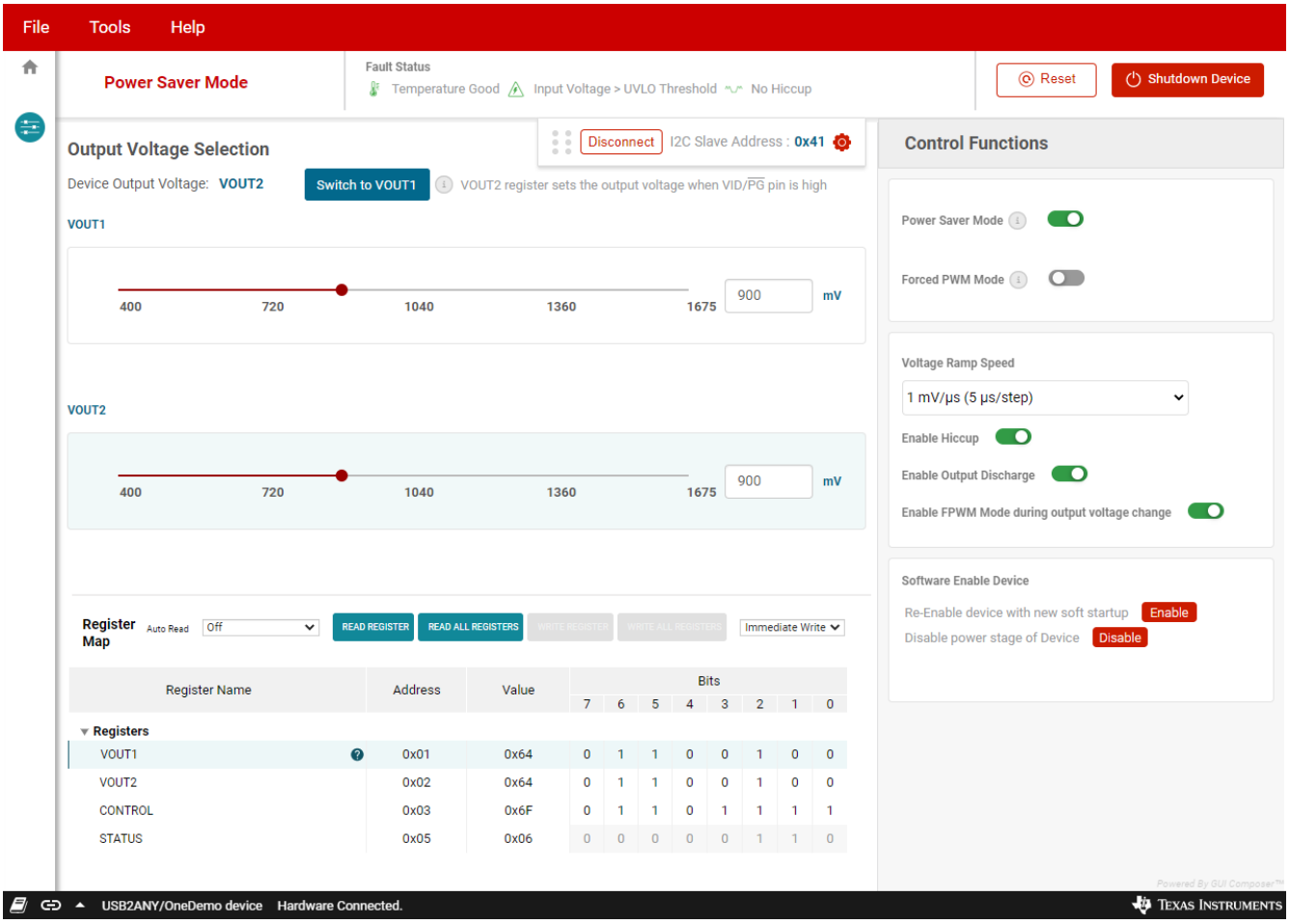

Figure 6-3. GUI Settings Screen

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2021) to Revision B (November 2021)	Page
• Updated *TPS628692* to *TPS628682*	1
• Updated title from *Setup* to *Hardware Setup*	2

Changes from Revision * (May 2021) to Revision A (March 2021)	Page
• Updated TPS62869EVM-118 Schematic	6

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