User's Guide

TPS92518EVM Dual Buck Controller Evaluation Module

ABSTRACT

This user's guide describes the specifications, board connection description, characteristics, operation, and use of the combined, two-board TPS92518 Evaluation Module (EVM). A complete schematic diagram, printed circuit board layouts, and bill of materials are included in this document.

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1 Description

The complete two-board TPS92518EVM solution provides a dual-channel, high-brightness LED current regulator which is configurable via a graphical user interface (GUI). It is designed to operate with an input voltage in the range of 6.5 V to 65 V. The EVM is setup for default output currents of 538 mA per channel, easily adjustable to different currents up to 1.65 A, for an LED stack between approximately 3 V to nearly 65 V. The TPS92518 provides high efficiency, high bandwidth, fast PWM dimming, SPI dimming, and adjustable off-time.

1.1 Typical Applications

This manual outlines the operation and implementation of the TPS92518 as a dual-channel LED current regulator with the specifications listed in Table 2-1. For applications with a different input voltage range or different output voltage range, refer to the TPS92518 data sheet (SLUSCR7). The TPS92518EVM-878 evaluation board is designed to be controlled by a TI microcontroller board, part number LEDSPIMCUEVM-879, available separately, although it can be controlled by any SPI-capable control system. Note that the TPS92518x supports a means to enable the part without SPI communication. By applying a voltage above the second threshold level, 23.6 V typical, on the ENABLE pin, the state of the LEDxEN register is bypassed. This allows a TPS92518 to be powered and operated using the default register values (for details, refer to the TPS92518 data sheet (SLUSCR7)).

1.2 Connector Description

Table 1-1 describes the connectors and Table 1-2 lists the test points on the EVM and how to properly connect, set up, and use the TPS92518EVM-878.

Table 1-1. Connector Descriptions

Connector	Label	Description
J1 and J18	VIN, GND	J1 connects power to channel 1 of the board, and J18 connects power to channel 2. The evaluation board is set up with both channel supplies connected through R15, so power connection can be to either J1 or J18 to power both channels from a single supply. The board silkscreen identifies power (one pin) and ground (two pins) connections on each connector.
J2 and J3	LED+, LED– and GND	J2 connects the channel 1 output to the LED load, and J3 connects the channel 2 output to a separate LED load. The leads to the LED load should be twisted and kept short to minimize voltage drop, inductance, and EMI. The board silkscreen identifies LED+ and LED– and GND.
J4	SPI control header	J4 allows attachment of a header cable for SPI control of the chip. The board silkscreen identifies GND, MISO, MOSI, SCK, and SSN.
J10 and J11	SPI control from an LEDSPIMCUEVM-879 controller board	J10 and J11 allow daisy-chaining TPS92518EVM-878 boards to each other with one LEDSPIMCUEVM-879 control board attached to the left-hand side of the left-most evaluation board for controlling the TPS92518. This interface allows control of the chip hardware enable line, PWM inputs to both channels, SPI lines, and hardware address lines for multiple SSN settings for systems that have multiple TPS92518EVM-878 boards controlled by a single LEDSPIMCUEVM-879 controller interface board.
J12 and J14	SPI MISO pullup resistor jumpers	J12 and J14 provide for two different values of pullup resistor to the MISO line, 2.2 kΩ and 4.7 kΩ provided on the evaluation board.
J13 and J6	PWM jumpers	J13 and J6 are jumpers provided to allow for PWM signals to the two channels to be generated from an LEDSPIMCUEVM-879 (when populated) or applied from an external source (when jumper is removed and the signal is connected to pin 1 one of the connector). J13 provides PWM to channel 1 of the chip, while J6 provides PWM to channel 2.
J9	SSN configuration jumper	J9 allows configuration of the SSN chip select line for use with multiple chips on the same SPI bus.

Table 1-1. Connector Descriptions (continued)

Connector	Label	Description
J8	MISO	This jumper enables configurations: shorting pins 5–6 sets the SPI communication architecture up for a single TPS92518 or the end point of a daisy chain of them, shorting 1–2 and 5–6 sets up for a TPS92518 in the middle of a daisy-chain, and shorting 3–4 and 5–6 provides for a star architecture.
J7	SPI DI out	If this jumper is closed, it allows multiple TPS92518 devices to be connected in a star configuration.
J10	Control connector	This connector allows the TPS92518 board to attach to a microcontroller, such as the LEDSPIMCUEVM-879.

Table 1-2. Test Points

Test Point	Description
Metal turrets	All metal turrets are grounds.
PWM1 and PWM2	The test points labeled PWM1 and PWM2 allow for external signal sources to control the TPS92518 hardware PWM dimming.
ENABLE	The test point labeled ENABLE near J10 allows for an external enable signal to control switching of the TPS92518.
VDIGI	The VDIGI test point allows for external application of power to the MISO pull-up resistors or monitoring of the pull-up voltage.
SW1 and SW2	The SW1 and SW2 test points provide locations to monitor the switch nodes of the two channels.
VIN	The VIN test point allows for external application of power to the digital system of the chip independent of the analog power supplies to either channel 1 or 2. On the evaluation board this is shorted to the analog supply by R16, so separate application of power is neither necessary nor useful without removal of R16.

2 Performance Specifications

Table 2-1. TPS92518 EVM Performance Specifications

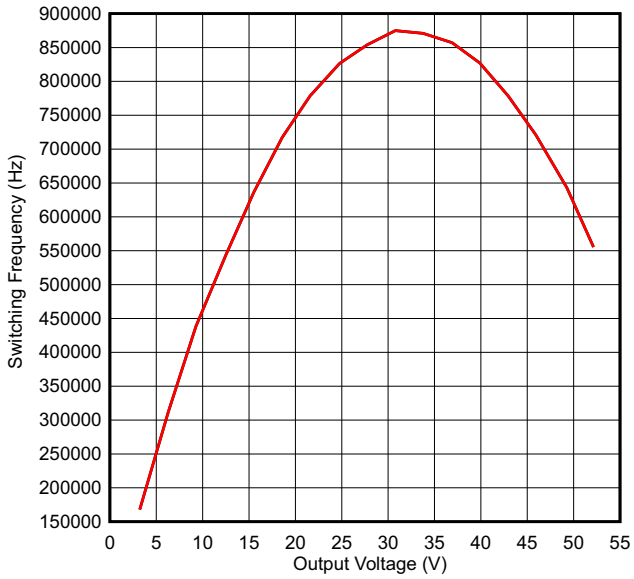
Parameter	Test Conditions	Min	Typ	Max	Units
Input Characteristics					
Voltage		6.5	14	65	V
Maximum Input Current				2.5	A
Output Characteristics					
Output Voltage, V_{LED}	Output/LED Voltage (absolute maximum)	0		65	V
	Output/LED Voltage (practical limit)			60	
Output Current, I_{LED}	Output current	0		1.65	A
	Default Output Current (Registers = 127/255)			0.538	
Dimming Methods					
Analog	LEDx_PKTH_DAC register = 0 to 255		yes		
PWM	Use PWMx pin input		yes		
Shunt FET	Use external FET, program LEDx_MAXOFF_DAC register as per datasheet outline		yes		

Table 2-1. TPS92518 EVM Performance Specifications (continued)

Parameter	Test Conditions	Min	Typ	Max	Units
Systems Characteristics					
Switching frequency	Switching Frequency (f_{SW}) Range	1		2000	kHz
Peak efficiency				95	%
Operating temperature		–40	25	125	°C

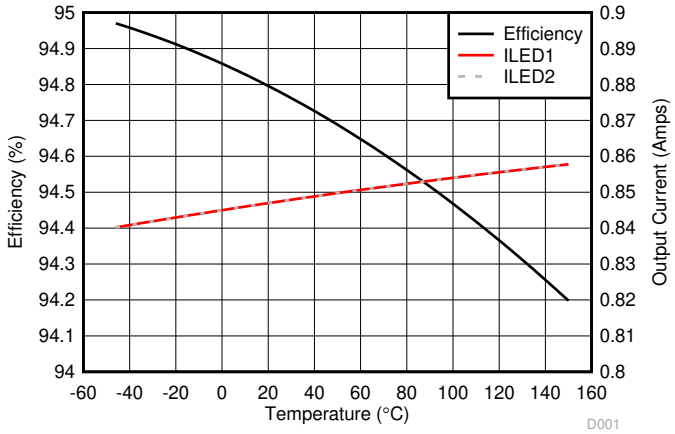
3 Performance Data and Typical Characteristic Curves

Figure 3-1 through Figure 3-4 illustrate the performance data and typical characteristic curves.



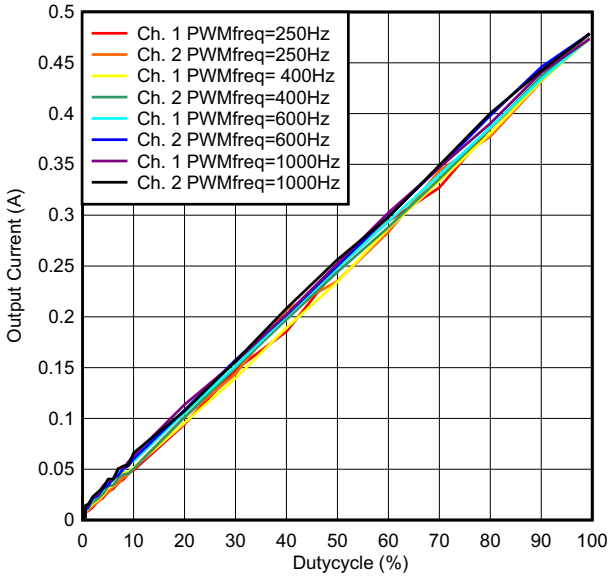
Conditions: V_{IN} 50 V, peak threshold = 50, minimum off-time = 127

Figure 3-1. Frequency vs Output Voltage



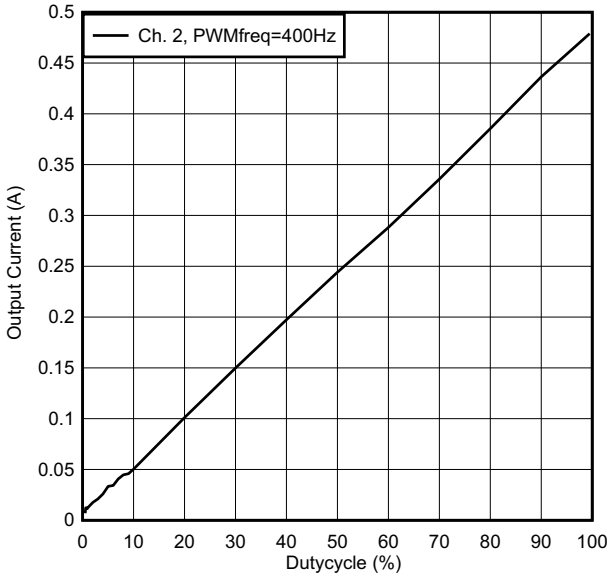
Conditions: V_{IN}= 50 V, V_{LED} = 24.7 V, peak threshold = 120, minimum off-time = 127

Figure 3-2. Efficiency Over Temperature at Different Peak Threshold Settings



V_{IN} = 12 V, V_{LED} = 3 V, peak threshold = 127, off time = 127

Figure 3-3. PWM Dimming, Multiple PWM Frequencies, Both Channels



V_{IN} = 12 V, V_{LED} = 3 V, peak threshold = 127, off time = 127

Figure 3-4. Single-Channel PWM Dimming at 400 Hz

3.1 Startup Waveforms

3.1.1 Startup After SPI Enable Command

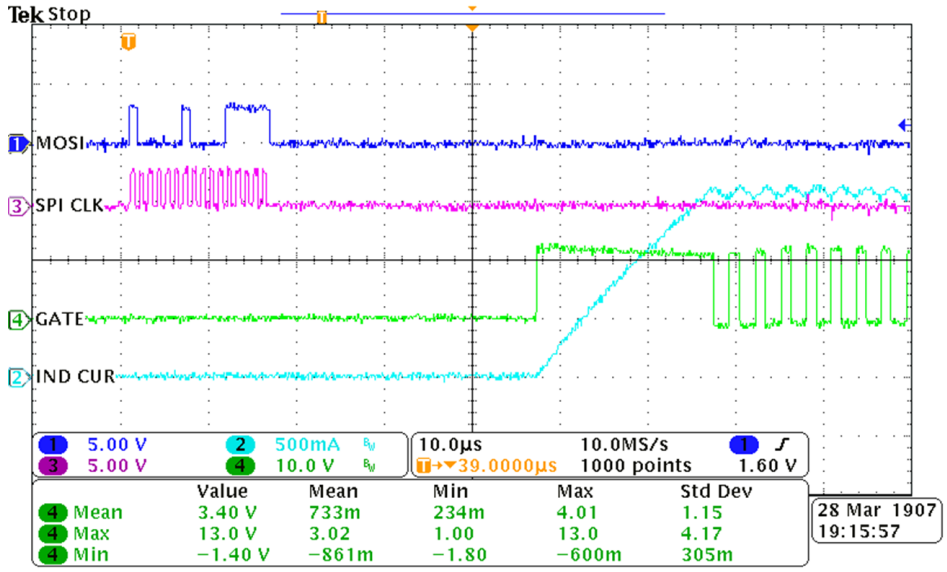


Figure 3-5. SPI Setting Output Enable Bit and Subsequent Switching Initiation

3.1.2 Startup on Hardware Enable Pin Transition

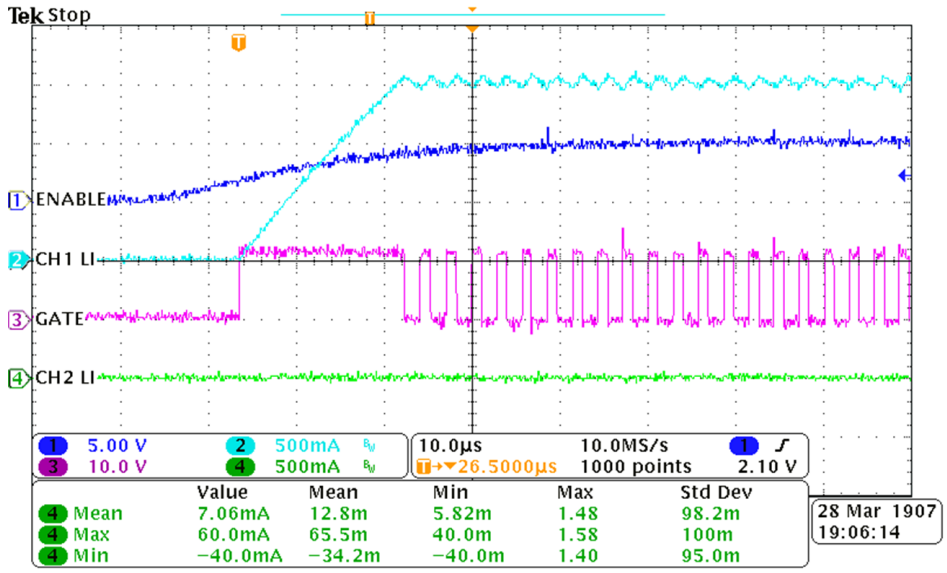


Figure 3-6. Hardware PWM Enable Pulled High, Triggering Switching

3.2 Shutdown Waveforms

3.2.1 Shutdown After SPI Disable

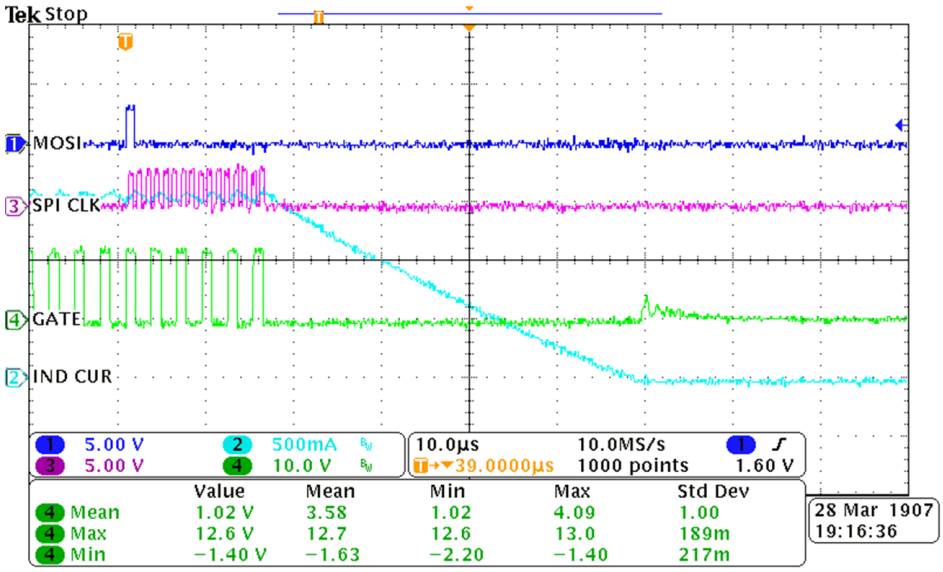


Figure 3-7. SPI Clearing Output Enable Bit and Subsequent Switching Shutdown

3.2.2 Shutdown After Hardware Enable Pin Transition

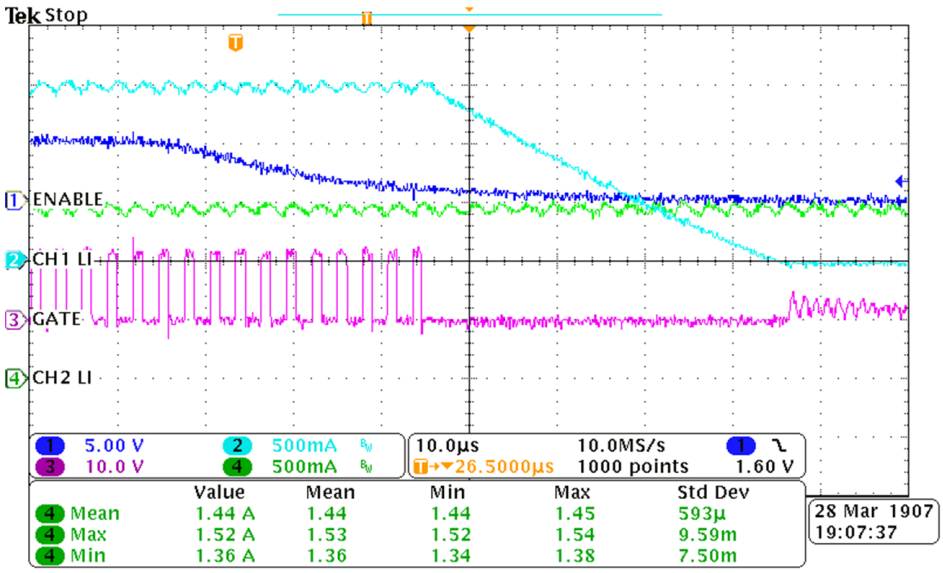
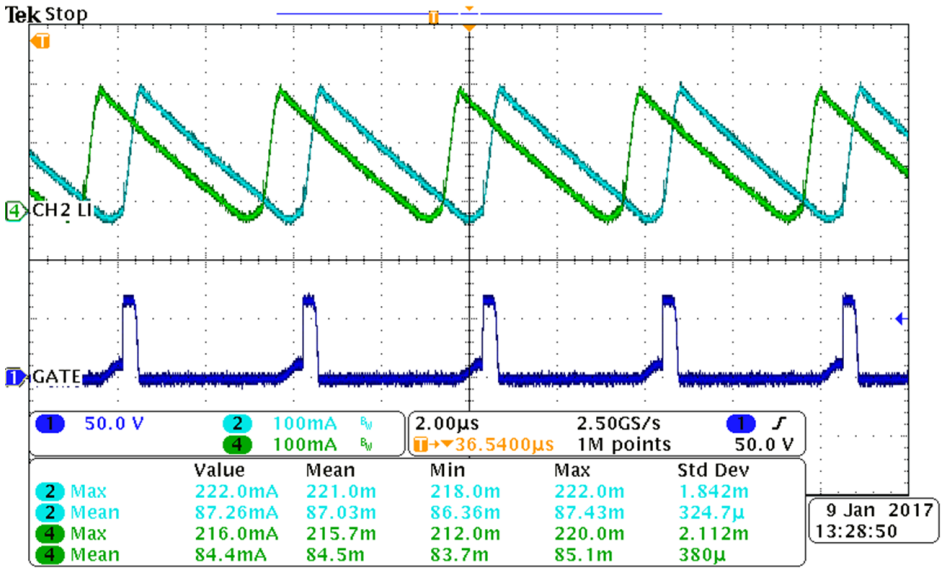


Figure 3-8. Hardware PWM Enable Pulled Low, Triggering Chip Shutdown

3.3 Current Sharing

The TPS92518 device can be set up to share current with both channels driving a single load.

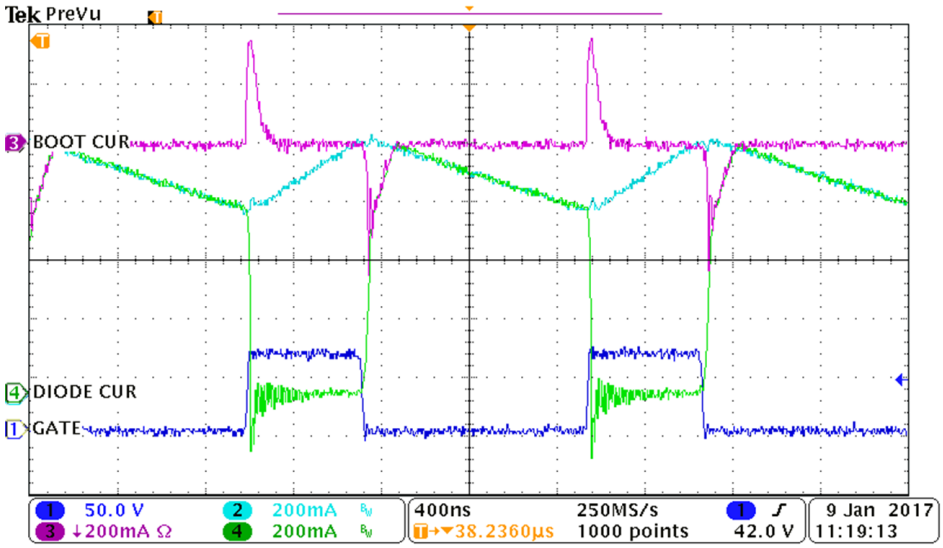


V_{IN} = 65 V, driving 1 LED for a V_{LED} of 3.0062 V, with a peak threshold = 45 to get approximately a 225-mA LED current, showing max and mean inductor currents on channels 1 and 2

Figure 3-9. Current Sharing

3.4 Diode and Boot Capacitor Current

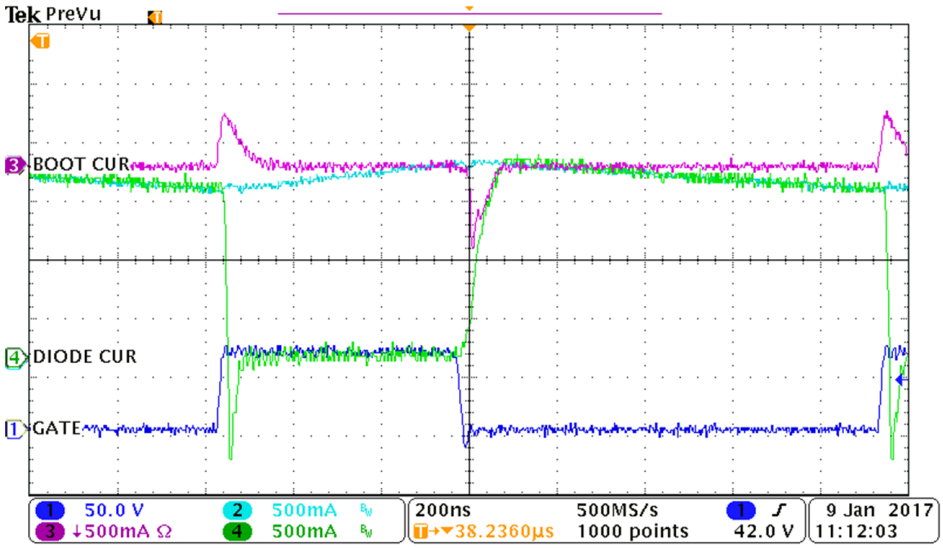
3.4.1 Diode, Inductor, and Boot Capacitor Current at Low Output Current



Showing inductor current into the LED and current flow through the catch diode and boot capacitor used for supplying gate drive power. V_{IN} = 65 V, V_{LED} = 23 V, T_{OFF} register setting = 50, peak threshold register setting = 1

Figure 3-10. Switch Node Current

3.4.2 Diode, Inductor, and Boot Capacitor Current at High Output Current



Showing inductor current into the LED and current flow through the catch diode and boot capacitor used for supplying gate drive power. V_{IN} = 65 V, V_{LED} = 23 V, T_{OFF} register setting 50, peak threshold register setting = 1

Figure 3-11. Switch Node Current

3.4.3 Shunt FET Dimming

Shunt FET dimming is simple with the TPS92518. Short leads between the evaluation board and the LED load boards are important to prevent V_{LED} overshoot. Locating the shunt FET on or near the LED load board also helps to reduce V_{LED} overshoot. Adding an appropriately rated diode from the LED+ line that conducts back to the positive V_{IN} input will clamp voltage overshoot.

Note

There is no provision for mounting such a diode on the board: it must be soldered into the wiring used to connect the shunt FET into the circuit.

Similarly, repopulating R17 and C21 with different values will also protect the VLED pin from overshoots. The Figure 3-12, green high-lighted area, illustrates the circuitry modifications for shunt FET dimming if high overshoots are being seen. Adding/increasing the resistance at R17 and greatly reducing C21, OR adding a diode (shown as Dshunt) back to VIN are proven solutions. If adding R17 ensure a small C21 is used, like 220 pF, to allow the feedback enough bandwidth for correct output voltage sensing.

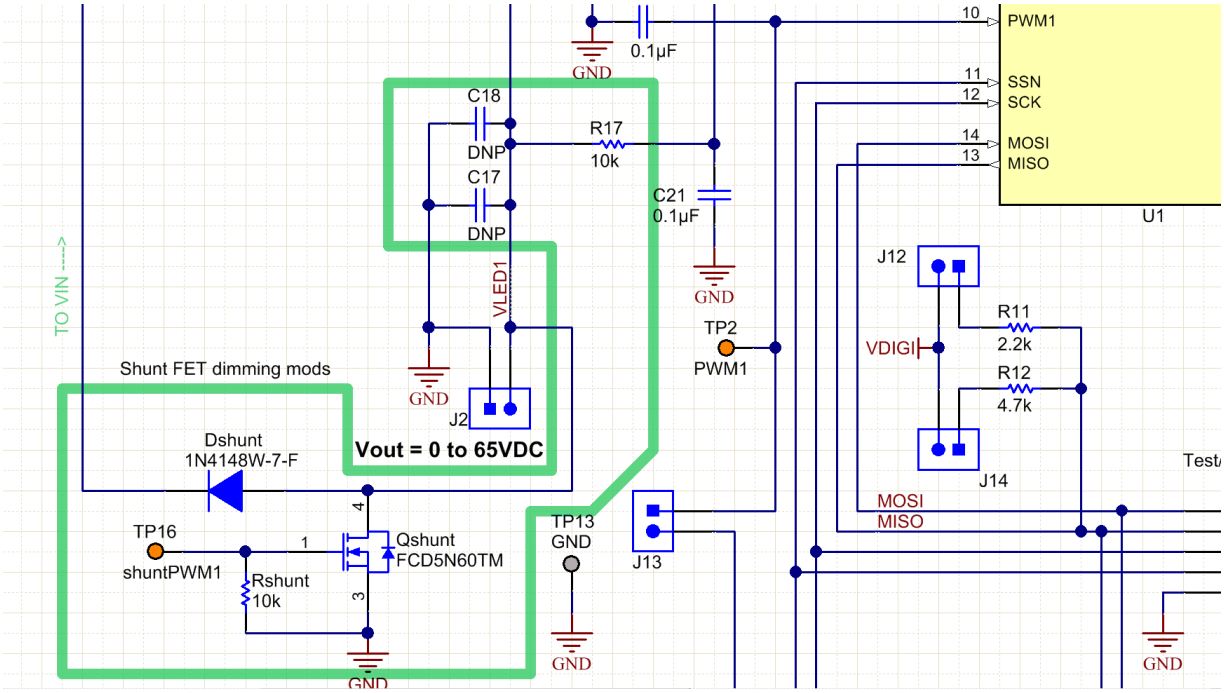


Figure 3-12. Additional Circuitry Required for Shunt FET Dimming

3.4.4 Undervoltage Lockout Description

The TPS92518 can be set up with undervoltage lockout protection with the ability to change the turn-on threshold and hysteresis, by populating a resistive divider that is unpopulated on the evaluation board. This involves loading R1 and changing the value of R2, and possibly populating C28. For details refer to the TPS92518 data sheet (SLUSCR7).

4 Schematic, PCB Layout, and Bill of Materials

This section contains TPS92518EVM-878 schematics, PCB layouts, and bill of materials (BOM).

4.1 Schematic

Figure 4-1 illustrates the TPS92518EVM-878 schematic.

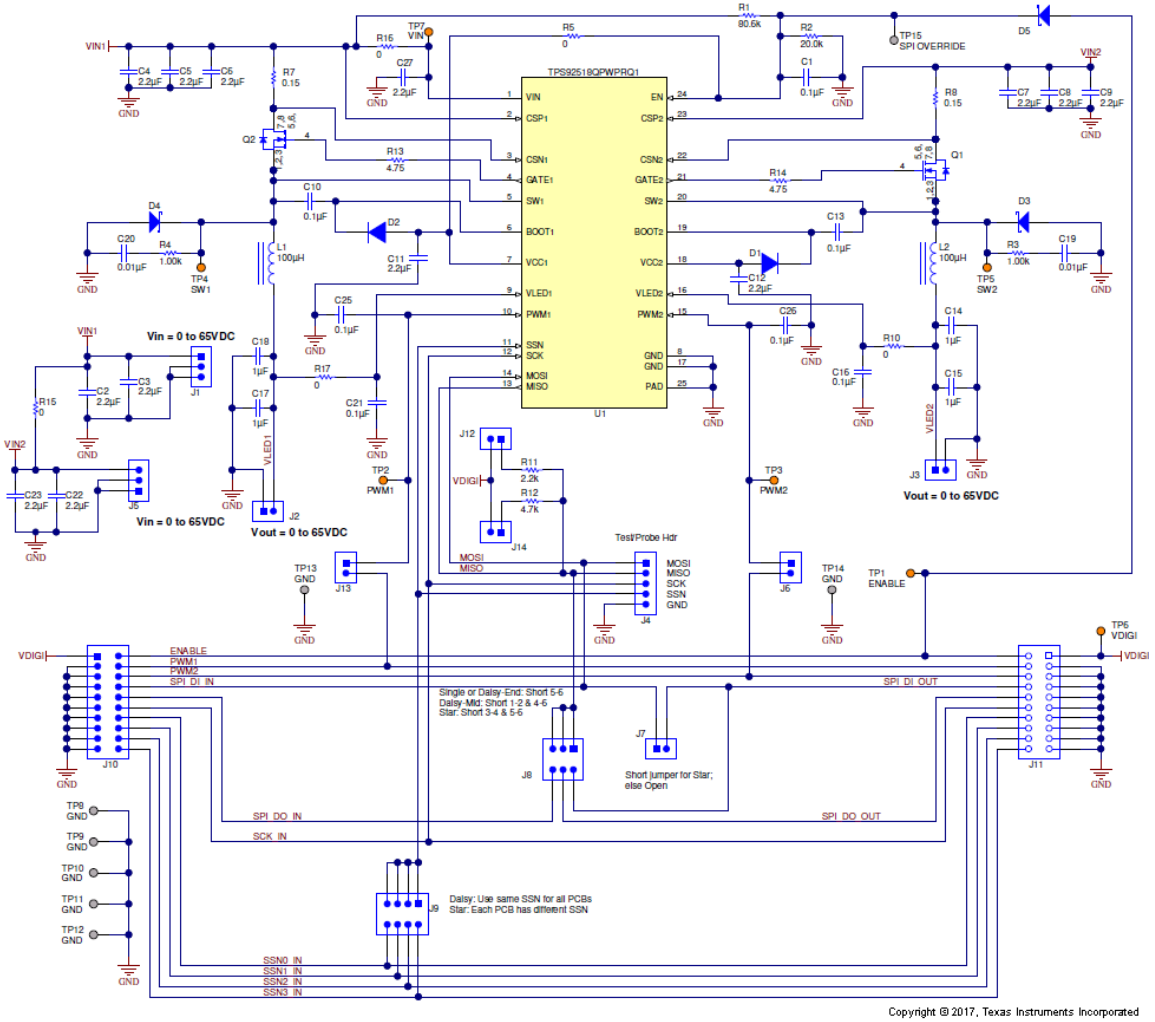


Figure 4-1. TPS92518EVM-878 Schematic

4.2 Layout

Figure 4-2 and Figure 4-3 illustrate the top and bottom side TPS92518EVM-878 PCB layouts.

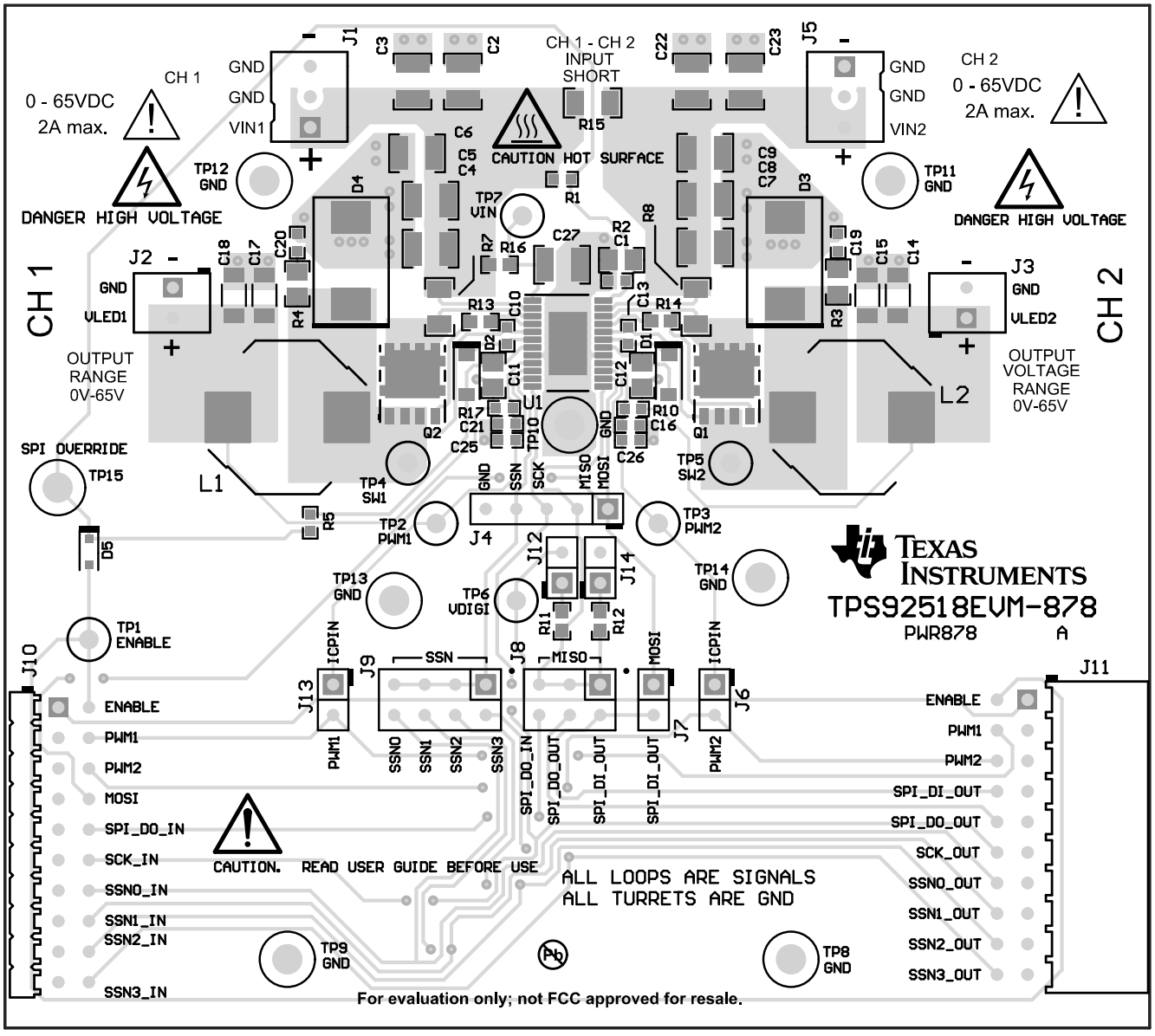


Figure 4-2. TPS92518EVM-878 Top Side

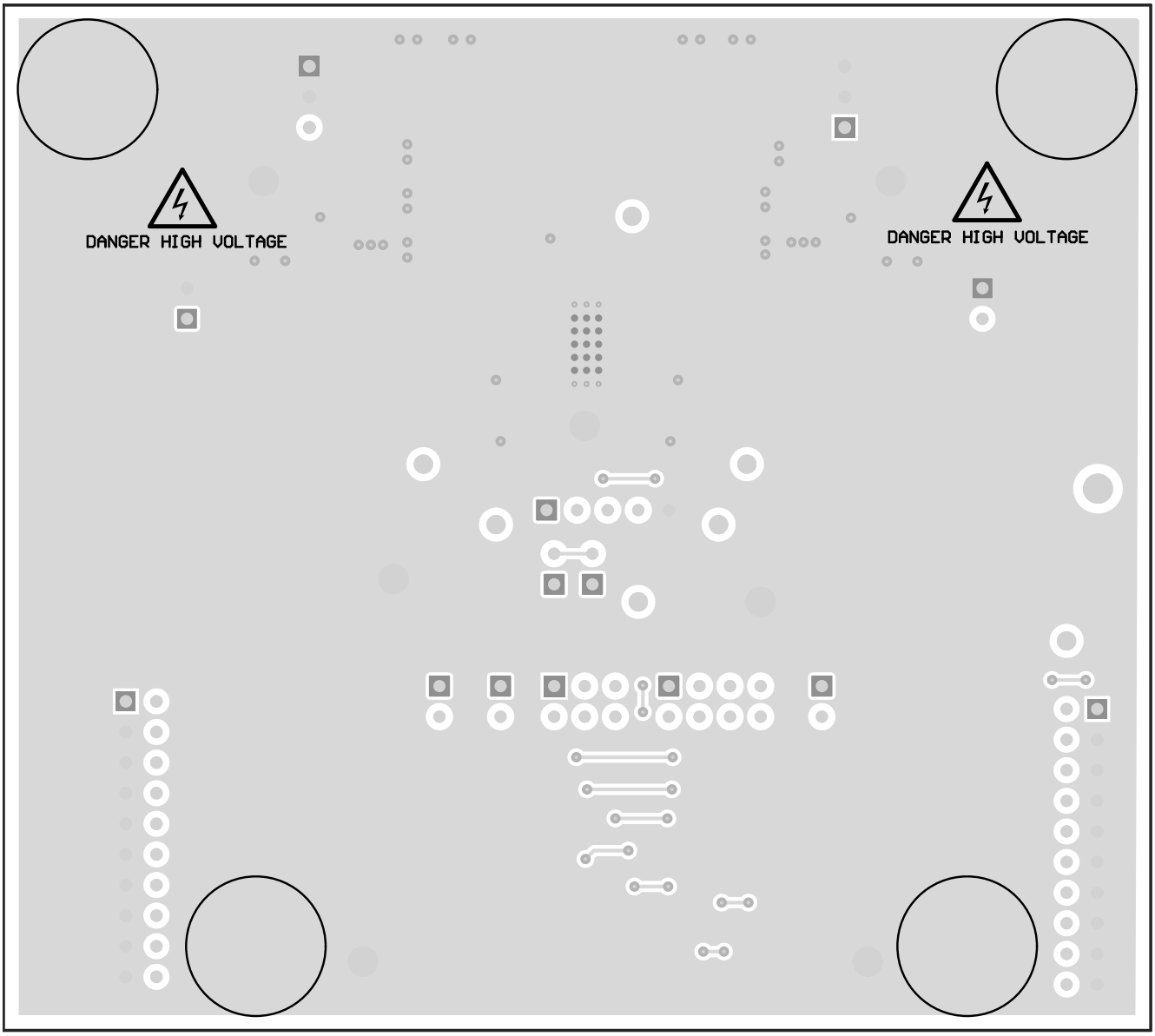


Figure 4-3. TPS92518EVM-878 Bottom Side

4.3 Bill of Materials

Table 4-1 lists the TPS92518EVM-878 bill of materials.

Table 4-1. TPS92518EVM-878 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
(none)	1		Printed Circuit Board		PWR878	Any
C2, C3, C4, C5, C6, C7, C8, C9, C22, C23, C27	11	2.2 µF	Capacitor, Ceramic, 2.2 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1,		CGA6N3X7R2A225K230AB	TDK
C10, C13	2	0.1 µF	Capacitor, Ceramic, 0.1 µF, 16 V, ±10%, X7R, 0603	0603	GCM188R71C104KA37D	Murata
C11, C12	2	2.2 µF	Capacitor, Ceramic, 2.2 µF, 16 V, ±10%, X7R, 0805	0805	GCM21BR71C225KA64L	Murata
C14, C15, C17, C18	4	1 µF	Capacitor, Ceramic, 1 µF, 100 V, ±10%, X7R, 1206	1206	GCM31CR72A105KA03L	Murata
D1, D2	2	100 V	Diode, Switching, 100 V, 0.2 A, SOD-123	SOD-123	MMSD4148T1G	ON Semiconductor
D3, D4	2	100 V	Diode, Schottky, 100 V, 3 A, SMC	SMC	SS3H10HE3_A/I	Vishay-Siliconix
D5	1	100 V	Diode, Schottky, 100 V, 0.25 A, SOD-323F	SOD-323F	BAT46WJ,115	NXP Semiconductor
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 mm x 0.20 mm, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J5	2		Header, 2.54 mm, 3 x 1, TH	Header, 2.54 mm, 3 x 1, TH	22-11-2032	Molex
J2, J3	2		Header, 2.54 mm, 2 x 1, Vertical, TH	Header, 2.54 mm, 2 x 1, TH	22-23-2021	Molex
J4	1		Header, 100 mil, 5 x 1, Gold, TH	5 x 1 Header	TSW-105-07-G-S	Samtec
J6, J7, J12, J13, J14	5		Header, 100 mil, 2 x 1, Gold, TH	2 x 1 Header	TSW-102-07-G-S	Samtec
J8	1		Header, 100 mil, 3 x 2, Gold, TH	3 x 2 Header	TSW-103-07-G-D	Samtec
J9	1		Header, 100 mil, 4 x 2, Gold, TH	4 x 2 Header	TSW-104-07-G-D	Samtec
J10	1		Header, 2.54 mm, 10 x 2, Tin, R/A, TH	Header, 2.54 mm, 10 x 2, R/A, TH	TSW-110-08-T-D-RA	Samtec
J11	1		Receptacle, 2.54 mm, 10 x 2, Gold, R/A, TH	Receptacle, 2.54 mm, 10 x 2, R/A, TH	SSW-110-02-G-D-RA	Samtec
L1, L2	2	100 µH	Inductor, Shielded, Ferrite, 100 µH, 2 A, 0.108 ohm, AEC-Q200 Grade 0, SMD	12.8 x 12.5 mm	MDH12577C-101MA=P3	Murata
L1, L2	0	100 µH	Alternate: Inductor, Ferrite, 100 µH, 2.2A, 0.12 ohm, AEC-Q200 Grade 0, SMD	12.8 x 12.0 mm	7847709101	Wurth
Q1, Q2	2	100 V	MOSFET, N-CH, 100 V, 20 A, AEC-Q101, 8-PowerVDFN	8-PowerVDFN	STL8N10LF3	STMicroelectronics
R2	1	20.0 kΩ	Resistor, 20.0 kΩ, 1%, 0.125 W, 0805	0805	CRCW080520K0FKEA	Vishay-Dale
R7, R8	2	0.15 Ω	Resistor, 0.15 Ω, 1%, 1/2W, 1206	1206 (3216 Metric)	ERJ-8BSFR15V	Panasonic Electronic Components
R10, R16, R17	3	0 Ω	Resistor, 0 Ω, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R11	1	2.2 kΩ	Resistor, 2.2 kΩ, 5%, 0.1 W, 0603	0603	CRCW06032K20JNEA	Vishay-Dale
R12	1	4.7 kΩ	Resistor, 4.7 kΩ, 5%, 0.1 W, 0603	0603	CRCW06034K70JNEA	Vishay-Dale
R13, R14	2	4.75 Ω	Resistor, 4.75 Ω, 1%, 0.1 W, 0603	0603	CRCW06034R75FKEA	Vishay-Dale
R15	1	0 Ω	Resistor, 0 Ω, 5%, 0.25 W, 1206	1206	CRCW12060000Z0EA	Vishay-Dale

Table 4-1. TPS92518EVM-878 Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
SH-J6, SH-J8, SH-J9, SH-J12, SH-J13	5		Shunt, 2.54 mm, Gold, Black	Shunt, 2.54 mm, Black	60900213421	Wurth Elektronik
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7	Orange	Test Point, Compact, Orange, TH	Orange Compact Testpoint	5008	Keystone
TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15	8	Double	Terminal, Turret, TH, Double	Keystone1502-2	1502-2	Keystone
U1	1		65V Automotive Dual Buck LED Controller with SPI Interface, PWP0024J (TSSOP-24)	PWP0024J	TPS92518QPWPRQ1	Texas Instruments
C1, C16, C21, C25, C26	0	0.1 µF	Capacitor, Ceramic, 0.1 µF, 16 V, ±10%, X7R, 0603	0603	GCM188R71C104KA37D	Murata
C19, C20	0	0.01 µF	Capacitor, Ceramic, 0.01 µF, 100 V, ±10%, X7R, 0603	0603	GCM188R72A103KA37D	Murata
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
R1	0	80.6 kΩ	Resistor, 80.6 kΩ, 1%, 0.1 W, 0603	0603	CRCW060380K6FKEA	Vishay-Dale
R3, R4	0	1.00 kΩ	Resistor, 1.00 kΩ, 1%, 0.125 W, 0805	0805	CRCW08051K00FKEA	Vishay-Dale
R5	0	0 Ω	Resistor, 0 Ω, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale

5 Software

5.1 TPS92518 Demonstration Kit Software Installation

Click on *TPS92518 Demonstration Kit* Installer.exe, right click, and click 'Run As Administrator'. Click ‘yes’ when *Windows Account Control* asks to allow the program to make changes to the computer.

The evaluation software screen shows:

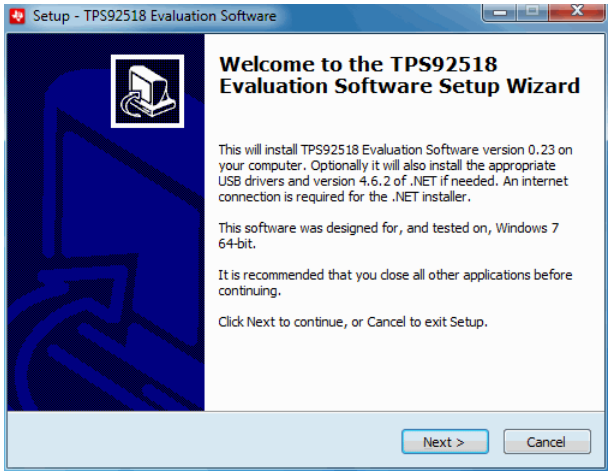


Figure 5-1. Setup Screen 1

Click the **Next >** button to install.

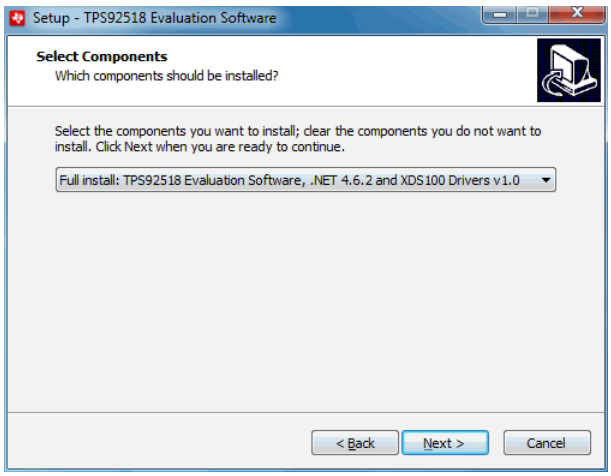


Figure 5-2. Setup Screen 2

Click the **Next >** button.

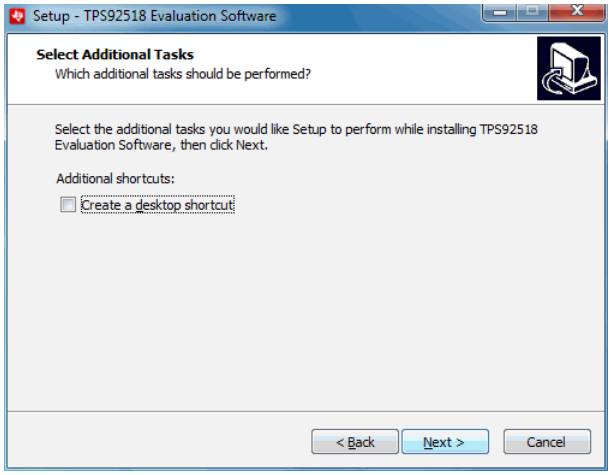


Figure 5-3. Setup Screen 3

Click the **Next >** button.

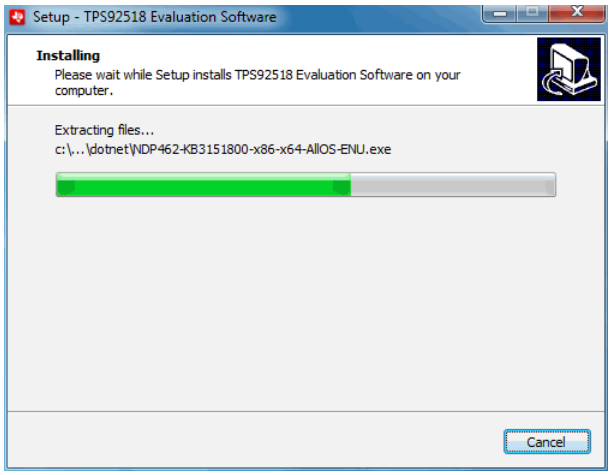


Figure 5-4. Setup Screen 4

Wait for it to finish extracting and installing files.

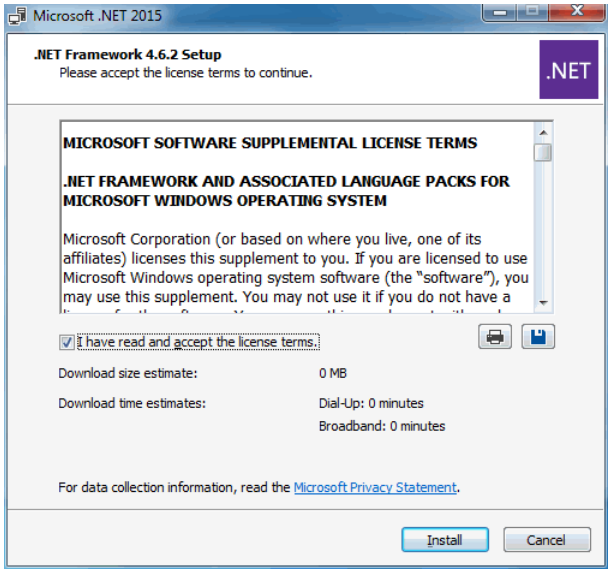


Figure 5-5. Setup Screen 5

Check the box stating you accept the license terms and click the **Install >** button.

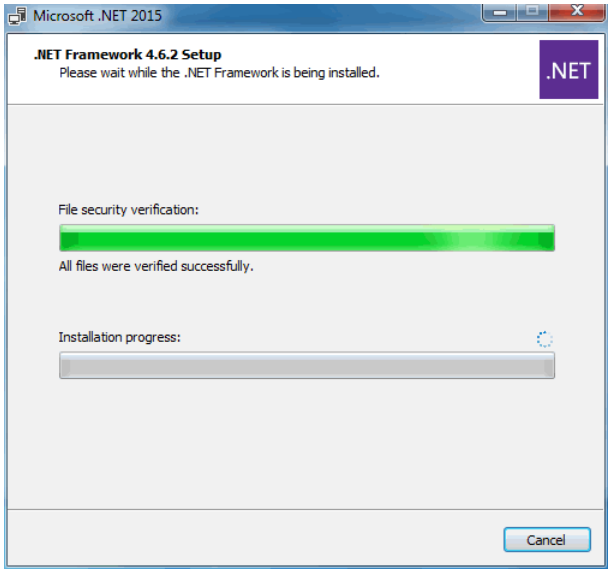


Figure 5-6. Setup Screen 6

It may be necessary to stop other programs using Microsoft® .NET Framework® during the installation process. Select **Yes**, if asked.

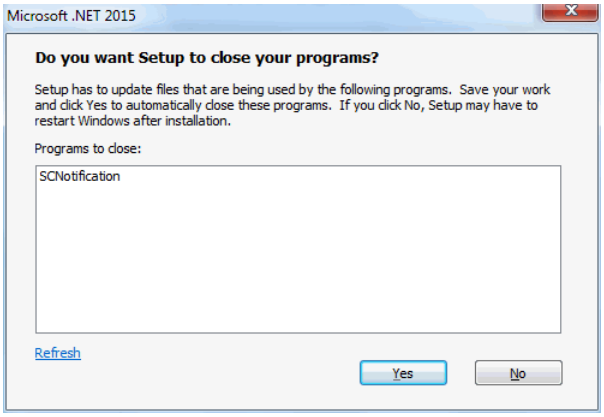


Figure 5-7. Setup Screen 7

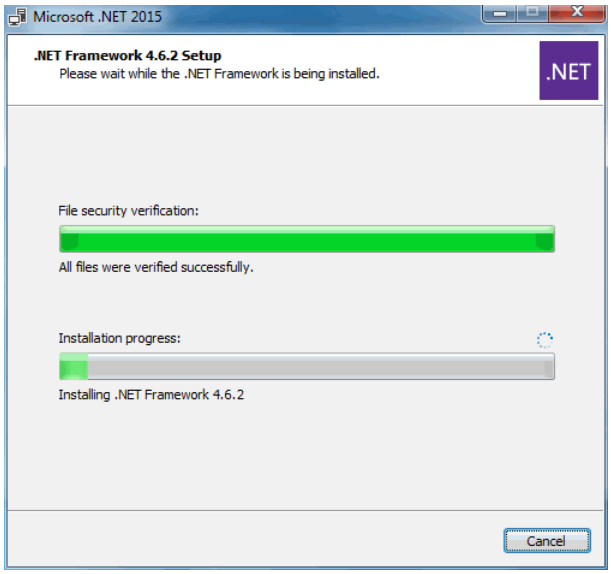


Figure 5-8. Setup Screen 8

Wait for .NET to download, verify, and install.

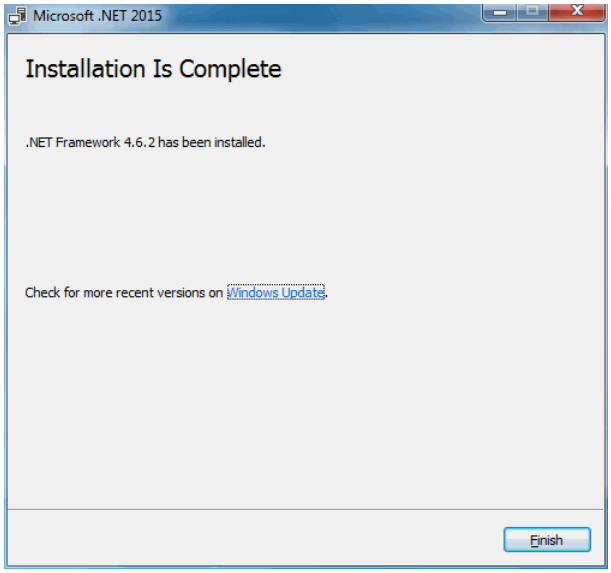


Figure 5-9. Setup Screen 9

Click the **Finish >** button.

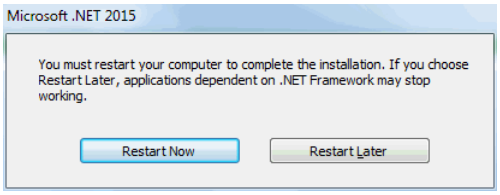


Figure 5-10. Setup Screen 10

Click on the **Restart Now** button.

5.1.1 Windows 10

Some versions of Windows 10 require a few extra steps to install unsigned drivers. A message that states the computer cannot complete the driver installation, requires the following steps. These steps allow the one-time installation of an unsigned driver.

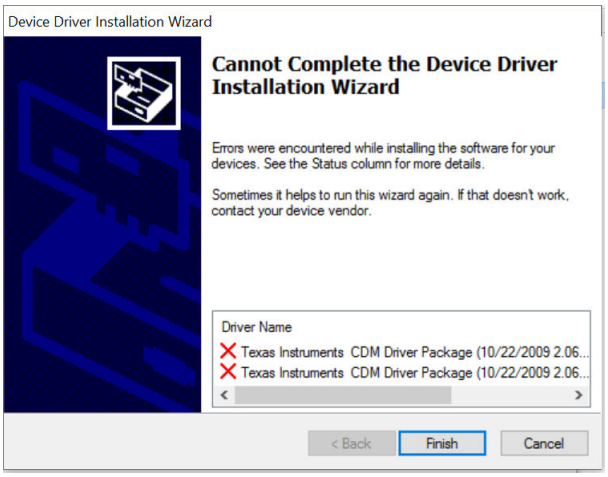


Figure 5-11. Unsigned driver error screen for Windows 10

1. Go to the Start menu and select **Settings**.

2. Click **Update and Security**.
3. Click **Recovery**.
4. Click **Restart now** under **Advanced Startup**.
5. Click **Troubleshoot**.
6. Click **Advanced Options**.
7. Click **Startup Settings**.
8. Click on **Restart**.
9. On the Startup Settings screen press F7 to disable driver signature enforcement.

Your computer will restart, allowing you to install unsigned drivers. You will have to repeat the entire reinstallation process. As .NET has already been installed in the previous installation, it will tell you that installing .NET failed. Close that window and continue. After the installer starts to install the drivers it will ask you twice if you wish to use unsigned drivers. Click on "install unsigned drivers" both times. On restarting a second time, the computer will return to requiring all drivers to be digitally signed in the future, unless this list is repeated.

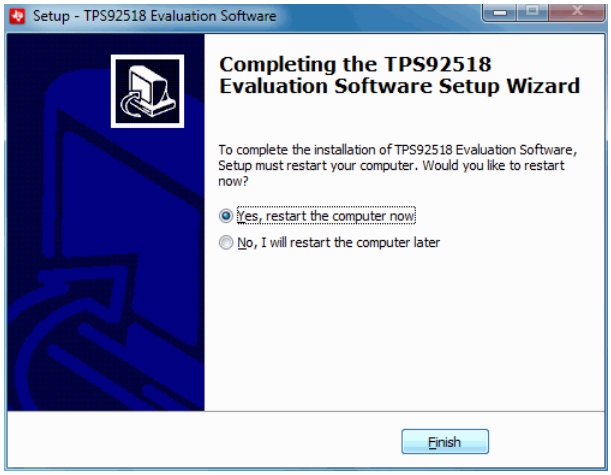
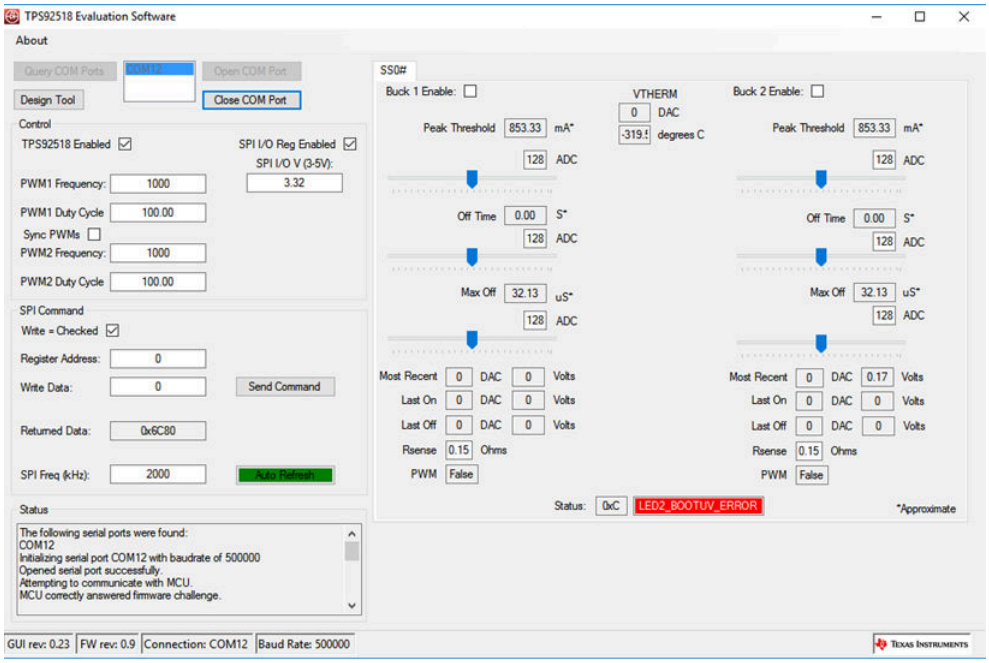


Figure 5-12. Setup Screen 11

Click on the **Finish >** button.

At this point the software should be ready to use. Click on the TI *TPS92518 Demonstration Kit* icon.



Quick Start: Provide input power of 6.5 V to 65 V to VIN, provide LED loads with output voltages of between 2 V and 64 V to the two output channels. Next click on the *TPS92518 Enabled* box so it is checked, then on the *Buck 1 Enable:* and *Buck 2 Enable:* boxes so they are checked. The integrated circuit should start switching on each channel and regulating current to the LED loads.

Design Customization and GUI Operation: Access to key TPS92518 registers is provided via the GUI main window. Each channel **Peak Threshold**, **Off Time** and **Maximum Off-time** can be adjusted using the respective slider. Minimum limits are enforced in the GUI for the Off-Time and Maximum Off-time as these values should not be set < 10 except under specific and controlled conditions. (see the datasheet section: Off-Time Thresholds - LEDx_TOFF_DAC and LEDx_MAXOFF_DAC) The registers can still be set manually to lower values via the SPI Command section of the GUI. The sliders can be moved and the affect on the output current and switching frequency observed.

For a specific design configuration, the **Design Tool** button can be selected. This opens a simple TPS92518 design calculator window. Design Parameters can be entered and adjusted. Component and register values will be calculated. This calculator can be used to aid in any TPS92518 design, and is not just for use with the EVM.

For each slider adjustment an estimation of the relevant parameter value is also shown. For the peak current estimate, the value of the sense resistor can be set in the area below the sliders. (default is the actual EVM value of 0.15 Ohms) The estimated off-time and maximum off-times are also updated and reflect the current LED output voltage as measured by the TPS92518x internal ADC.

In the GUI **Control** section, the TPS92518 enable pin voltage can be controlled via the enable check box. The GUI also provides the ability to create PWM dimming signals. A PWM duty cycle and frequency can be set creating the corresponding signal at the TPS92518 PWMx pin. In normal operation the PWM duty cycle must be left at 100% to disable PWM dimming.

Registers may also be written manually via the **SPI Command** section. By using the TPS92518 datasheet *Registers* section as a guide, specific registers can be manually read and written. To preform a register write, set the write check-box. Un-check the box for a read. When reading and writing manually it is best to disable the *Auto Refresh* of the registers by toggling the feature via the 'Auto Refresh' box. Once the register value and write data (if applicable) are set, select the *Send Command* button. Due to the nature of a SPI bus operation, read commands must be sent twice; once to load the read command and another time to clock out the requested data.

6 Use of LEDSPIMCUEVM-879 Microcontroller Board for SPI Communications with the TPS92518

The LEDSPIMCUEVM-879 evaluation board is available separately to be used with TI's *TPS92518 Bench Evaluation Software*. It comes with firmware installed that converts the software settings into SPI and hardware-generated PWM signals to drive the TPS92518. It is set up correctly as packaged, but make sure that jumpers J6, J7, J8, and J9 are all shorted. These provide the power for the SPI pullup hardware, the PWM signals, and the enable signal to the TPS92518. Reprogramming the LEDSPIMCUEVM-879 is beyond the scope of this document, and firmware for reflashing the existing board is not supplied. The board has DC isolation between the USB section and the TPS92518 driver section, and voltage translators to handle the I/O logic level requirements of the TPS92518. Schematics are supplied as a guide to determining if the microcontroller board has been damaged and is not communicating correctly with the TPS92518 evaluation board.

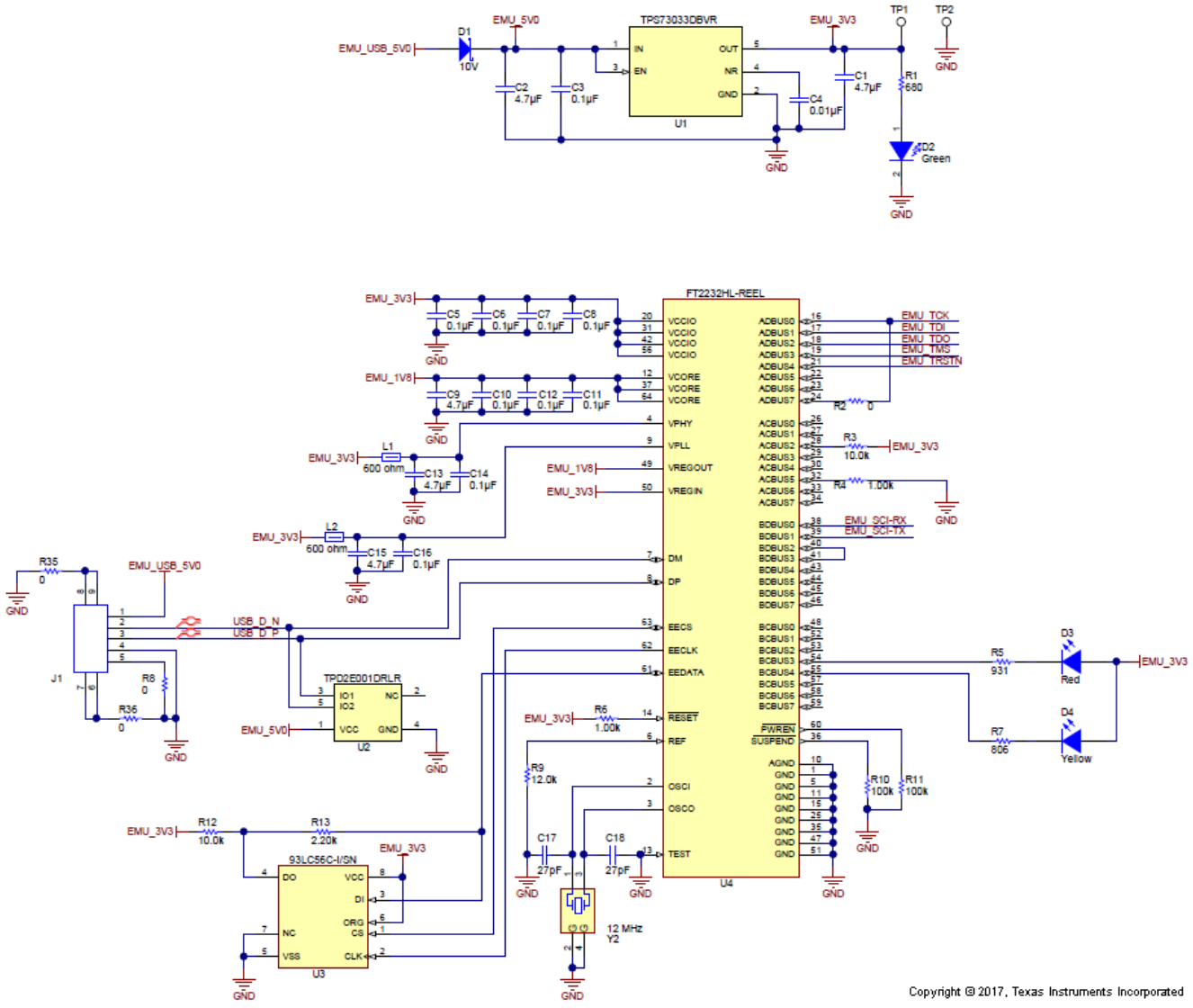


Figure 6-1. LEDSPIMCUEVM-879 Schematic, Page 1

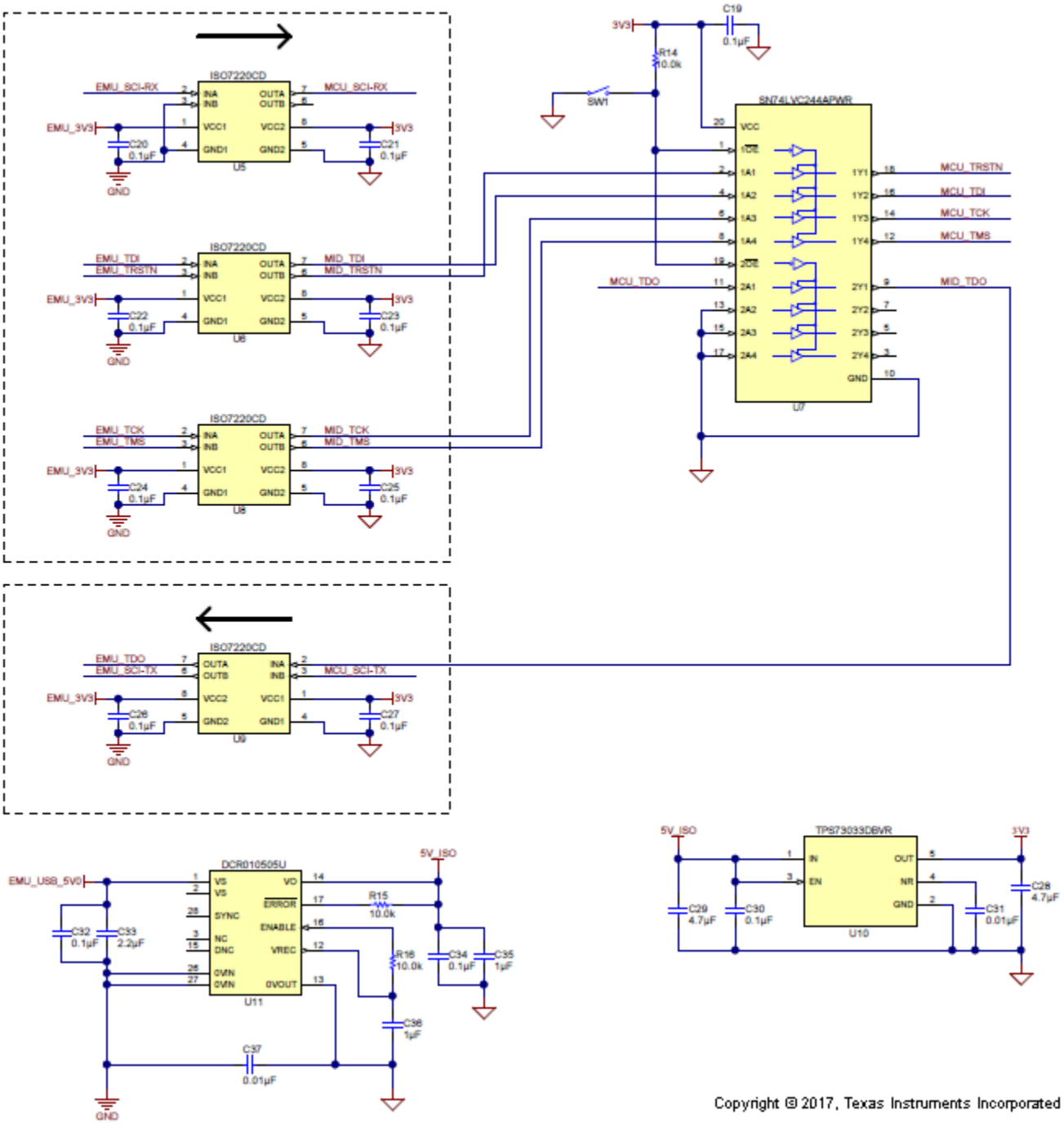


Figure 6-2. LEDSPIMCUEVM-879 Schematic, Page 2

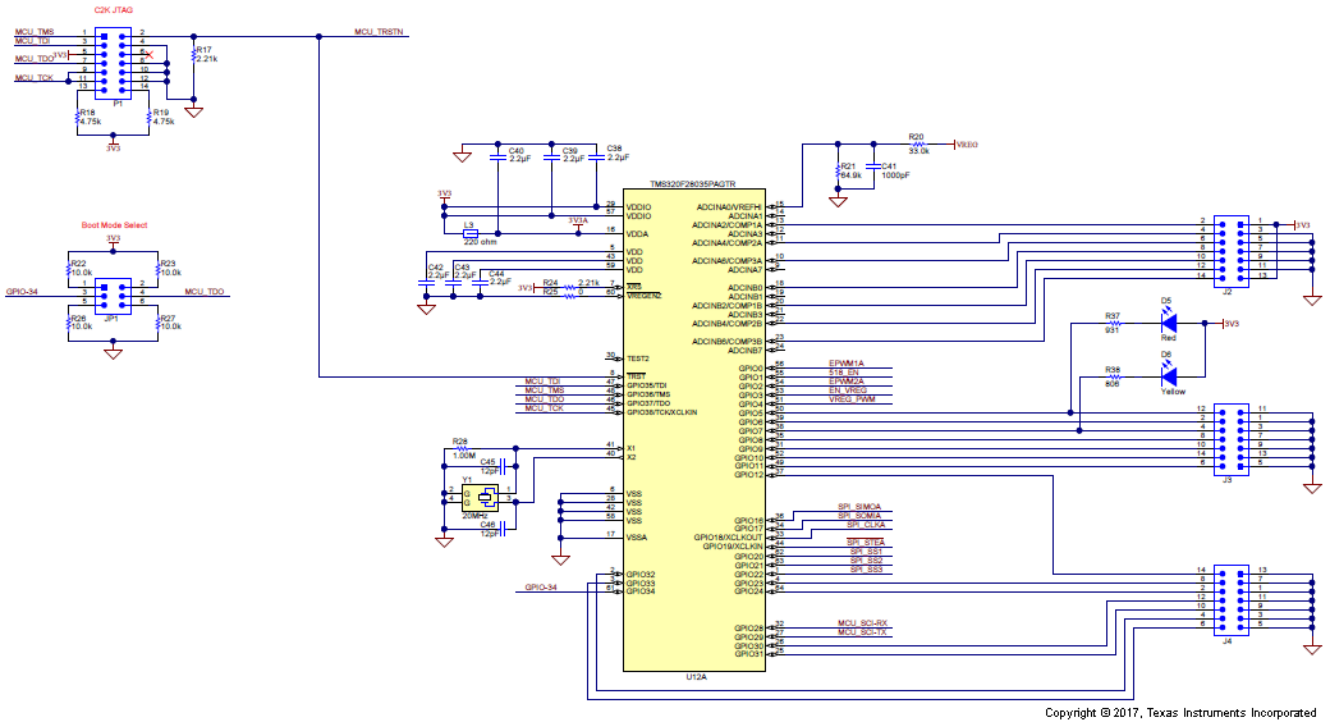


Figure 6-3. LEDSPIMCUEVM-879 Schematic, Page 3

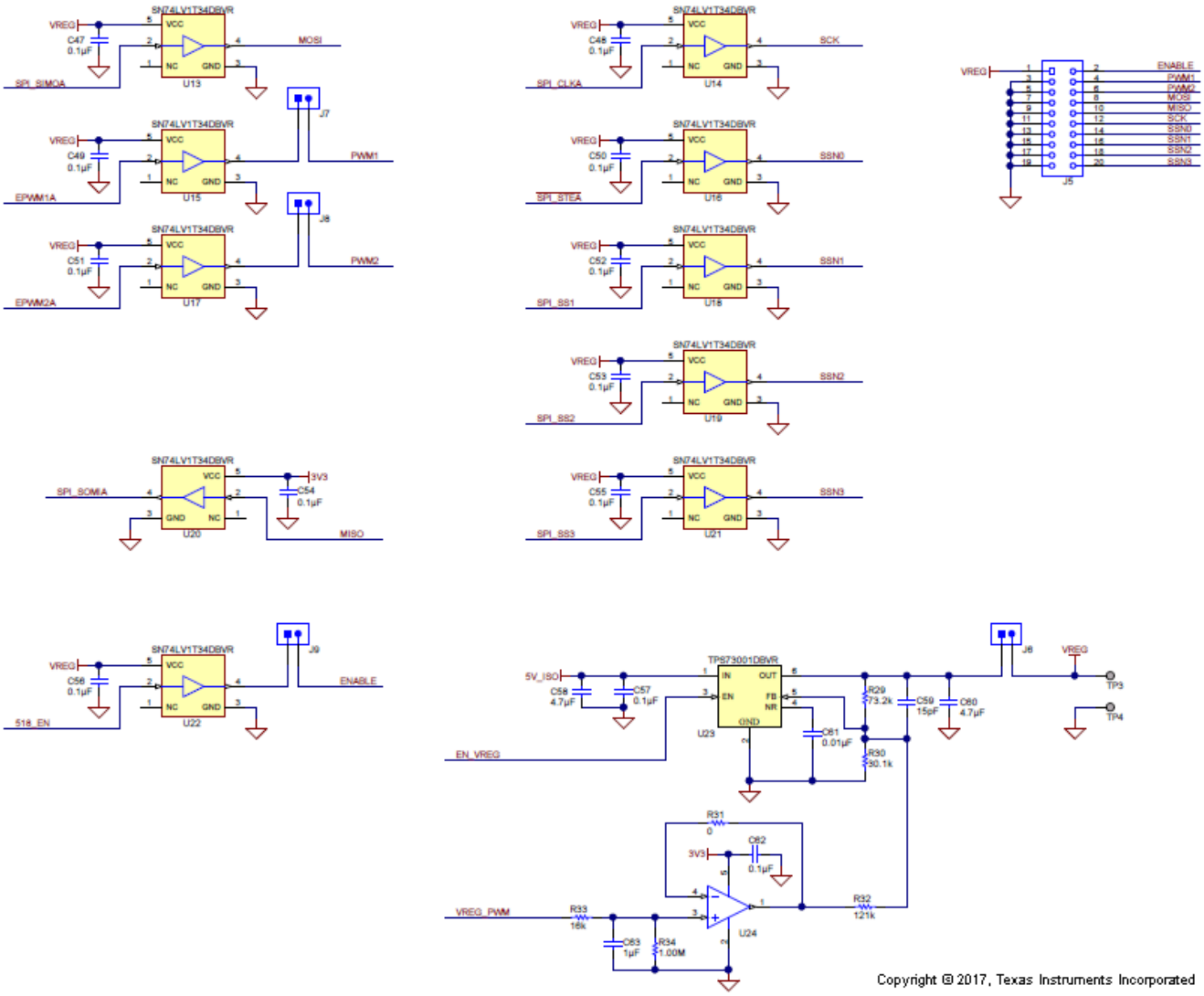


Figure 6-4. LEDSPIMCUEVM-879 Schematic, Page 4

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2018) to Revision D (October 2020)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updated Section 3.4.3	9

Changes from Revision B (April 2018) to Revision C (June 2018)	Page
• Added Wurth part for designator L1, L2	14

Changes from Revision A (January 2018) to Revision B (April 2018)	Page
• Changed J15 to J6 in the *PWM jumpers* row of *Table 1-1, Connector Descriptions*	2
• Changed *Figure 4-2*	12
• Changed *Figure 4-3*	12

Changes from Revision * (May 2017) to Revision A (January 2018)	Page
• Changed "on time" to "off-time" in *Section 1*	2
• Clarified installation instructions in *Section 5.1*	16
• Added operating instructions for Windows 10 in *Section 5.1.1*	20

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