User's Guide

TPS40190 Buck Controller Evaluation Module User's Guide

Table of Contents

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1 Introduction

The TPS40190EVM-001 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.5-V output at up to 10 A from a 12-V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40190 reduced pin count synchronous buck controller.

1.1 Description

The TPS40190EVM-001 is designed to use a regulated 12-V (10 V–14 V) bus to produce a high current, regulated 1.5-V output at up to 10-A of load current. The TPS40190EVM-001 is design to demonstrate the TPS40190 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40190 in a given application. The EVM can be modified to support output voltages from 0.9 V to 3.3 V by changing a single set resistor.

1.2 Applications

- Non-isolated medium current point of load and low voltage bus converters
- Networking equipment
- Telecommunications equipment
- DC power distributed systems

1.3 Features

- 10-V to 14-V input range
- 1.5-V fixed output, adjustable with single resistor
- 10 A_{DC} steady state output current
- 300-kHz switching frequency (fixed by the TPS40190)
- Single main switch N-channel MOSFET and single synchronous rectifier N-channel MOSFET
- Double sided 3-inch × 3-inch PCB with all components on top side
- Active converter uses less than 1.2 square inches – 1.775 × 0.670
- Convenient test points for probing critical waveforms and non-invasive loop response testing

2 TPS40190EVM-001 Electrical Performance Specifications

Table 2-1. TPS40190EVM-001 Electrical and Performance Specifications

Parameter	Notes and Conditions		Min	Typ	Max	Units
Input Characteristics						
Input voltage range			10		14	V
Max input current	V_{IN} = 10 V, I_{OUT} = 10 A			2		A
No-load input current	V_{IN} = 14 V, I_{OUT} = 0 A			100		mA
Output Characteristics						
Output voltage	R6 = 6.49 k, R5 = 10 k		1.45	1.50	1.55	V
Output voltage regulation	Line regulation (10 V < V_{IN} < 14 V, I_{OUT} = 5 A)				1	%
	Load regulation (< 0 A < I_{OUT} < 10 A, V_{IN} = 12 V)					
Output voltage ripple	V_{IN} = 14 V, I_{OUT} = 10 A			25	50	mVpp
Output load current			0		10	A
Output over current				23		A
System Characteristics						
Switching frequency			240	300	360	kHz
Peak efficiency	V_{OUT} = 1.5 V, 8 A < I_{OUT} < 12 A	V_{12V_IN} = 10 V		87		%
		V_{12V_IN} = 12 V		85		
		V_{12V_IN} = 14 V		83		
Full load efficiency	V_{OUT} = 1.5 V, I_{OUT} = 15 A	V_{12V_IN} = 10 V		84		%
		V_{12V_IN} = 12 V		83		
		V_{12V_IN} = 14 V		81		

3 Schematic

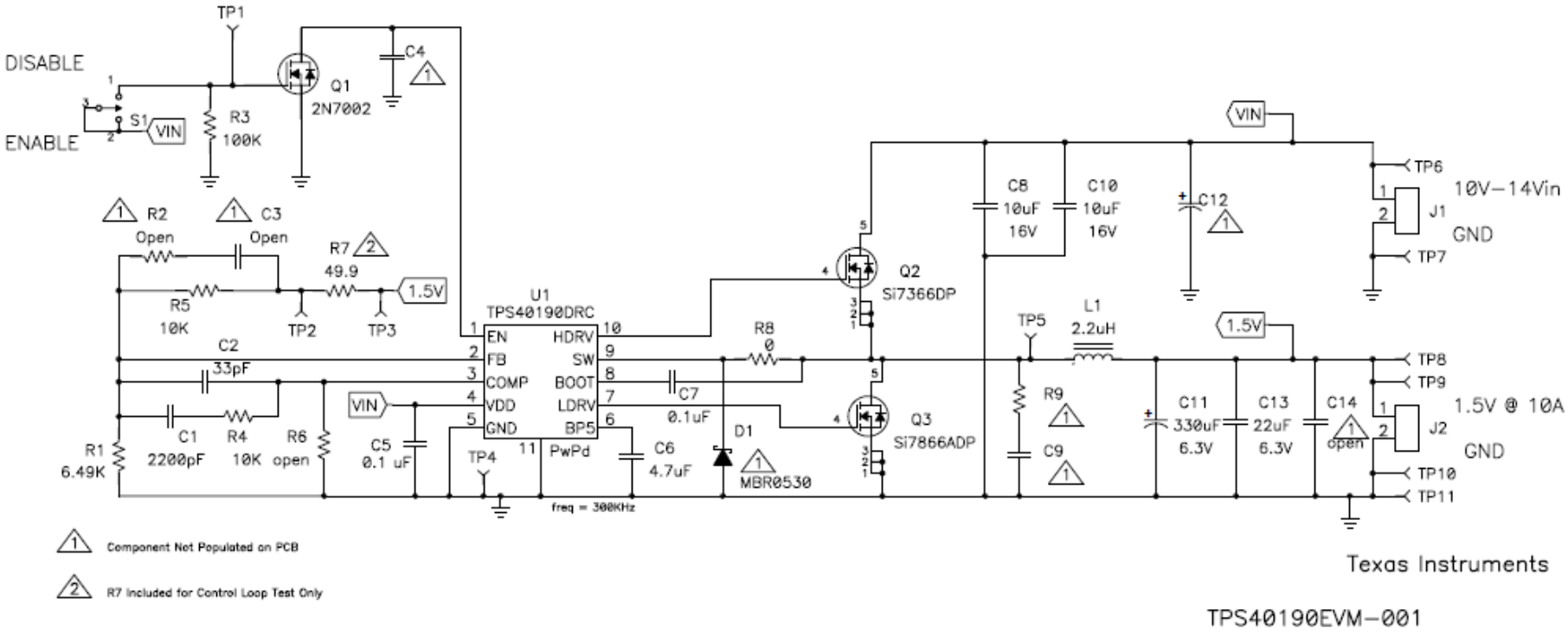

Figure 3-1. TPS40190EVM-001 Power Stage/Control Schematic

Note

The schematic is for reference only. See Table 3-2 for specific values.

3.1 Adjusting Output Voltage (R1)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R1). The output voltage is given by Equation 1.

$$V_{OUT} = V_{VREF} \times \frac{R5 + R1}{R1} \quad (1)$$

where

- V_{VREF} = 0.591 V
- R5 = 10 kΩ

Table 3-1 contains common values for R1 to generate popular output voltages. The TPS40190EVM-001 is stable through these output voltages but the efficiency can suffer as the power stage is optimized for the 1.5-V output.

Table 3-1. Adjusting V_{OUT} with R1

V_{OUT}	R1
3.3 V(1)	2.15 k
2.5 V(1)	3.09 k
2.25 V	3.57 k
2.0 V	4.22 k
1.8 V	4.87 k
1.5 V	6.49 k
1.2 V	9.76 k

(1) For output voltages greater than 2.5 V, change C11 to 330 µF, 4 V or higher PosCAP.

3.2 Adjusting Short Circuit Protection (R6)

The TPS40190 uses a selectable current limit for short circuit protection. The current limit is selected from three levels by placing a resistor at R6. The TPS40190 compares the voltage drop across the high-side FET (VDD to SW) to an internal reference voltage selected during start-up. The voltage levels are shown in Table 3-2.

Table 3-2. Adjusting V_{SCP} with R6

V_{SCP}	R6
160 mV	3.9 k
320 mV	OPEN
420 mV	12 k

The current before declaring short circuit protection can be determined by dividing the VSCP by the RDS(ON) of the high-side FET (Q2).

3.3 Disable (TP1 and SW1)

The TPS40190EVM-001 provides both a Disable input (TP1) and a Disable switch (SW1) to allow the user to evaluate the Enable Function of the TPS40190. When the switch is ON or TP1 is pulled high, Q1 pulls EN (U1 pin 1) to ground and disables the TPS40190 IC.

4 Test Setup

4.1 Equipment

4.1.1 Voltage Source (V_{12V_IN})

The input voltage source (V12V_IN) should be a 0-V to 15-V variable DC source capable of 5 A_{DC}. Connect V12V_IN to J1 as shown in Table 3-2.

4.1.2 Meters

- A1: 0 A_{DC} to 5 A_{DC}, ammeter
- V1: V_{12_IN}, 0-V to 15-V voltmeter
- V2: V_{1V5_OUT}, 0-V to 5-V voltmeter

4.1.3 Loads (LOAD1)

The output load (LOAD1) should be an electronic constant current mode load capable of 0-A_{DC} to 15 A_{DC} at 1.5 V.

4.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the ripple voltage on VOUT. The oscilloscope should be set for the following to take output ripple measurements:

- 1-MW impedance
- 20-MHz bandwidth
- AC coupling
- 1-ms/division horizontal resolution
- 20-mV/division vertical resolution

TP 9 and TP 10 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP 9 and holding the ground barrel to TP 10 as shown in Figure 4-1. For a hands-free approach, the loop in TP 10 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

V_{12V_IN} to J1

The connection between the source voltage, V12V_IN, and J1 of the TPS40190EVM-001 can carry as much as 3 A_{DC}. The minimum recommended wire size is AWG #16 with the total length of wire less than four feet (2-feet input, 2-feet return).

J2 to LOAD1 (Power)

The power connection between J2 of TPS40190EVM-001 and LOAD1 can carry as much as 15 A_{DC}. The minimum recommended wire size is 2× AWG #16, with the total length of wire less than four feet (2-feet output, 2-feet return).

4.1.6 Other

FAN

This evaluation module includes components that can get hot to the touch. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

4.2 Equipment Setup

Figure 4-1 is the basic test setup recommended to evaluate the TPS40190EVM-001. Please note that although the return for J1 and J2 are the same, the connections should remain separate as shown in Figure 4-1.

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V12V_IN, it is advisable to limit the source current from V12V_IN to 5.0-A maximum. Make sure V12V_IN is initially set to 0 V and connected as shown in Figure 4-1.
3. Connect the ammeter A1 (0-A to 5-A range) between V12V_IN and J1 as shown in Figure 4-1.
4. Connect voltmeter V1 to TP6 and TP7 as shown in Figure 4-1.
5. Connect LOAD1 to J2 as shown in Figure 4-1. Set LOAD1 to constant current mode to sink 0 A_{DC} before V12V_IN is applied.
6. Connect voltmeter V2 across TP8 and TP11 as shown in Figure 4-1.
7. Connect an oscilloscope probe to TP9 and TP10 as shown in Figure 4-1Figure 3.
8. Place a fan as shown in Figure 4-1 and turn on, making sure air is flowing across the EVM.

4.2.2 Diagram

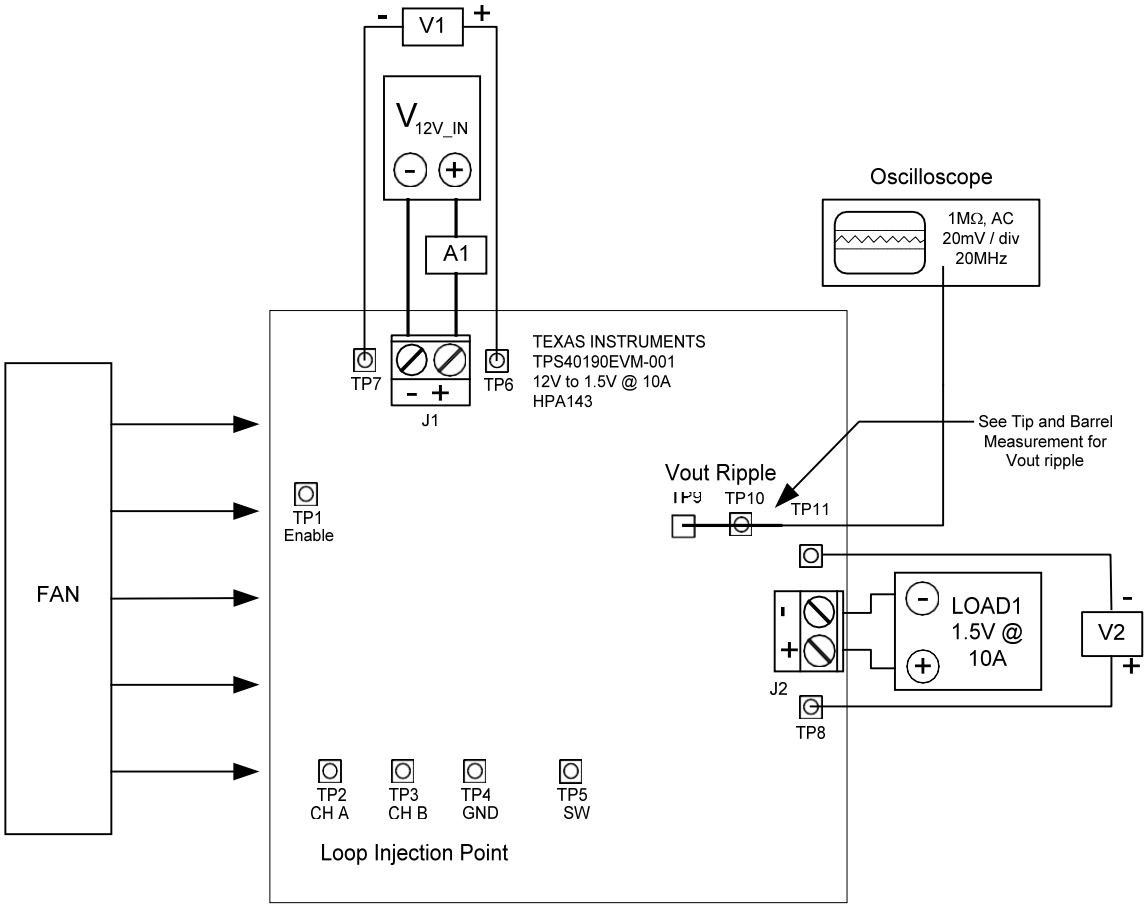

Figure 4-1. TPS40190EVM-001 Recommended Test Setup

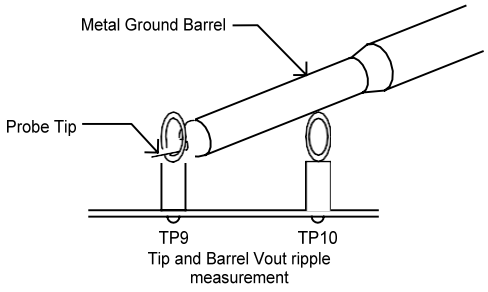

Figure 4-2. Output Ripple Measurement – Tip and Barrel Using TP9 and TP10

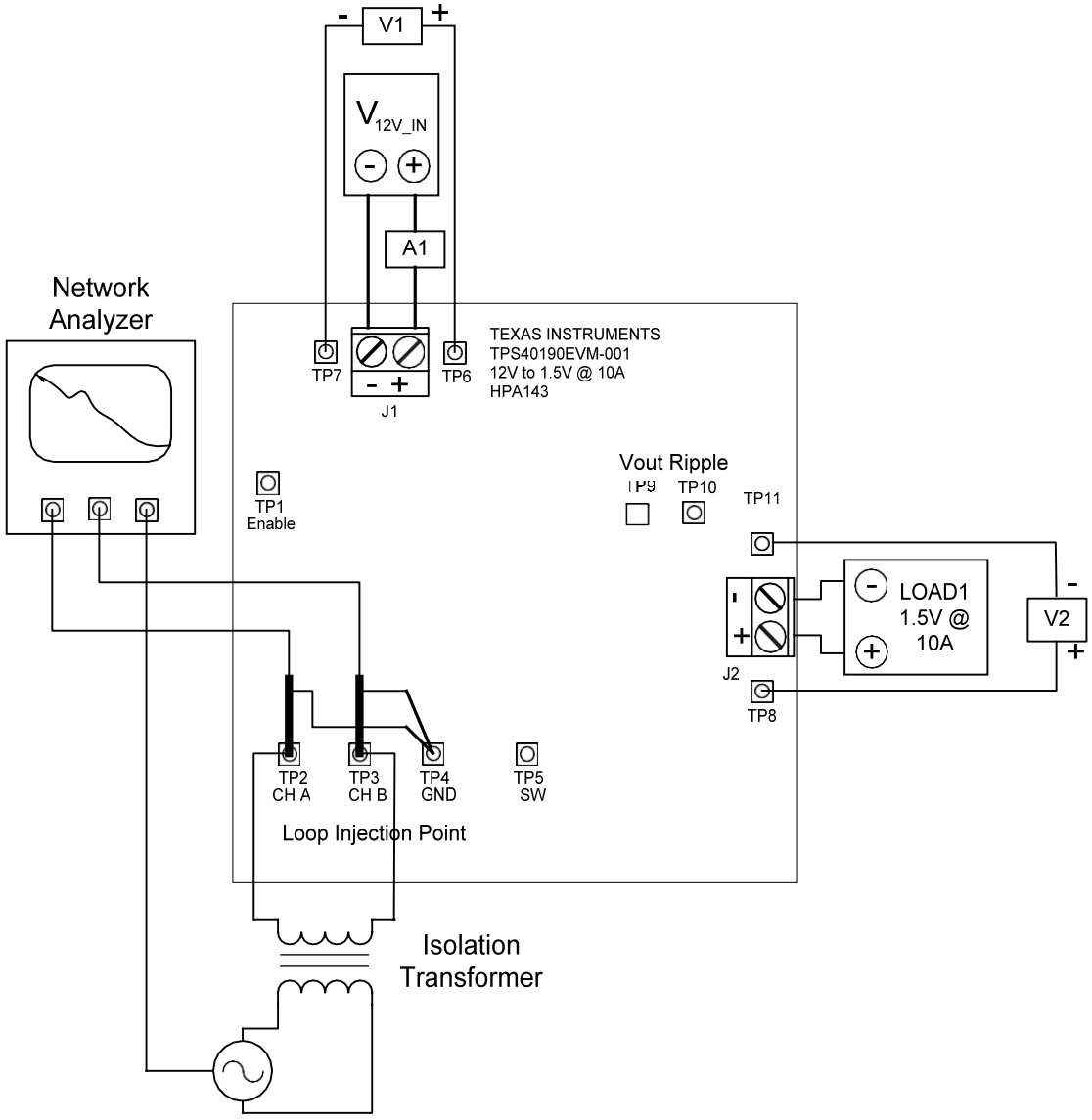

Figure 4-3. Control Loop Measurement Setup

4.3 Start-Up/Shutdown Procedure

1. Increase V_{12V_IN} from 0 V to 10 V_{DC}.
2. Vary LOAD1 from 0 A_{DC} to 10 A_{DC}.
3. Vary V_{12V_IN} from 1- V_{DC} to 14 V_{DC}.
4. Decrease LOAD1 to 0 A.

4.4 Control Loop Gain and Phase Measurement Procedure

1. Connect a 1-kHz to 1-MHz isolation transformer to TP2 and TP3 as shown in Figure 4-1.
2. Connect an input signal amplitude measurement probe (Channel A) to TP2 as shown in Figure 4-1.
3. Connect an output signal amplitude measurement probe (Channel B) to TP3 as shown in Figure 4-1.
4. Connect the ground lead of Channel A and Channel B to TP 4 as shown in Figure 4-1.
5. Inject 25-mV or less signal across R7 through an isolation transformer.
6. Sweep frequency from 1 kHz to 1 MHz with 10-Hz or lower post filter.
7. Control loop gain can be measured by $20 \times LOG\left(\frac{ChannelB}{ChannelA}\right)$.
8. Control loop phase is measured by the phase difference between Channel A and Channel B.
9. Disconnect the isolation transformer from TP2 and TP3 before making other measurements (signal injection into feedback can interfere with accuracy of other measurements).

4.5 Equipment Shutdown

1. Shut down the oscilloscope.
2. Shut down LOAD1.
3. Shut down V_{12V_IN}.
4. Shut down FAN.

5 TPS40190EVM Typical Performance Data and Characteristic Curves

Figure 5-1 and Figure 5-2 present typical performance curves for the TPS40190EVM-001. Since the actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

5.1 Efficiency

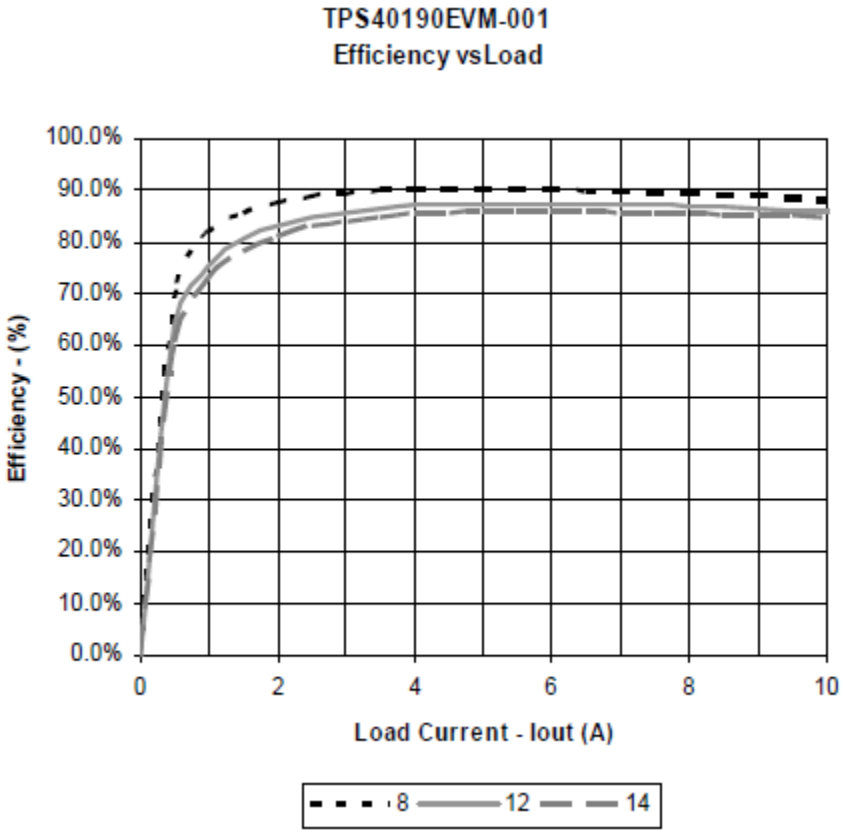

Figure 5-1. TPS40190EVM-001 Efficiency, V_{IN} = 10 V to 14 V, V_{OUT} = 1.5 V, I_{OUT} = 0 A to 10 A

5.2 Line and Load Regulation

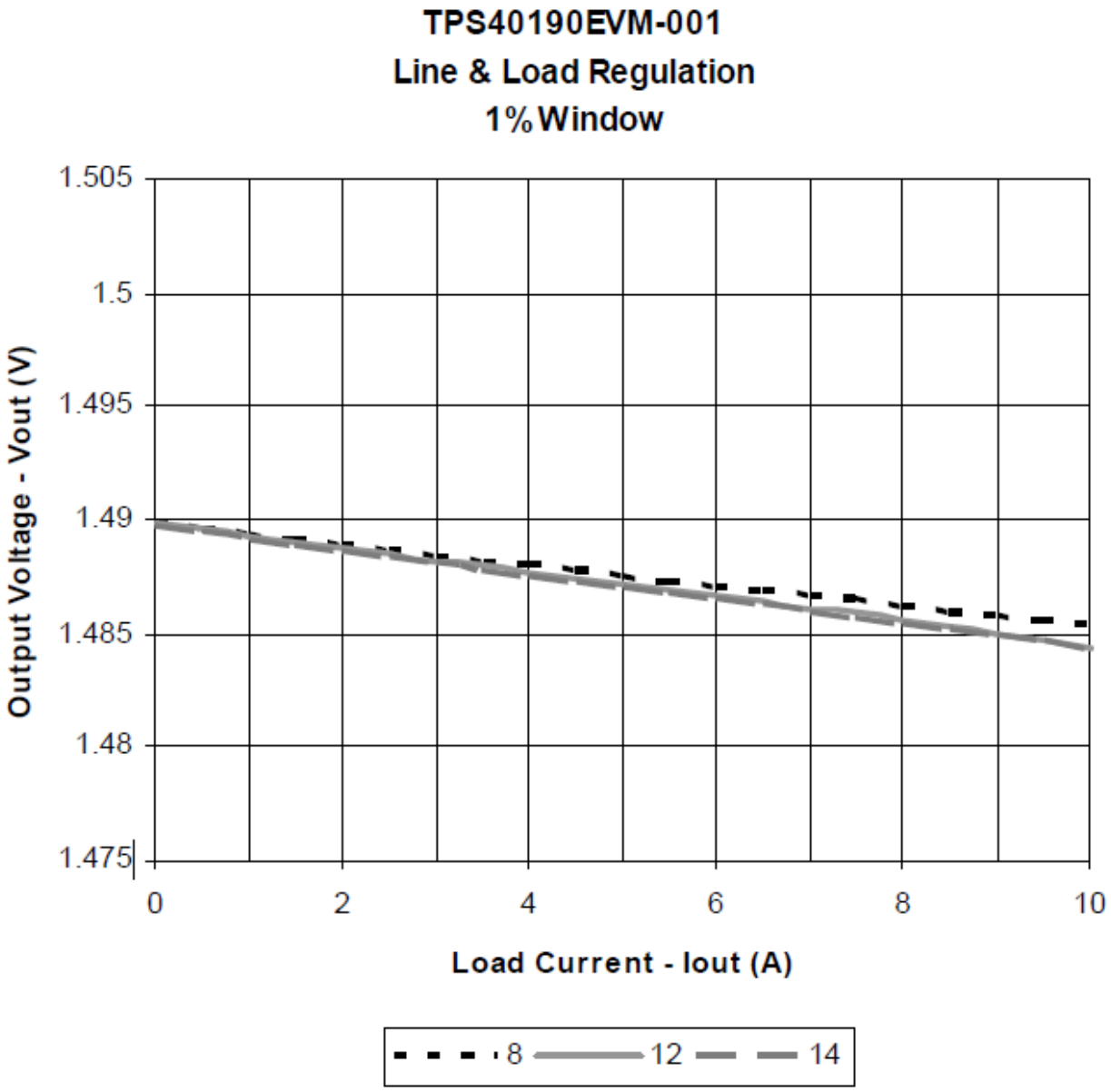

Figure 5-2. TPS40190EVM-001 Line and Load Regulation

6 EVM Assembly Drawings and Layout

Figure 6-1 and Figure 6-4 show the design of the TPS40190EVM-001 printed circuit board. The EVM has been designed using a double sided, 2-oz copper-clad circuit board 3.0-inch × 3.0-inch with all components on the top side to allow the user to easily view, probe, and evaluate the TPS40190 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

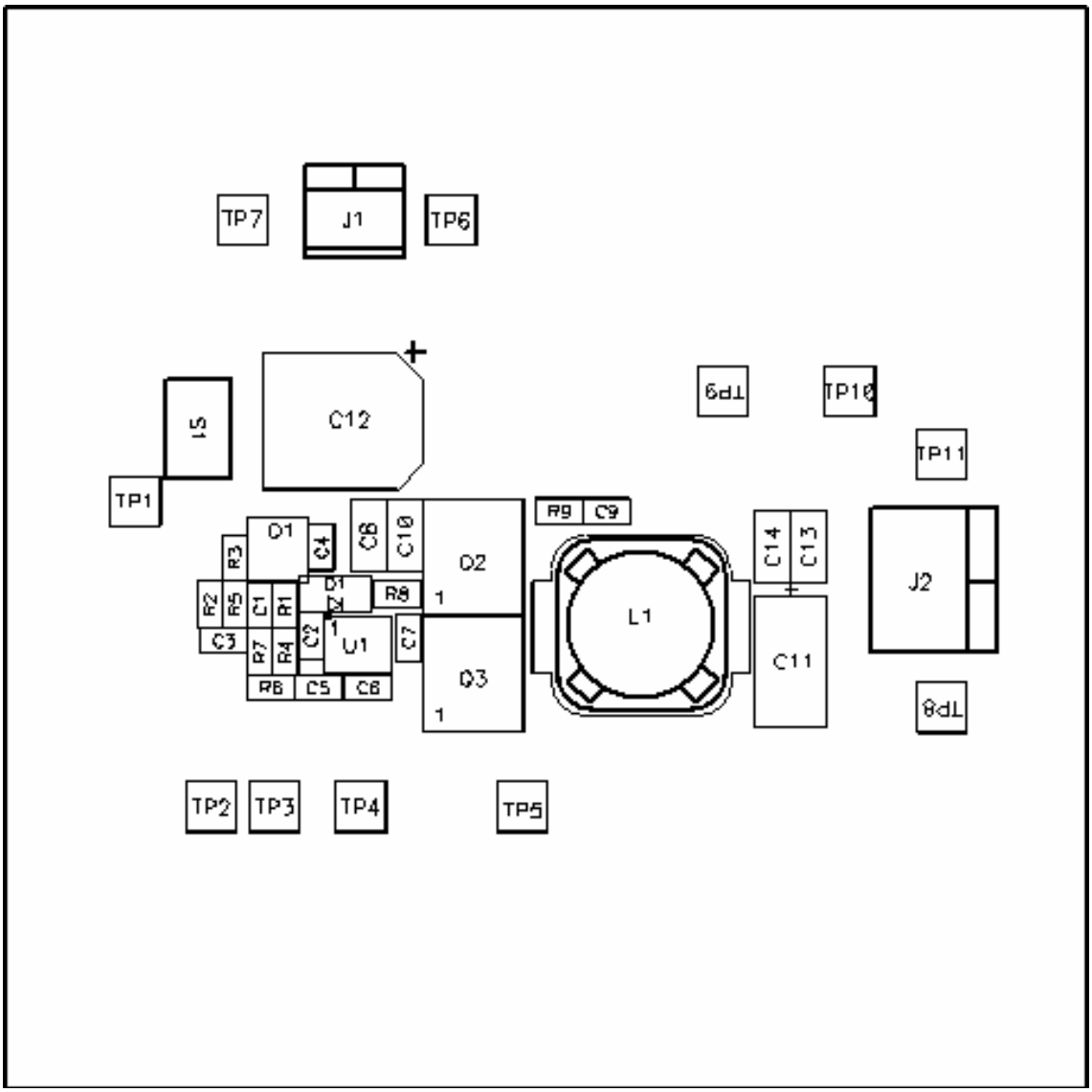

Figure 6-1. TPS40190EVM-001 Component Placement (Viewed from Top)

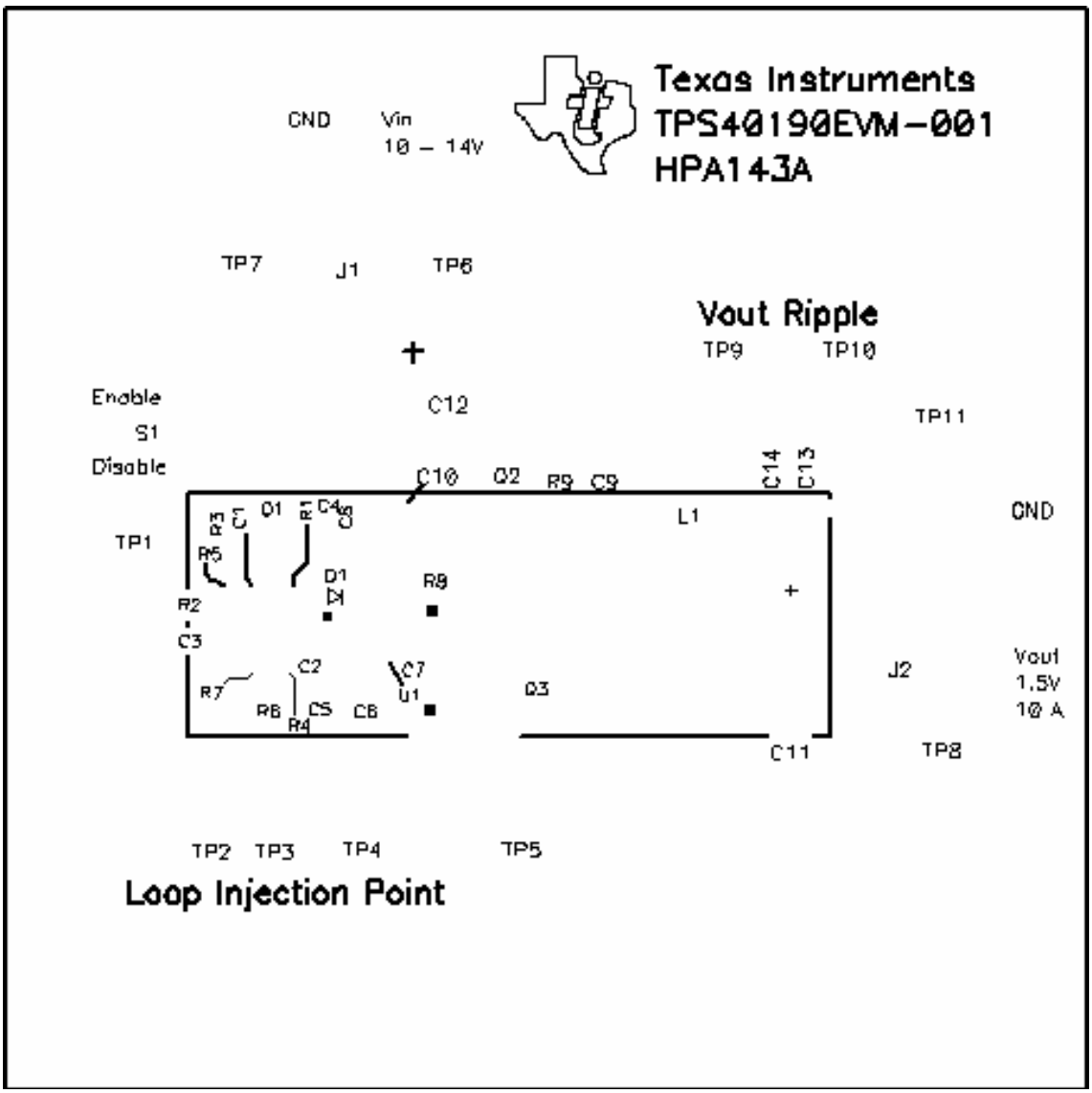

Figure 6-2. TPS40190EVM-001 Silkscreen (Viewed from Top)

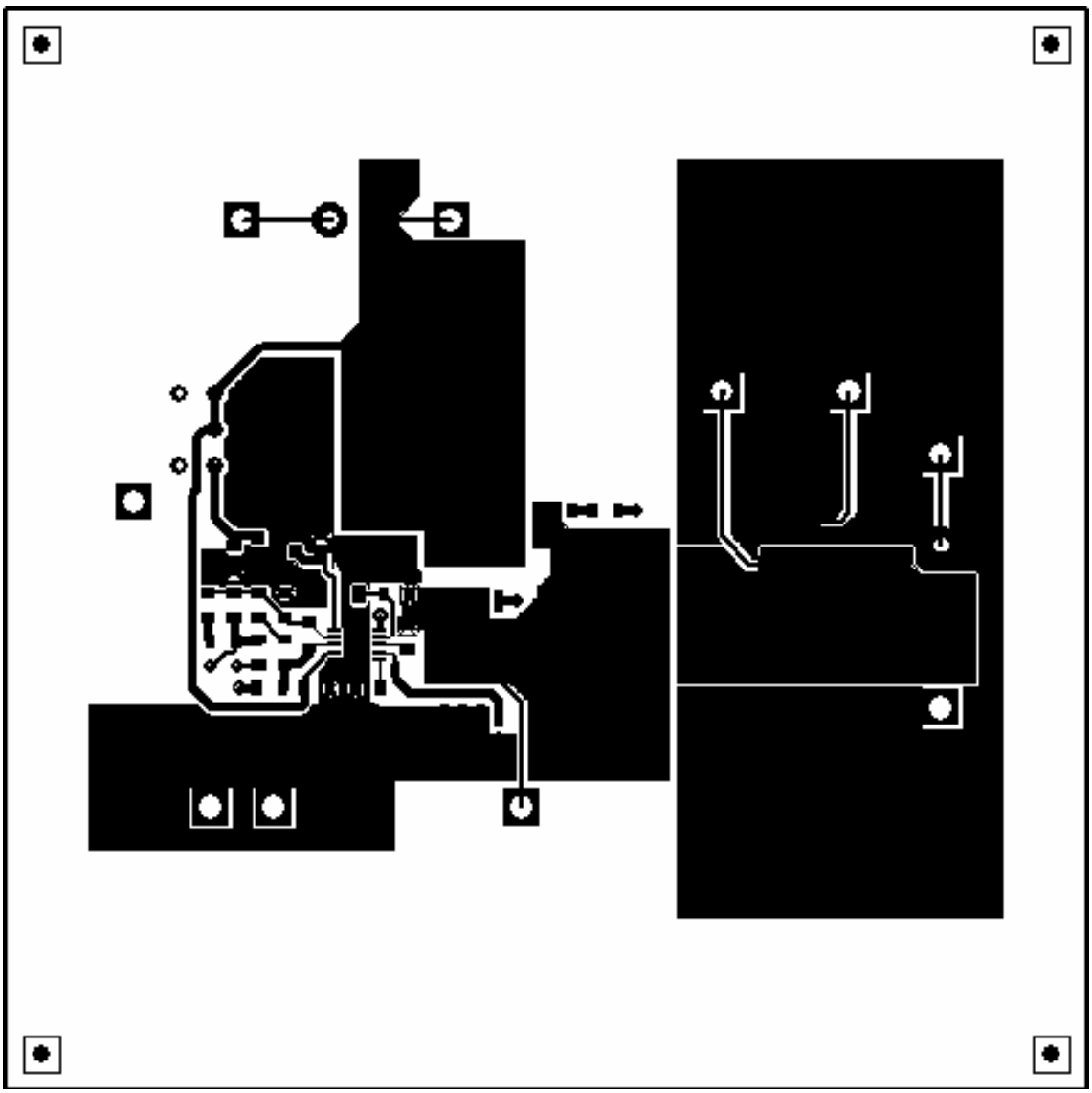

Figure 6-3. TPS40190EVM-001 Top Copper (Viewed from Top)

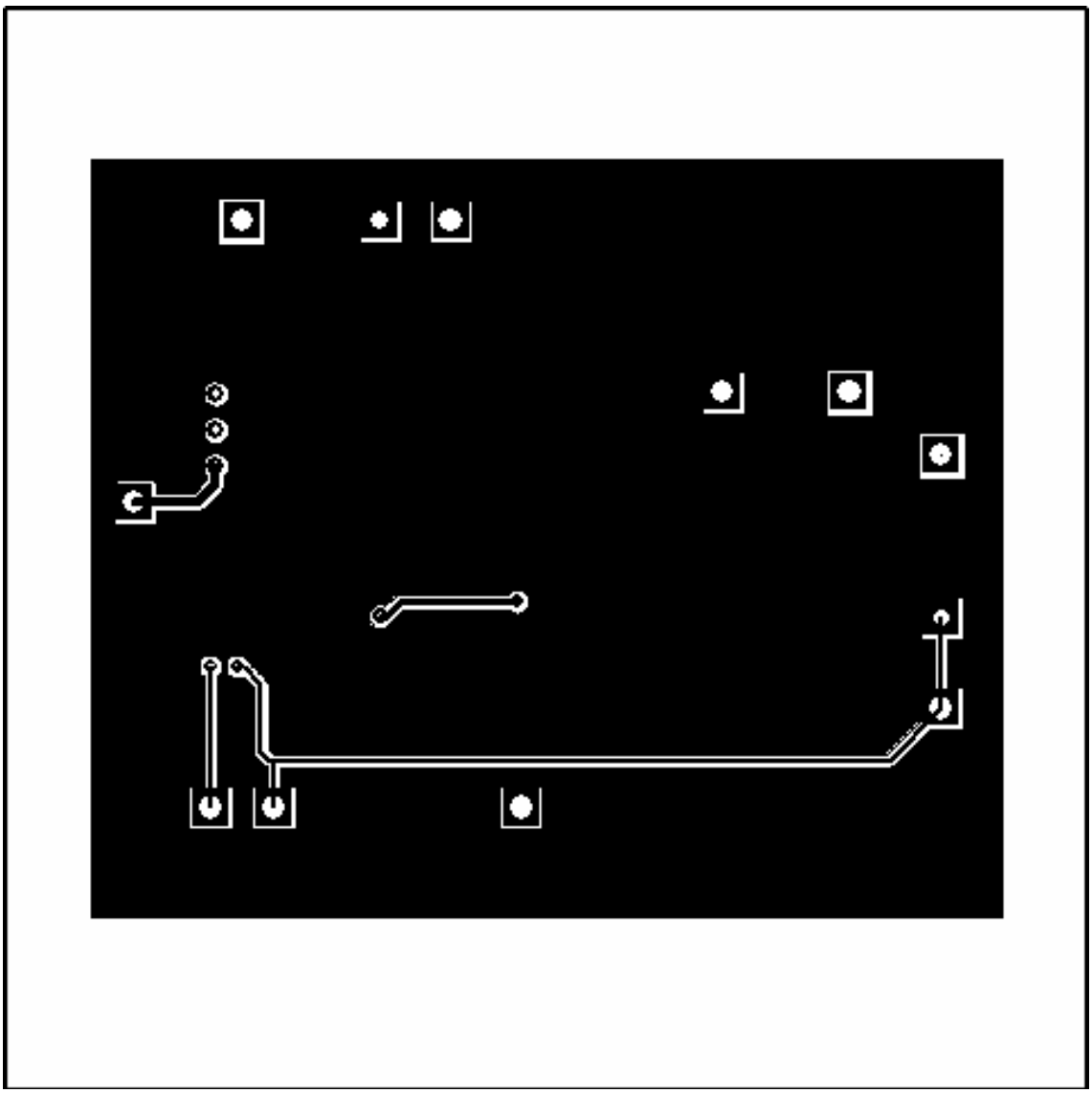

Figure 6-4. TPS40190EVM-001 Bottom Copper (X-Ray View from Top)

7 List of Materials

Table 7-1. TPS40190EVM-001 Bill of Materials

Count	RefDes	Description	Size	Mfr	PartNumber
1	C1	Capacitor,Ceramic, 2200 pF, 50 V, X7R	0603	Std	Std
1	C11	Capacitor,PosCAP, 330 µF, 6.3 V, 20%	7343	Sanyo	6TPB330M
0	C12	Capacitor,Aluminum, open	8x10mm		
1	C13	Capacitor,Ceramic, 22 µF, 6.3 V, X5R	1206	TDK	C3216X5R0J226KT
0	C14	Capacitor,Ceramic, open	1206		
1	C2	Capacitor,Ceramic, 33 pF, 50 V, C0G	0603	Std	Std
0	C3, C4, C9	Capacitor,Ceramic, open	0603		
2	C5, C7	Capacitor,Ceramic, 0.1 µF, 16 V, X5R	0603	Std	Std
1	C6	Capacitor,Ceramic, 4.7 µF, 6.3 V, X5R	0603	TDK	C1608X5R0J475KT
2	C8, C10	Capacitor,Ceramic, 10 µF, 16 V, X5R	1206	TDK	C3216X5R1C106KT
0	D1	Diode,Schottky, 0.5 A, 30 V	SOD123	OnSemi	MBR0530T1
1	J1	TerminalBlock, 2-pin, 6-A, 3.5 mm	0.27x 0.25	OST	ED1514
1	J2	TerminalBlock, 2-pin, 15-A, 5.1 mm	0.40x 0.35	OST	ED1609
1	L1	Inductor,SMT, 2.2 µH, 12.5 A, 4 mΩ	0.492sq inch	Coiltronics	DR127-2R2
1	Q1	MOSFET, N-ch, 60 V, 115 mA, 1.2 Ω	SOT23	Vishay	2N7002
1	Q2	MOSFET,NChannel, 20 V, 16 A, 9 mΩ	PWRPAKS0-8	Vishay	Si7366DP
1	Q3	MOSFET,NChannel, 20 V, 40 A, 3.0 mΩ	PWRPAKS0-8	Vishay	Si7866ADP
1	R1	Resistor,Chip, 6.49 kΩ, 1/16-W, 1%	0603	Std	Std
0	R2, R6, R9	Resistor,Chip, Open, 1/16-W, 1%	0603	Std	Std
1	R3	Resistor,Chip, 100 kΩ, 1/16-W, 1%	0603	Std	Std
2	R4, R5	Resistor,Chip, 10 kΩ, 1/16-W, 1%	0603	Std	Std
1	R7	Resistor,Chip, 49.9 Ω, 1/16-W, 1%	0603	Std	Std
1	R8	Resistor,Chip, Zero Ω, 1/16-W, 1%	0603	Std	Std
1	S1	Switch,ON-ON Mini Toggle	0.28 × 0.18		633-G12AP
4	TP1, TP2, TP3, TP5	TestPoint, White, Thru Hole	0.125 × 0.125	Farnell	5012
4	TP4, TP7, TP10, TP11	TestPoint, Black, Thru Hole	0.125 × 0.125	Farnell	5011

Table 7-1. TPS40190EVM-001 Bill of Materials (continued)

Count	RefDes	Description	Size	Mfr	PartNumber
3	TP6, TP8, TP9	TestPoint, Red, Thru Hole	0.125 × 0.125	Farnell	5010
1	U1*	IC,Low cost synchronous buck controller	DRC10	TI	TPS40190DRC
1	—	PCB,2-Layer FR4, 3.0 inch × 3.0 inch × 0.062 inch	3.0 inch× 3.0 inch	Any	TPS40190EVM-001
4	—	Bumpon,Transparent	0.44 inch× 0.2 inch	3M	SJ5303

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2005) to Revision A (January 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title....2
- Edited user's guide for clarity....2

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