*Application Note*

# *Review of Different Power Factor Correction (PFC) Topologies' Gate Driver Needs*

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**ABSTRACT**

When designing a switching power supply, high efficiency, high power factor (PF), and low power line harmonics are critical. This application note provides an overview of power factor correction (PFC) topologies including relative advantages and the gate drivers that are needed for each.

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## Trademarks

# 1 Introduction

To understand PFC, we must first define power factor. Power factor is the ratio of real power in Watts divided by the apparent power. The real power is what is consumed by the load and the apparent power is what is circulating between the source and the load. The ideal power factor is 1, meaning that there are no losses due to reactive power and all apparent power is real power. Figure 1-1 and Figure 1-2 shows waveforms of a system with a power factor of 1 and of 0.69. Note the increase in peak current due to the decreased power factor.

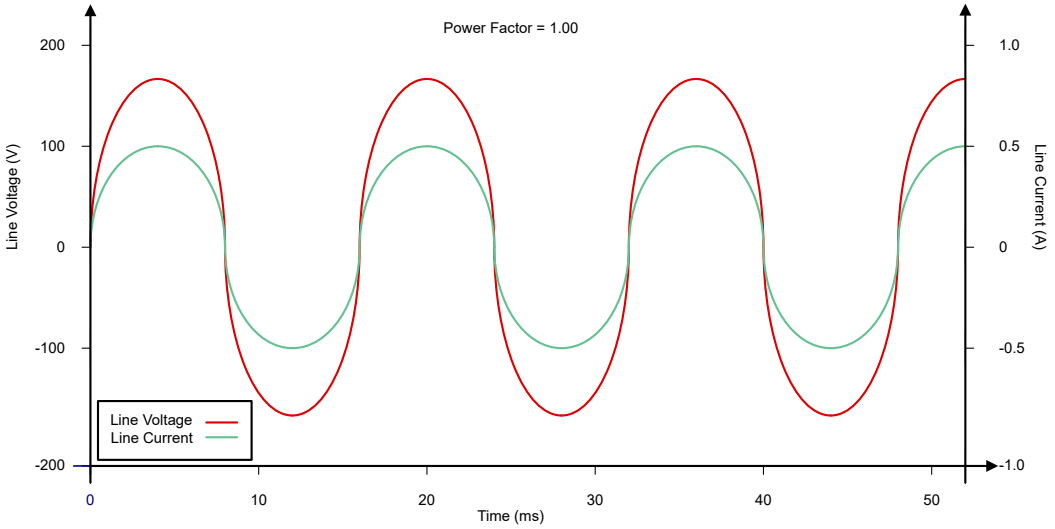


**Figure 1-1. Power Factor of 1.00**

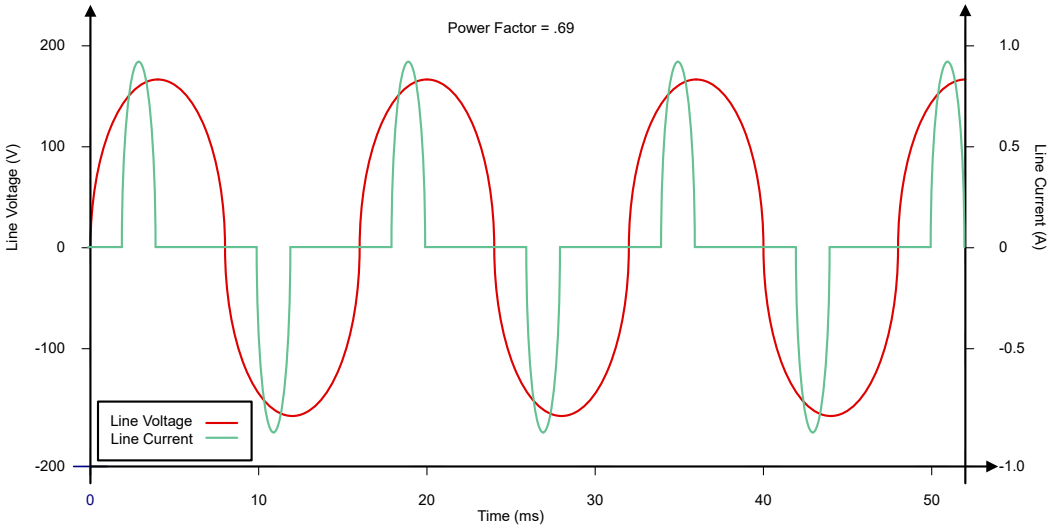


**Figure 1-2. Power Factor of 0.69**

Switching power supplies are often used for power factor correction. Switching power supplies typically utilize a diode bridge to rectify an alternating current (AC) signal to a direct current (DC) signal. This diode bridge chops the AC signal which impacts both power factor and total harmonic distortion (THD). Filters are sometimes used for smoothing this chopped signal and improving power factor. However, these filters require large passive components and yield large power losses. Figure 1-3 shows an example of a diode bridge and a passive filtering method of PFC.

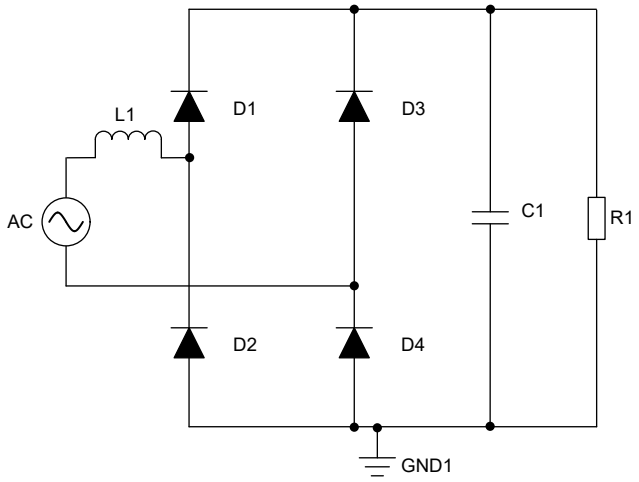


**Figure 1-3. Simple Passive PFC Circuit Diagram With a Diode Rectifying Bridge**

## 2 Typical PFC Topologies

Some of the more popular, active topologies that are discussed here are the boost, interleaved boost, bridgeless boost, and the bridgeless totem pole. Passive topologies are not discussed here due to them typically being used in systems less than 100W. This is due to the large passive component required for higher power systems and the narrow operating ranges. The active topologies depend on MOSFET switching for control with a gate driver IC driving the MOSFETs.

### 2.1 Boost PFC

Switching converter topologies are used for active power factor correction to improve both power efficiency and density. Over the past two decades, one of the most prominent topologies is the boost PFC, which utilizes a single low-side MOSFET, an inductor, and a diode. For efficient AC-to-DC conversion, the MOSFET gate driver must meet certain requirements to drive the MOSFET effectively. Some of these driver requirements include the peak drive current and the switching characteristics. High drive current is needed due to the high-power switches that are required for PFCs. Fast switching characteristics such as rise and fall times as well as propagation delays allow for fast switching transitions, reducing losses and increasing efficiency. This need for fast switching transitions is due to the switching losses in the MOSFETs. The MOSFETs are inefficient during the turn on and off times due to the dynamic voltages and currents that are handled. Other requirements include under voltage lockout and noise handling capabilities. Boost PFCs are often driven by single-channel, low-side, non-isolated gate drivers. Texas Instruments has a large portfolio of drivers that meet or exceed these requirements such as the UCC27517A.

By using a low-side gate driver and a MOSFET for switching, the boost converter PFC forces input current to be in-phase with the input voltage, thus correcting the power factor. This is accomplished by the boost converter controller that is sending PWM pulses to the gate driver that is used to provide voltage and current gain to drive the FET. This approach is typically used for power levels of 100W up to 4kW. Figure 2-1 shows a typical boost converter PFC utilizing the UCC27517A.

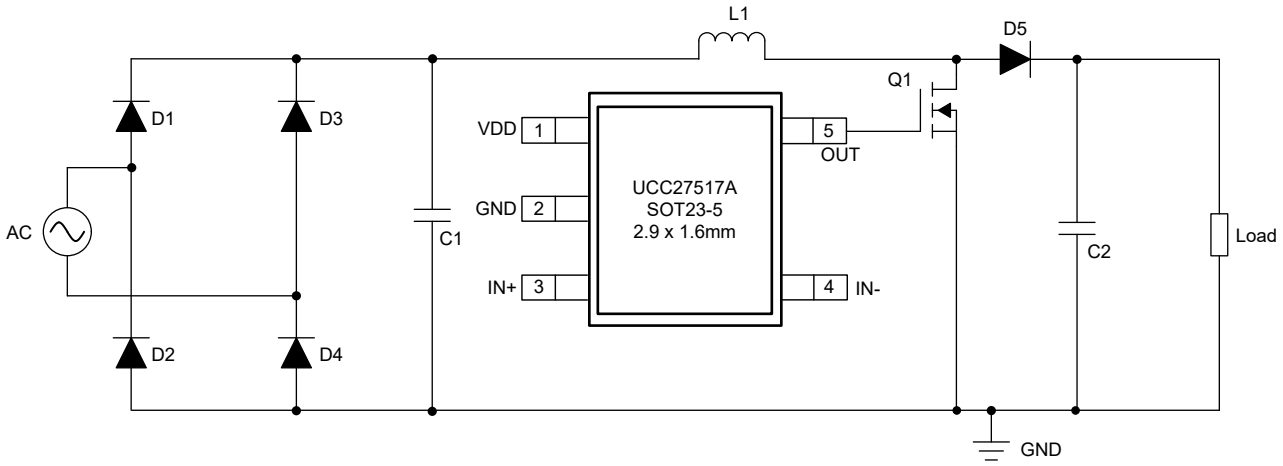


**Figure 2-1. Boost PFC Using a MOSFET, Rectifier Bridge, an Inductor and a Diode With an Output Capacitor Filter**

The UCC27517A is a non-isolated, single-channel low-side gate driver that can be used for driving these high power MOSFETs in the boost topology. This driver has output current capabilities of 4A sink and 4A source and an 18V maximum recommended operation on VDD rating. UCC27517A has a propagation delay of 13ns and a rise time of 9ns and fall time of 7ns on the output to also help maximize efficiency that is needed for these systems. This device features under-voltage lockout (UVLO) to maintain glitch-free operation in power on and off transients to increase system robustness.

## 2.2 Interleaved Boost PFC

Interleaved boost PFCs are a more efficient and complex option than the traditional boost PFC. The interleaved boost PFC offers improvements to system efficiency, but at the cost of additional components. The gate driver requirements for an interleaved boost system are very similar to that of the boost system, except an additional channel is needed for the second MOSFET. To drive the two MOSFETs required for this topology, a dual-channel low-side gate driver such as the UCC27624 is often used. Figure 2-2 shows an example of an interleaved boost circuit.

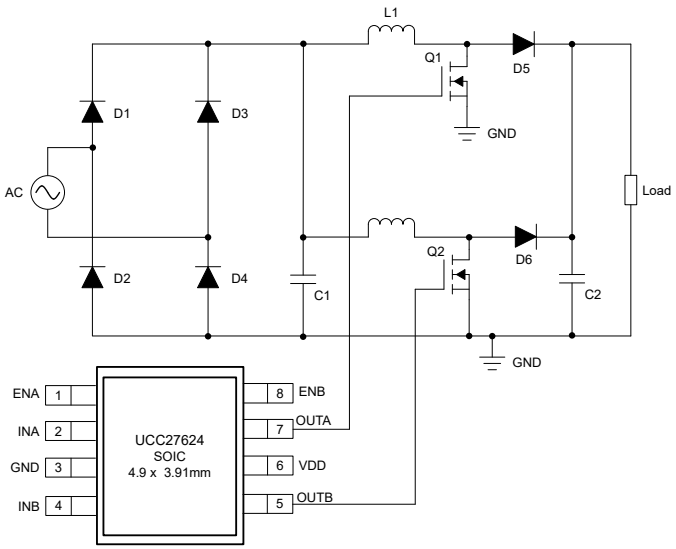


**Figure 2-2. Interleaved Boost Converter PFC With Parallel Boost Converters and a Diode Rectifier Bridge**

Overall, by interleaving two boost circuits into one interleaved boost PFC there is a reduction in electromagnetic interference (EMI) and the boost inductor size. However, this comes with the tradeoff between a reduction in inductor size or a reduction in switching frequency. Reducing the switching frequency can help reduce the size of the EMI filter, but requires a larger inductor which increases magnetic volume. Also, the root mean squared

(RMS) current in the boost capacitor is greatly reduced due to interleaving, but with that comes added cost and complexity.

The UCC27624 is often used in interleaved boost PFC circuit designs. The UCC27624 is dual-channel to account for driving both MOSFETs and is a non-isolated low-side gate driver. The UCC27624 can drive the high power MOSFETs that are used in the interleaved boost topologies due to the high output current capabilities of 5A sink and 5A source and is 30V rated. This driver's propagation delay of 17ns and delay matching of 1ns as well as the rise time of 6ns and fall time of 10ns on the output channels helps to achieve the maximum efficiency that is required of these systems. UCC27624 also features UVLO and a -10V tolerance on the inputs for increased system robustness.

## 2.3 Bridgeless Boost PFC

The bridgeless boost PFC is similar to the interleaved boost PFC with the exception of the input rectifier bridge (diodes D1, D2, D3 and D4 in Figure 2-2). Removing these diodes eliminates two elements of loss during each switching cycle compared to the interleaved boost topology. The body diode of the FET that is not conducting is subject to losses as the body diode acts as a slow diode in the OFF state of the half cycle. In this topology is EMI because the output voltage ground stays floating in reference to the input AC signal. So, all of the parasitic capacitances contribute to the common-mode noise that can be difficult to filter. Increasing the switching frequency reduces the losses due to the parasitic capacitances.

Therefore, the required sizes of the passive components (the inductor and capacitor) can be reduced which minimizes system size, cost, and EMI. Figure 2-3 shows that the switches in this topology can be driven by a dual channel low-side driver such as the UCC27624.

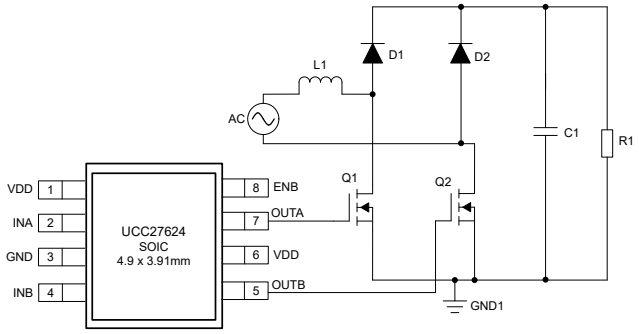


**Figure 2-3. Bridgeless Boost PFC Circuit With UCC27624 Low-Side Dual-Channel Gate Driver**

## 2.4 Bridgeless Totem Pole PFC

One of the latest developments in PFC topologies is the totem pole PFC. The active, bridgeless topology replaces the diode-rectifying bridge of the previously shown passive topology with switches. These additional power switches are typically silicon (Si), silicon carbide (SiC), or gallium nitride (GaN). Here, the focus is on Si and SiC FETs for this topology. Silicon carbide (SiC) FETs only have two junctions in series (as opposed to three in the boost topology). Utilizing SiC FETs allows for faster switching and lower reverse recovery charge which leads to reduced switching losses. Figure 2-4 and Figure 2-5 show two configurations for the totem pole PFC topology.

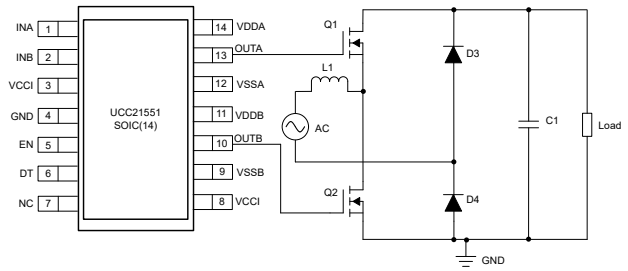


**Figure 2-4. Totem Pole PFC Circuit Utilizing Diodes for Line Rectification**

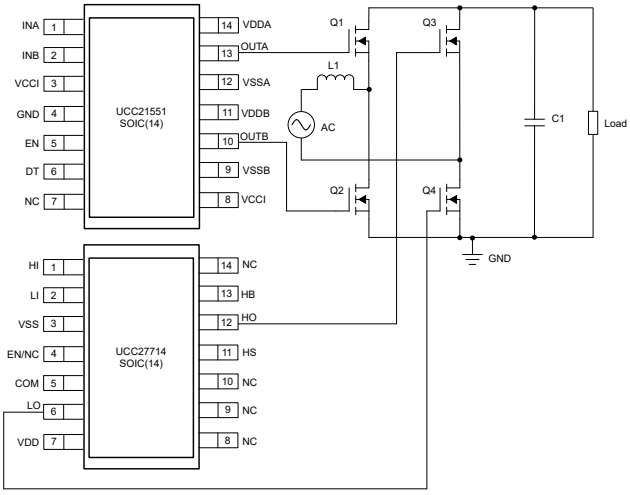


**Figure 2-5. Totem Pole PFC Circuit Utilizing MOSFETs for Line Rectification**

The totem pole topology has two branches of switching, the right-side branch with either two silicon (Si) MOSFETs (Q3 and Q4 in Figure 2-5) or two diodes (D3 and D4 in Figure 2-4) and the left branch with two SiC FETs (Q1 and Q2 in Figure 2-4 and Figure 2-5). The right branch, called the slow leg, provides line rectification of the AC signal at grid frequency (typically 50 or 60Hz). The slow leg is in a half-bridge configuration and so a 600V half-bridge driver is needed. This voltage rating is due to these circuits typically outputting around 400V DC. The left branch, the fast leg, which switches at high frequencies (100 to 250kHz), is used step up the voltage and shape the input current. At these high switching frequencies, operational difficulties occur with noise-creating transients, adding inefficiencies. These transients are due to the differential voltage between the two separate ground references. The gate driver's tolerance to this noise is called common-mode transient immunity (CMTI). Isolated gate drivers provide high CMTI, therefore, an isolated dual-channel gate driver is needed to output the high current needed for the SiC power FETs and maintain maximum efficiency.

For the slow leg, a 600V half-bridge gate driver that provides high drive current and fast switching characteristics to drive the high-power switches used is needed. The UCC27714 is a 600V, non-isolated driver with high output current capabilities of 4A sink and 4A source peaks. The low propagation delay of 90ns and delay matching of 20ns as well as the rise and fall times of 15ns on HO and LO helps achieve the maximum efficiency that is required of these systems.

The SiC FETs that are often used on the fast leg require low delay times, high CMTI and high current to maximize efficiency. The UCC21551 is an example of a driver that meets the needs of the fast leg. The UCC21551 has a CMTI rating of 125V/ns and drive current of 4A source and 6A sink. The UCC21551 also has the fast switching characteristics needed such as a 33ns propagation delay and 5ns maximum delay matching. The input side isolation of the UCC21551 is rated at $5kV_{RMS}$ peak-reinforced isolated barrier as well as UVLO protection of 12V or 17V.

## 3 Switches and Gate Drivers in PFC Topologies

In PFC circuits, the switching components (diodes and MOSFETs) account for around 20% of all losses, therefore, careful selection of the power switch is important, as well as the driver that controls the power switch to optimize performance. To minimize losses, a MOSFET with low $R_{DS(ON)}$ conduction losses and a low gate charge ($Q_G$) is important. To compare FETs, a rating is created that is a scalar value with the loss contributing parameters of $R_{DS(ON)}$ multiplied by $Q_G$. This scalar result is a figure of merit that creates a rating scale to compare FETs where the lowest rating yields the most efficient power switch. For most of these topologies, Si MOSFETs are an excellent choice and operate as needed, but SiC or GaN FETs are needed for the high switching frequencies required by the highest efficiency applications.

Table 3-1 shows some examples of the power switches that have been used in reference designs for PFC circuits.

**Table 3-1. MOSFETs Used in Reference Designs for PFC**

| Topology | Boost | Boost | Bridgeless Boost | Interleaved Boost | Interleaved Boost | Totem Pole | Totem Pole | |
|---|---|---|---|---|---|---|---|---|
| **Power (W)** | 1000 | 1000 | 300 | 1500 | 700 | 6600 | 3000 | |
| **Type** | Si | SiC | Si | Si | Si | SiC | SiC | Si |
| **$V_{DS}$ (V)** | 650 | 900 | 550 | 600 | 650 | 1000 | 750 | 600 |
| **$V_{GS(th)}$ (V)** | 4 | 2.1 | 3 | 3 | 3 | 2.1 | 4.8 | 3.5 |
| **$R_g$ (Ω)** | 3.5 | 3.5 | 2.2 | 0.85 | 1.3 | 3.5 | 4.5 | 0.45 |
| **$r_{DS(on)}$ (Ω)** | 0.171 | 0.065 | 0.22 | 0.063 | 0.22 | 0.065 | 0.018 | 0.015 |
| **$C_{oss}$ (pF)** | 76 | 66 | 63 | 215 | 54 | 70 | 217 | 200 |
| **$Q_g$ (nC)** | 37 | 30 | 27 | 170 | 26 | 37 | 37.8 | 340 |
| **Rating** | 6.327 | 1.95 | 5.94 | 10.71 | 5.72 | 2.405 | 0.6504 | 3.6 |
| **Gate Driver** | UCC27614 | UCC21520 | UCC27624 | UCC27517A (2) | UCC27524 | UCC21520 | UCC21551 | UCC27714 |

Table 3-1 also highlights some of the gate drivers used for these various switches. For SiC switching, isolated gate drivers such as the UCC21551 and the UCC21520 are used. This is due to the high voltage, power and switching frequencies needed for SiC FETs. For Si power switches, single or dual-channel gate drivers can be utilized depending on the topology. As seen for a boost circuit, a single-channel device such as the UCC27517A or the UCC27614 is needed to drive these power transistors. For dual-channel gate driver scenarios, the UCC27524 and the UCC27624 are often used. These scenarios include bridgeless boost and interleaved boost PFCs. For applications where GaN FETs are utilized, drivers such as the UCC27517A, the UCC27624, and the UCC21222 are all capable of driving GaN FETs.

## 4 Summary

Power Factor Correction circuits require strategic design and product selection to achieve maximum efficiency. There are many components in each of these PFC topologies that factor into the efficiency of these circuits. Specifically, proper gate driver selection is key to maintaining maximum efficiency due to the losses incurred during switching transition time, which is handled by the driver. For this, there are needs for a variety of gate drivers, both isolated and non-isolated and both low-side and half-bridge as well as single-channel and dual-channel. Texas Instruments offers a wide variety of gate drivers to meet the needs of all of these circuits including isolated, low-side, and half-bridge gate drivers.

## 5 References


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- Texas Instruments, *Power Factor Correction (PFC) Circuit Basics* power supply design seminar.
- Texas Instruments, *An Interleaved PFC Preregulator for High-Power Converters* document.
- Texas Instruments, *A comparative analysis of topologies for a bridgeless-boost PFC circuit* analog design journal.
- Texas Instruments, *98.6% Efficiency, 6.6-kW Totem-Pole PFC Reference Design for HEV/EV Onboard Charger* design.
- Texas Instruments, *Power factor correction (PFC) topology comparison* video.
- Texas Instruments, *4-A/4-A single-channel gate driver with 5-V UVLO and negative input voltage handling* product page.
- Texas Instruments, *5-A/5-A dual-channel gate driver with 4-V UVLO, 30-V VDD and low prop delay* product page.
- Texas Instruments, *4-A, 600-V half bridge gate driver* product page.
- Texas Instruments, *4A/6A 5kVRMS dual-channel isolated gate driver with EN and DT pins for IGBT and SiC* product page.

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