Application Note

Increasing NVCD Battery Chargers' Discharge Current

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ABSTRACT

Battery-powered equipment like vacuum robots or speakers have load transient currents that can exceed a maximum discharge current specification of a battery charge IC's internal battery FET. This application note explains how to make sure that the battery charge IC can provide the needed system load.

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Trademarks

1 Introduction

Integrated FET (I-FET), NVDC switch-mode battery chargers with internal battery FETs between the system (SYS) and battery (BAT) pins are desired for their small PCB footprint. However, unlike battery charger controllers with customizable external FETs, the charger's internal FETs have fixed max current limitations due primarily to their $R_{DS(ON)}$ and small package. The internal battery FET's maximum discharge current from BAT to SYS might not be enough to provide the system load when the charger is in battery only mode. To alleviate this issue in some applications, the system load is connected directly to the battery. However, this configuration cannot take advantage of the NVDC's key features of accurate charge and termination current or ability to start up the system from a discharged battery. This application note explains how to make sure that battery charge IC can provide the needed system load.

2 IRMS Discharge Current

Many times, the battery FET's maximum discharge current is given as root mean square current (ARMS). RMS discharge current for pulsed system load with duty cycle D is computed by the following equation.

$$I_{\text{DCHRG-RMS}} = \sqrt{D} \times I_{\text{DCHRG-PK}} \quad (1)$$

As an example, if a charger's RMS discharge current is 6 A, the charger can safely sustain the peak discharge current, clamped to 10 A, as a function of system load duty cycle as shown in Figure 2-1.

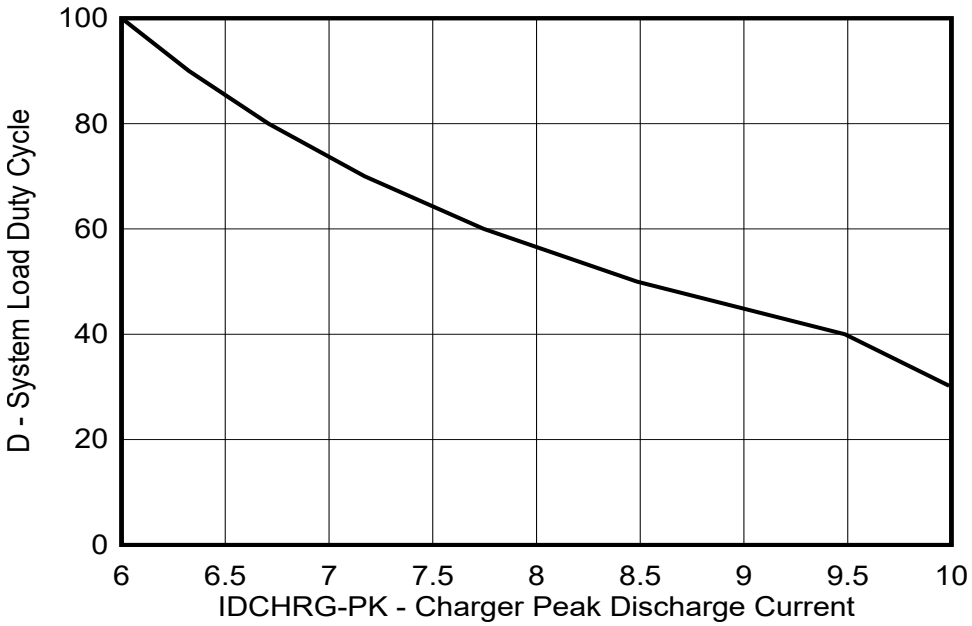

Figure 2-1. Peak Discharge Current vs. Duty Cycle

From the graph, if the system load duty cycle is only 40% at a fixed frequency, the internal battery FET's peak discharge current can be as high as 9A.

3 External Battery FET

Unfortunately, the system load duty cycle is not always known or varies significantly. So, adding an external battery PMOS FET (PFET) powered by the battery and in parallel with the charger's internal battery FET (BATFET) can be necessary. The external PFET turns on when the charger is in sleep or HiZ mode (for example, when the charger has no valid input power). The PFET does not turn on to provide supplement current if the converter enters DPM at maximum input power. The PFET's drain to source voltage rating, V_{DS}, must be higher than the difference between the charger's maximum SYS pin voltage (usually only slightly higher than the battery regulation voltage) and the minimum BAT pin voltage, which can zero if the pack protector opens. In addition, the PFET's gate to source voltage rating, V_{GS}, must be high enough to withstand the maximum battery voltage or a resistor divider or zener diode clamp must be added to protect the PFET's gate. The PFET's R_{DSon} must be at least as low as the internal battery FET RDSon if not lower. The FET's maximum threshold voltage ($V_{GSth\text{-}max}$) can also be at least 0.5 V below the lowest battery voltage that is expected to power the FET. For example, the BQ25798's BATFET has R_{DSon} of 8 mΩ typical. If the BQ25798 is configured for battery voltage up to 16.8 V maximum and not lower than 10 V minimum, Alpha and Omega's AONR21357 in 3 mm x 3 mm 8-DFN-EP package with R_{DSon} = 7.8 mΩ at V_{GS} = -10 V is a good choice for external, parallel BATFET for a 2S application. The PFET's source to gate pullup resistor (R_{PU}) must be sized large enough to reduce battery leakage (for example, in the MΩ range) when there is no load on SYS but not too large (for example, > 10 MΩ) for the FET's gate leakage (if significant) to cause a significant voltage drop.

4 Charger With $\overline{PG}$ and or Host GPIO

If the charger has an open drain power good ($\overline{PG}$) pin or the host has an available GPIO pin, turning on the external battery PFET, Q1, only requires a low cost NFET, Q2, like 2N7002. Alternatively, a host GPIO can be used or diode OR'd with /PG to also drive Q2's gate.

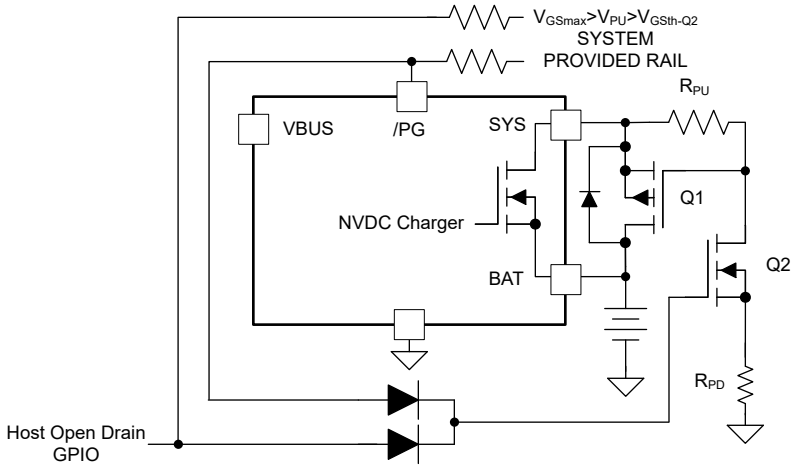

Figure 4-1. Implementation Using Charger's $\overline{PG}$ Pin and or Host GPIO Pin

If the maximum SYS voltage [V(SYS)max] is higher than Q1's maximum V_{GS} voltage ($V_{GSmax\text{-}Q1}$), the pull down resistor R_{PD} can be sized, using the equations below, to protect Q1. These resistors eliminate the need for a Zener diode clamp in case V(SYS)max is greater than $V_{GSmax\text{-}Q1}$.

$$V_{GS(MAX)-Q1} > \frac{R_{PU}}{R_{PU}+R_{PD}} \times V_{SYS} \quad (2)$$

$$V_{PU} - 0.6V - V_{GSth(MAX)-Q2} > \frac{R_{PD}}{R_{PU}+R_{PD}} \times V_{SYS} \quad (3)$$

If V(SYS)max is not higher then $V_{SGmax\text{-}Q1}$, R_{PD} can be zero ohms.

5 Buck-only Charger

If no $\overline{PG}$ pin is available, the charger is always bucking (for example. input voltage > battery voltage + PFET's V_{GSth}) and the maximum system (battery) voltage is below $V_{GSmax-Q1}$, the input voltage can be used to directly drive the PFET's gate, as shown in Figure 5-1.

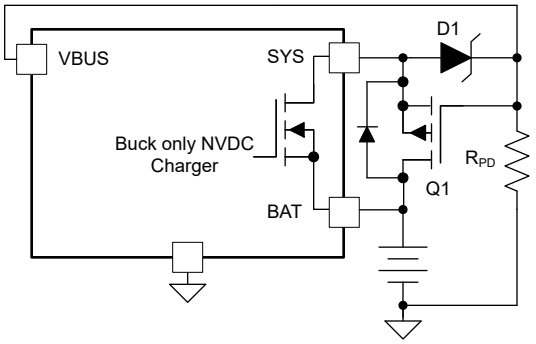

Figure 5-1. Implementation Using a Buck-only Charger

The Zener diode clamp, D1, from the PFET's source to gate is only necessary if the charger's input voltage is higher than the $V_{SGmax-Q1}$. If this configuration, R_{PD} provides current limiting for D1 in forward mode, for example, when no VBUS is applied.

6 Boosting Charger

If the charger only boosts or boosts and bucks, an additional IC is needed to drive the external PFET's gate low when input power is removed. A comparator determines when the input voltage has been removed. The comparator needs a reference for the negative input to compare to the charger's input voltage. The reference does not have to be extremely accurate, must be present when the charger's input voltage is not present and does not need to provide any significant current. $\overline{QON}$, powered by the higher of the input or battery voltage, can be used as this reference as long as the charger's minimum operating input voltage is above the $\overline{QON}$ maximum voltage [$V(\overline{QON})_{MAX}$], of 3.3V. As soon as the input voltage drops below $V(\overline{QON})$, the comparator turns on the PFET. TLV1861 is a comparator with up to 40V input (up to a 9S battery pack), quiescent current of 440nA typical and open drain output.

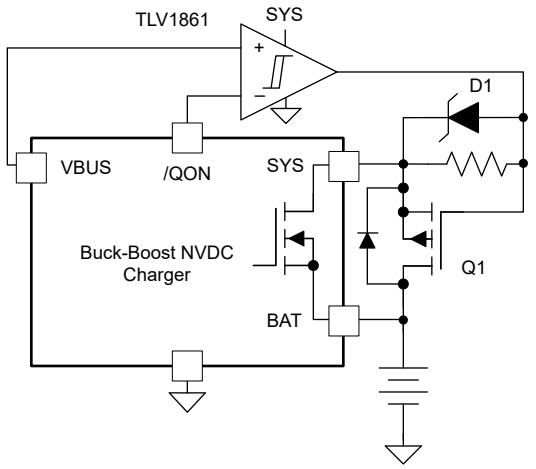

Figure 6-1. Implementation for Boosting Charger

The Zener diode clamp, D1, from the PFET's source to gate is only necessary if the battery voltage is higher than the PFET's max V_{GS}.

7 Summary

Adding an external battery in parallel with an I-FET charger's internal battery FET is an easy way to increase the charger's battery discharge current capability. Note in all three cases, some battery current is required for the pull up resistor and, in the last case, the comparator. Choosing a PFET with high V_{GSmax} (commonly ±20 V) is also recommended. Any battery discharge current detection or protection provided by the internal battery FET is no longer valid due to the extra current flowing through the external FET. If long battery life (low leakage) is critical for the application, then a charger or charge controller with external battery FET or connecting the load directly to the battery can be better options.

8 References

- Texas Instruments,*BQ25798 I2C Controlled, 1- to 4-Cell, 5-A Buck-Boost Battery Charger with Dual-Input Selector, MPPT for Solar Panels and Fast Backup Mode*, data sheet.
- Texas Instruments, *TLV185x and TLV186x Family of 40 V, Nanopower Comparators*, data sheet.
- Alpha & Omega, *AONR21357 – 30V P-Channel MOSFET*, data sheet.

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