Application Note

How to do Co-Layout Between SOT-563 Package and SOT-236 Package

Lucia Gao, Edwin Zang, Junjie Mai

ABSTRACT

Co-layout is more and more required in Buck converters applications due to the advantage of design flexibility. This application note focuses on how to co-lay between TPS56x242/7, TPS56x202/3/6/7 with SOT-563 package and TPS56x201/8 with SOT-236 package. First, the pin-out is compared. Next, the schematic design and layout consideration are introduced. Finally, a co-layout design example is given and this application design is verified based on experiments.

Table of Contents

List of Figures

List of Tables

Trademarks

D-CAP3™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

The TPS56x242/7, TPS56x202/3/6/7 are single, adaptive on-time, D-CAP3™ control mode, synchronous buck converters that requires a very low external component count. The D-CAP3 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. TPS56x201/8 star parts series including: TPS561201/8, TPS562201/8, TPS563201/8, TPS564201/8, and TPS565201/8 which have been widely used in DTV, STB, surveillance, networking home terminal, and so on. Co-layout is more and more required in Buck converters applications due to the advantage of design flexibility. This application report mainly discusses how to do co-layout between TPS56x242/7, TPS56x202/3/6/7 and TPS56x201/8.

2 Comparison of Pin-out

Figure 2-1 shows TPS56x242/7 pin-out with SOT-563 package which has been optimized. It integrates BST pin and add AGND for pin 4. Figure 2-2 shows TPS56x201/8 pin-out with SOT-236 package which is different from TPS56x242/7. Figure 2-3 shows TPS56x202/3/6/7 pin-out with SOT-563 package. Both packages and pin locations are different for these three families. VBST pin of TPS56x201/8 and TPS56x202/3/6/7 is used to supply input for the high-side NFET gate driver circuit. AGND pin of TPS56x242/7 is the ground of internal analog circuitry.

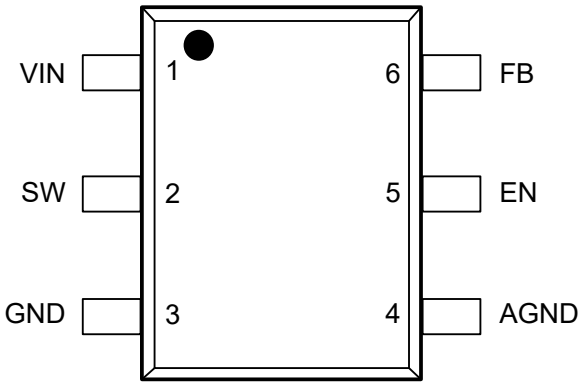

Figure 2-1. TPS56x242/7 Pin-out

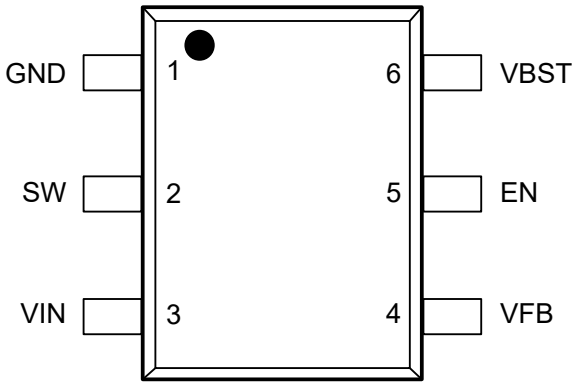

Figure 2-2. TPS56x201/8 Pin-out

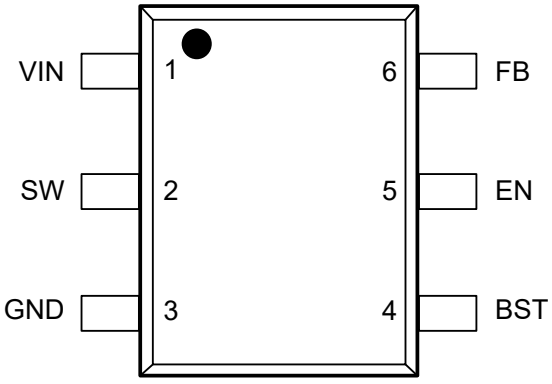

Figure 2-3. TPS56x202/3/6/7 Pin-out

Table 2-1. Pin Functions

Pin				Description
Name	NO.			
	TPS56x242/7	TPS56x202/3/6/7	TPS56x201/8	
VIN	1	1	3	Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.
SW	2	2	2	Switch node pin. Connect the output inductor to this pin.
GND	3	3	1	GND pin source terminal of the low-side power NFET as well as the ground terminal for controller circuit.
FB	6	6	4	Converter feedback input. Connect to the output voltage with a feedback resistor divider.
EN	5	5	5	Enable input control. Driving EN high enables the converter.
VBST	NA	4	6	Supply input for the high-side NFET gate driver circuit. Connect 0.1-uF capacitor between VBST and SW pins.
AGND	4	NA	NA	Ground of the internal analog circuitry. Connect AGND to the GND plane.

3 Schematic Diagram

Since packages and pin locations are different for TPS56x242/7 and TPS56x201/8, the compatible schematic is designed to achieve co-lay. Figure 3-1 shows the co-lay schematic. There are several differences for the BOM. Table 3-1 shows solder information for different part.

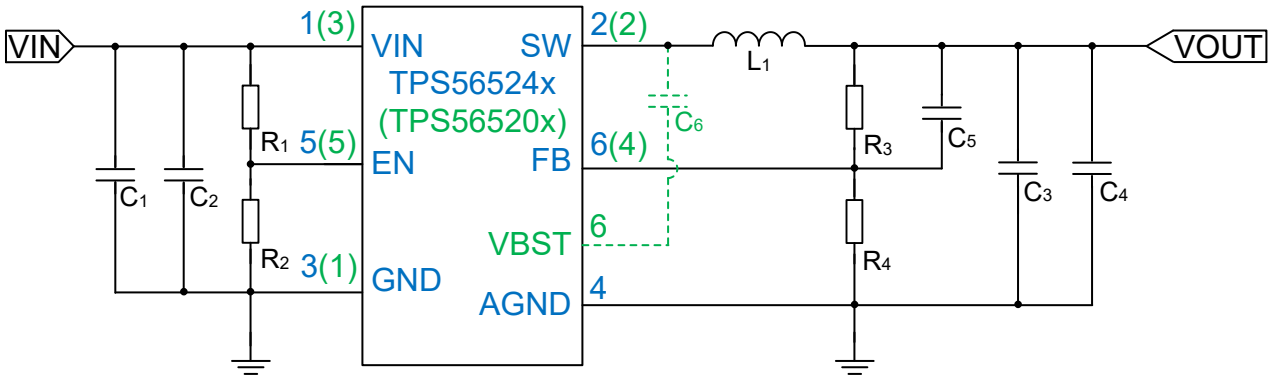

Figure 3-1. Schematic Diagram to Achieve Co-lay

Table 3-1. Solder Information for Different Part

Part Number	Description
TPS56x242/7	C_6 needs to be floating. EN pin max voltage is 6 V.
TPS56x201/8	C_6 needs to be soldered. EN pin max voltage is 19 V.

4 Layout Consideration

TPS56x242/7 is SOT-563 package which is 1.60 mm × 1.60 mm and TPS56x201/8 is SOT-236 package which is 1.60 mm × 2.90 mm. The body size of TPS56x201/8 is bigger than TPS56x242/7. When doing co-layout, the relative positions between SOT-236 device and SOT-563 devices needs to be considered and comply with manufacturer's rules. There are two types of co-layout design. Figure 4-1 shows the mirror symmetrical co-layout design. This type of design needs to put one part on the front and another on the back of the board. The pin-out can match well with each other and follow with layout guidelines. Vias are required for VIN, SW and GND pin according to the load current. Figure 4-2 shows the piggyback co-layout design. This type of design can put both parts on same side of the board. Please make sure that the input capacitors of both devices are placed as close to the VIN pin to minimize trace impedance.

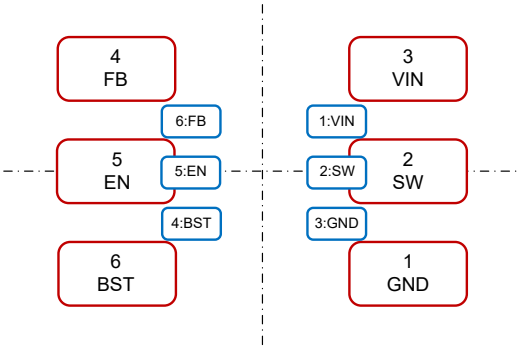

Figure 4-1. Type 1 – Mirror Symmetrical Co-layout for TPS56x201/8 and TPS56x202/3/6/7

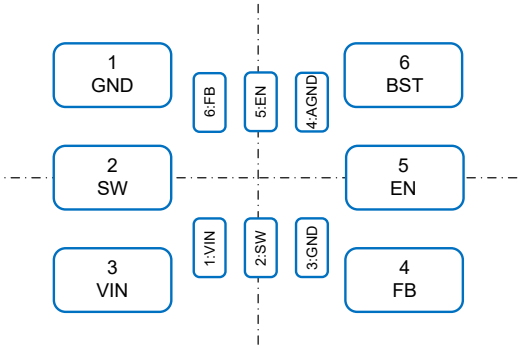

Figure 4-2. Type 2 – Piggyback Co-layout for TPS56x201/8 and TPS56x242/7

The recommend type 1 and type 2 co-layout design are shown in Figure 4-3 and Figure 4-4. For type 2, the input capacitor is placed as close as possible to VIN pin. Voltage feedback loop is placed away from the high-voltage switching trace and has ground shield. The trace of the FB node is as small as possible to avoid noise coupling. When soldered with TPS565201, the switching trace is short and wide enough. When soldered with TPS565242, the switching trace goes through from the top layer to the bottom layer then back to the top layer with the connecting inductor. Please keep in mind that do not allow switching current to flow under the device.

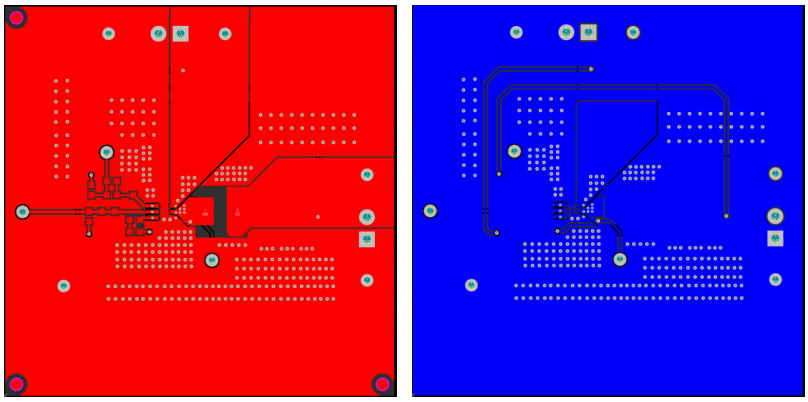

Figure 4-3. Type 1 Co-layout EVM

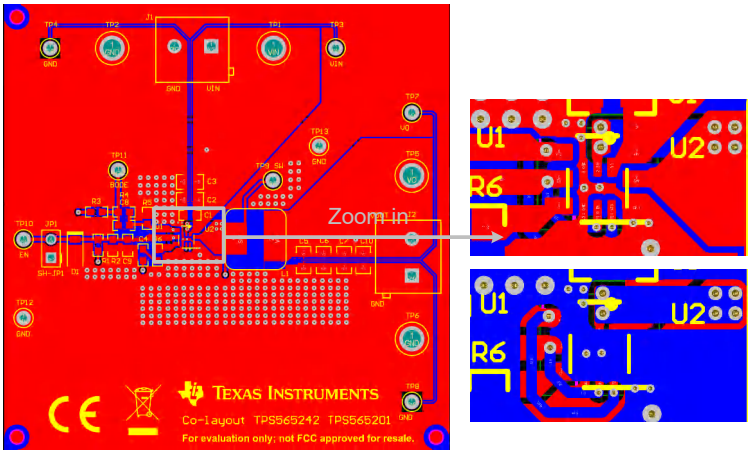

Figure 4-4. Type 2 Co-layout EVM

5 Experimental Verification

This topic gives experimental verification of Type 2 co-layout design. The BOM of the co-layout board is the same as TI EVM board.

Figure 5-1 and Figure 5-2 show the board layout for the co-layout design.

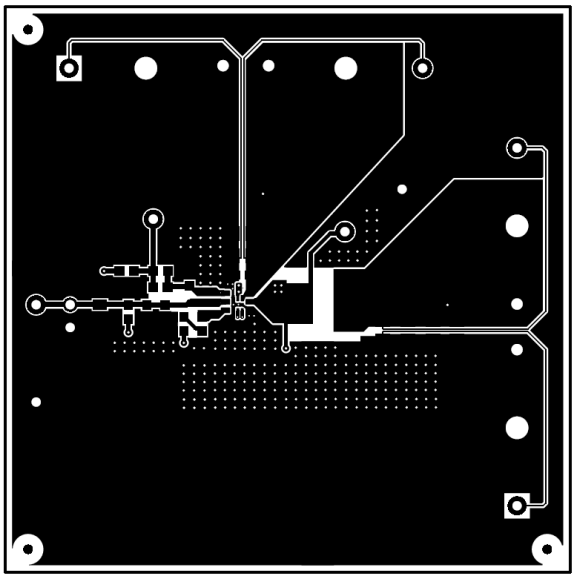

Figure 5-1. Co-layout Design Top Layer

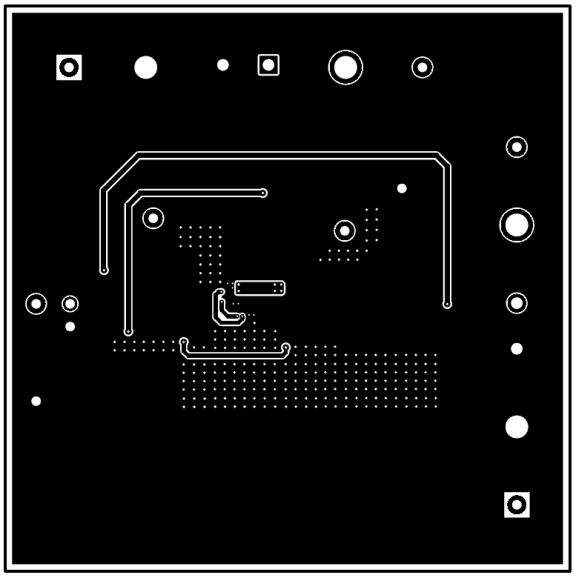

Figure 5-2. Co-layout Design Bottom Layer

Figure 5-3 and Figure 5-4 shows the output voltage ripple of EVM board and co-layout board with TPS565242. Figure 5-5 and Figure 5-6 shows the output voltage ripple of EVM board and co-layout board with TPS565201. The results show that co-layout board with both TPS565201 and TPS565242 can work well.

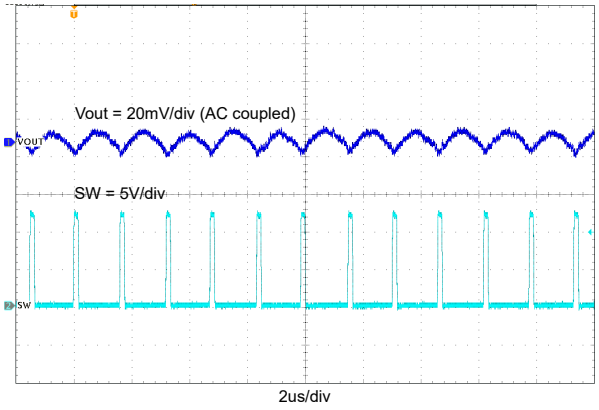

Figure 5-3. EVM Board with TPS565242 Output Ripple, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

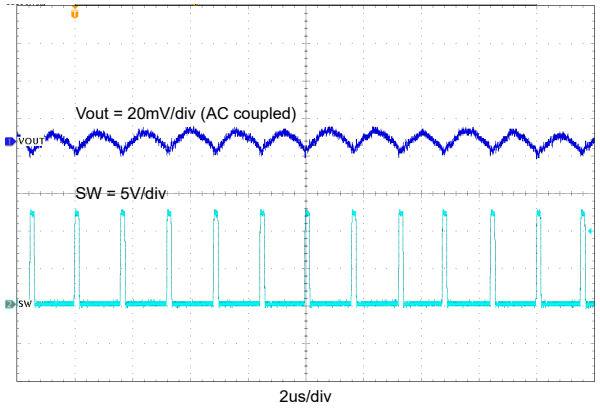

Figure 5-4. Co-layout Board with TPS565242 Output Ripple, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

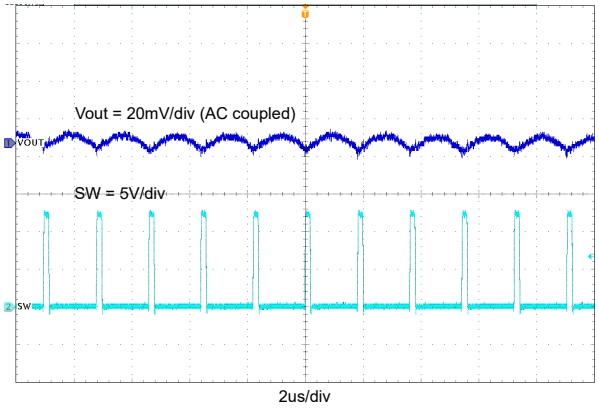

Figure 5-5. EVM Board with TPS565201 Output Ripple, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

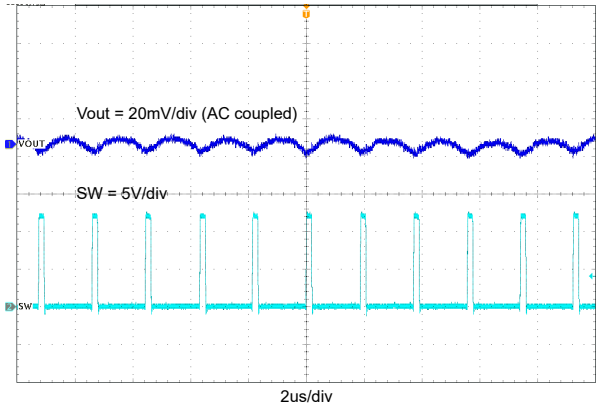

Figure 5-6. Co-layout Board with TPS565201 Output Ripple, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

Efficiency comparison between EVM and co-layout board which are tested at 1.05 V_{out} and 5 V_{out} are shown in Table 5-1. From the effciency results, it shows that the efficiency of co-layout board is slightly lower than EVM board.

Table 5-1. Efficiency Comparison between EVM and Co-layout Board, V_{IN} = 12 V, I_{OUT} = 5 A

	V_{out} (V)	Efficiency	V_{out} (V)	Efficiency
TPS565242 EVM board	1.05	84.2%	5	94.8%
TPS565242 Co-lay board	1.05	83.5%	5	94.4%
TPS565201 EVM board	1.05	77.3%	5	92.3%
TPS565201 Co-lay board	1.05	77.0%	5	92.2%

Switching spike voltage comparison between EVM and co-layout board which are tested at 1.05 V_{out} are shown in Table 5-2. From the switching spike results, it shows that co-layout board is slightly worse than EVM board.

Table 5-2. Switching Spike Comparison between EVM and Colay Board

	V_{in} (V)	V_{out} (V)	I_{out} (A)	Switching spike voltage (V)
TPS565242 EVM board	12	1.05	5	12.0
TPS565242 Co-lay board	12	1.05	5	12.4
TPS565201 EVM board	12	1.05	5	13.2
TPS565201 Co-lay board	12	1.05	5	14.7

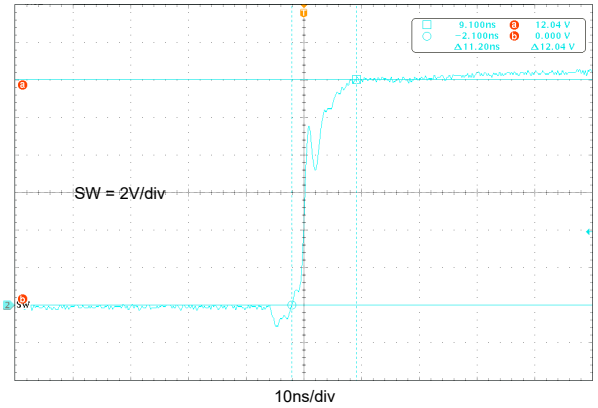

Figure 5-7. EVM Board with TPS565242 Switching Spike, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

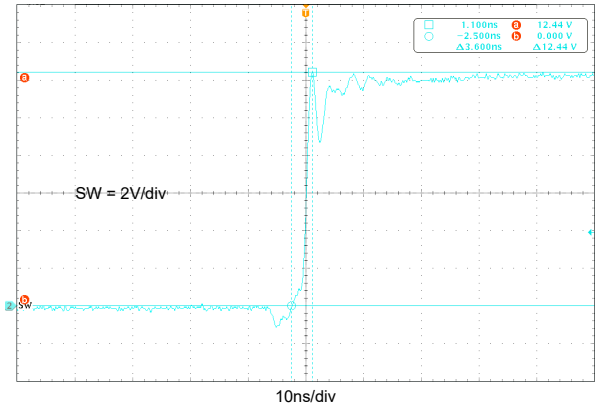

Figure 5-8. Co-layout Board with TPS565242 Switching Spike, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

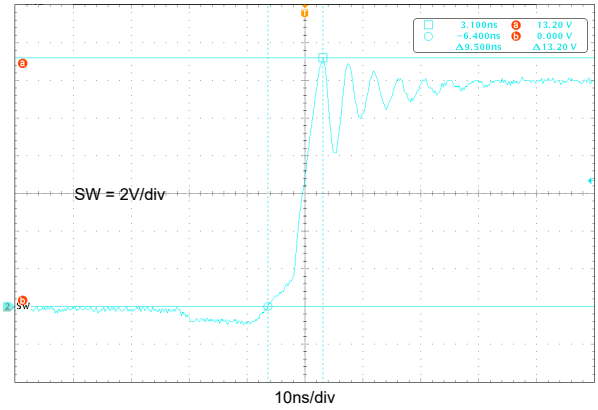

Figure 5-9. EVM Board with TPS565201 Switching Spike, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

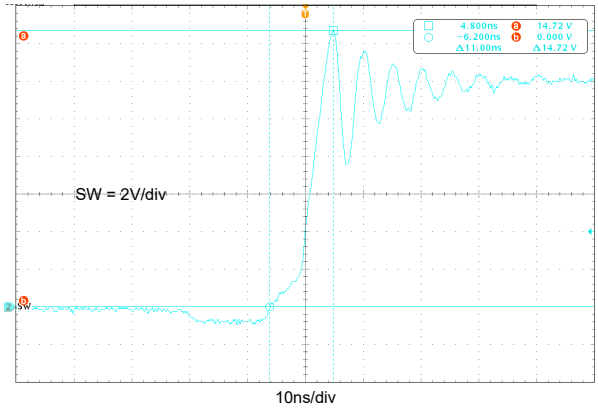

Figure 5-10. Co-layout Board with TPS565201 Switching Spike, V_{IN} = 12 V, V_{OUT} = 1.05 V, I_{OUT} = 5 A

Figure 5-11 and Figure 5-12 shows the co-layout board with TPS565242 transient response with 0.1 A to 2.5 A and 1.25 A to 3.75 A. The current steps slew rate is set as 0.8 A/us.

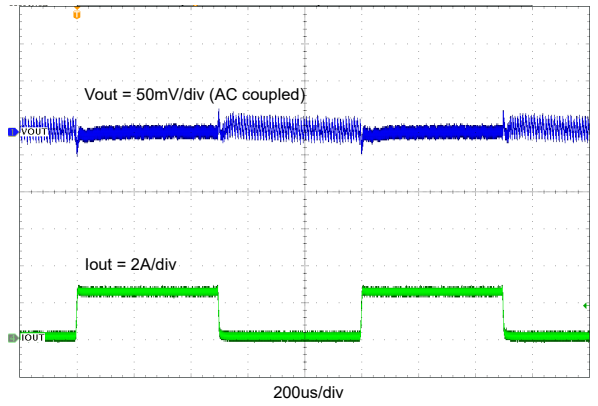

Figure 5-11. Co-layout Board with TPS565242 Transient Response, V_{IN} = 12 V, V_{OUT} = 1.05 V, 0.1 A - 2.5 A

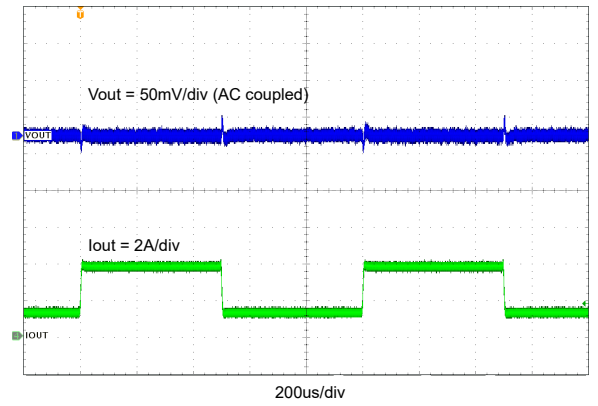

Figure 5-12. Co-layout Board with TPS565242 Transient Response, V_{IN} = 12 V, V_{OUT} = 1.05 V, 1.25 A - 3.75 A

Figure 5-11 and Figure 5-12 shows the co-layout board with TPS565201 transient response with 0.1 A to 2.5 A and 1.25 A to 3.75 A. The current steps slew rate is set as 0.8 A/us.

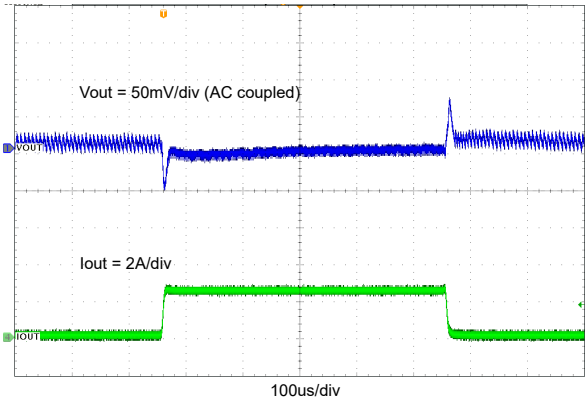

Figure 5-13. Co-layout Board with TPS565201 Transient Response, V_{IN} = 12 V, V_{OUT} = 1.05 V, 0.1 A - 2.5 A

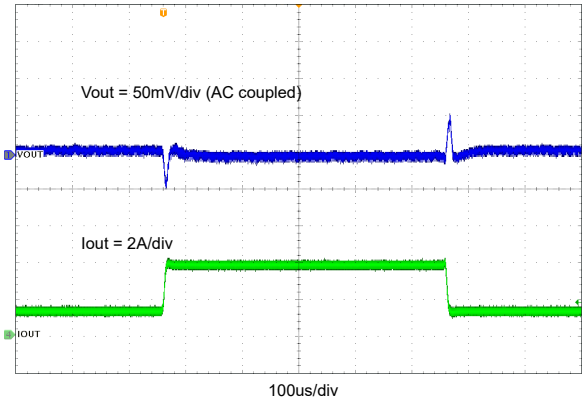

Figure 5-14. Co-layout Board with TPS565201 Transient Response, V_{IN} = 12 V, V_{OUT} = 1.05 V, 1.25 A - 3.75 A

6 Summary

This application note introduces how to co-layout between TPS56x242/7 with SOT-563 package and TPS56x201/8 with SOT-236 package. Pin-out is compared and layout recommendations are given. Finally, the application note shows the experiment verification results of the co-layout design. From the test results, both TPS56x242/7 and TPS56x201/8 can work well with co-layout board.

7 References

- Texas Instruments, *TPS56524x 3-V to 16-V Input Voltage, 5-A Synchronous Buck Converter in SOT-563 Package* data sheet.
- Texas Instruments, *TPS56424x 3-V to 16-V Input Voltage, 4-A Synchronous Buck Converter in SOT-563 Package* data sheet.
- Texas Instruments, *TPS565201 4.5-V to 17-V Input, 5-A Synchronous Step-Down Voltage Regulator* data sheet.
- Texas Instruments, *TPS564201 4.5-V to 17-V Input, 4-A Synchronous Step-Down Voltage Regulator* data sheet.

8 Revision History

Changes from Revision * (December 2022) to Revision A (July 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added mirror symmetrical co-layout design	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265