Application Report
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Design Considerations With Dual-Channel SR Controller UCC24624

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ABSTRACT

The UCC24624 is a high-performance synchronous rectifier (SR) controller for LLC resonant converter applications. It integrates two channels of SR control into a single 8-pin SOIC package, minimizes the external components, and simplifies PCB layout. Many features make the UCC24624 device a good choice for the high-efficiency LLC solutions, including proportional gate drive, adjustable turn-off threshold, two-channel interlock, automatic standby mode transition, and so forth. A common use of the UCC24624 is to implement it with the LLC controller UCC25640x or a single digital controller in the primary side, used in industrial AC/DC, server PSU and telecom power applications. To accelerate the design process with the UCC24624, several common questions or concerns are discussed in this report.

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1 Gate Driving Capability

In higher power level applications, SR MOSFETs are configured in parallel, to achieve lower on-state resistance, which results in lower conduction loss and better efficiency. Meanwhile, the amplitude of the gate driver voltage V_{GS} determines the actual drain-source on-state resistance ($R_{DS(on)}$) of the MOSFET. Taking the MOSFET IPB072N15N3 as an example, Figure 1 shows the relationship between $R_{DS(on)}$ and different V_{GS} amplitudes.

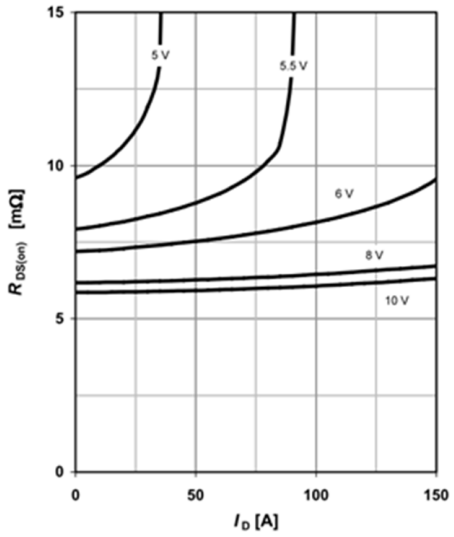

Figure 1. IPB072N15N3 Drain Source On-Resistance

Ideally, with the internal linear regulator, the UCC24624 device can clamp the gate driver voltage to a maximum level of 11 V with the VDD supply voltage above 11 V. This minimizes the conduction loss for MOSFETs. However, the SR MOSFET is only driven high with the full driving capability of the UCC24624 of 1.5 A during its minimum pullup time t_{MGPU} (typically 275 ns). After that, the SR MOSFET gate is kept high by a weak current source of approximately 200 µA. Thus, it is helpful to check what the final amplitude of V_{GS} can reach during the UCC24624 t_{MGPU} interval, especially in the applications where several SR MOSFETs are in parallel.

See the *Fundamentals of MOSFET and IGBT Gate Driver Circuits Application Report*, before being turned on by UCC24624, the SR MOSFET body diode conducts first. The drain-to-source voltage V_{ds} equals the body diode forward voltage drop. At that moment, the parasitic capacitances C_{GD} and C_{DS} are actually discharged to 0. Also, the Miller effect is not present. Thus, the full driving process is to raise the voltage across C_{GD} and C_{DS} capacitors from 0 V to the final VGS level. Taking 3 IPB072N15N3 MOSFETs in parallel as an example, a simple simulation method with Simplis is discussed as follows.

According to the dynamic characteristics in the IPB072N15N3 data sheet, the input capacitance C_{iss} = 5.47 nF, the gate resistance R_G = 2.3 Ω. If using the UCC24624 to directly drive 3 IPB072N15N3 devices, the simulation circuit is shown in Figure 2.

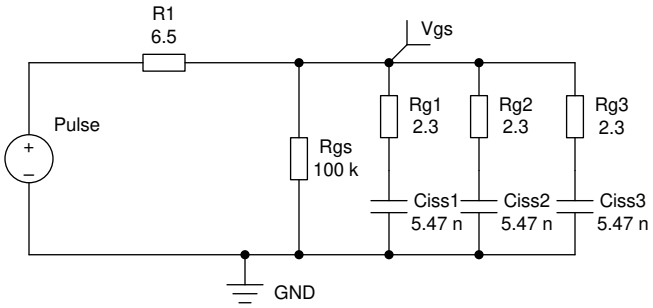

Figure 2. Driving Capability Simulation Circuit

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The pulse source is a 275-ns width pulse with an amplitude of 11 V. R1 = 6.5 Ω refers to the VG pullup resistance inside UCC24624, as shown in Table 1. Note that R_{gs} = 100 kΩ is selected, which is a bit larger than normal applications. Traditionally, this resistor is used to discharge the charge built up on the SR gate. Due to the weak pullup current in UCC24624, this resistor needs to have much larger value than the traditional 10-kΩ pulldown. The 100-kΩ resistance together the internal 200 µA allows the SR gate to remain at 11-V driving voltage level, after the minimum pullup time, t_{MGPU}. The resistance is so large that it does not affect the pullup capability.

Table 1. UCC24624 Gate Driver Characteristics(1)

Parameter		Test Conditions	MIN	TYP	MAX	Unit
R_{VG_PU}	VG pullup resistance		3.5	6.5	11.25	Ω
R_{VG_PD}	VG pulldown resistance		0.2	0.9	1.5	Ω
VG_{HI}	VG high clamp level	I_{VG} = 0 mA	9.95	10.9	11.68	V

(1) At V_{VDD} = 12 VDC, C_{VG1}= C_{VG2} = 0 pF, C_{REG} = 2.2 µF V_{VD1} = V_{VD2} = 0 V, –40°C ≤ T_J = T_A ≤ +125°C

Figure 3 shows the simulation result of the driving capability, indicating that V_{gs} can be driven up to 10.1 V within the t_{MGPU} interval, which is high enough to ensure minimum $R_{DS(on)}$ during conduction. Observing the $R_{DS(on)}$ vs. V_{gs} curve, it can be seen when the gate voltage is above 8 V, the $R_{DS(on)}$ reduction becomes relatively small.

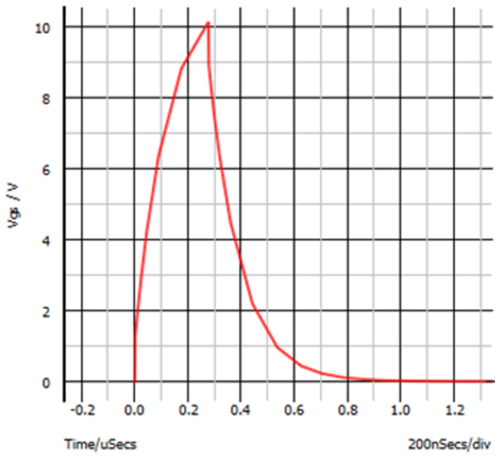

Figure 3. Simulation Result of the Driving Capability

2 UCC24624 Power Loss Estimation

Since UCC24624 is used in LLC converters with high-switching frequency, it is important to evaluate its thermal performance. Ensure the UCC24624 device is operating within its thermal safety-related conditions. The power loss of UCC24624 can be estimated by two main portions.

The first portion is the static power loss P_Q. The I_{VDDRUN} = 1.1 mA referring to the run mode is selected here. Assuming V_{VDD} is supplied by 12 V, the P_Q can be calculated with Equation 1:

$$P_Q = V_{VDD} \times I_{VDDRUN} = 13.2 \text{ mW} \quad (1)$$

The second one is switching operation loss P_{DRV}. The total dynamic loss P_{SW}, due to charging or discharging the C_{ISS} capacitor, can be calculated as Equation 2 shows:

$$P_{SW} = 2 \times Q_g \times V_{gs} \times f_{sw} \times N \quad (2)$$

where

- Q_g is the gate charge of the MOSFET
- f_{sw} is the gate-drive frequency
- N is the number of the MOSFET in parallel

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Using the example application in Section 1, and assuming the LLC frequency is 200 kHz, the calculated result:

$$P_{SW} = 2 \times 70\ \text{nC} \times 10.1\ \text{V} \times 200\ \text{kHz} \times 3 = 848\ \text{mW} \quad (3)$$

P_{SW} is dissipated in the gate drive circuits, including the driver output impedances, the external gate resistor and the internal gate mesh resistance, so P_{DRV} can be expressed

$$P_{DRV} = \frac{P_{sw}}{2} \times \left(\frac{R_{VG\_PU}}{R_{VG\_PU} + R_{gate} + R'_g} + \frac{R_{VG\_PD}}{R_{VG\_PD} + R_{gate} + R'_g} \right)$$

where

- Pullup resistance R_{VG_PU} = 6.5 Ω
- Pulldown resistance R_{VG_PD} = 0.9 Ω (4)

According to Table 1; R_{gate} refers to the external gate resistor, and takes 0 in this example. R'_g is the equivalent resistance of 3 IPB072N15N3 in parallel, 2.3 Ω / 3 = 0.76 Ω.

Thus, P_{DRV} in this case can be calculated as

$$\frac{848\ \text{mW}}{2} \times \left(\frac{6.5}{6.5 + 0.7} + \frac{0.9}{0.9 + 0.76} \right) = 609\ \text{mW} \quad (5)$$

Therefore, the total power loss dissipated in UCC24624 is

$$P_{LOSS} = P_Q + P_{DRV} = 622.2\ \text{mW} \quad (6)$$

According to the *Semiconductor and IC Package Thermal Metrics Application Report*, the junction temperature (T_J) of the UCC24624 can be estimated with Equation 7:

$$T_J = T_{PCB} + \Psi_{JB} \times P_{LOSS} \quad (7)$$

or

$$T_J = T_C + \Psi_{JT} \times P_{LOSS}$$

where

- T_{PCB} is the board temperature measured by an IR camera or fiber optic probe
- T_C is the UCC24624 case-top temperature measured with a thermocouple or some other instrument
- Ψ_{JB} is the junction-to-board characterization parameter
- Ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table (8)

Note that using Ψ_{JB} and Ψ_{JT}, instead of the junction-to-ambient thermal resistance $R_{\Theta JA}$, can greatly improve the accuracy of the junction temperature estimation, they are experimentally derived by assuming that the amount of energy leaving the IC will be similar in both the testing environment and the application environment.

As long as the recommended layout guidelines are observed, with Ψ_{JB} = 52.8°C/W and the max T_J = 125°C, the maximum PCB temperature can be estimated as

$$T_{PCB} = T_J - \Psi_{JB} \times P_{LOSS} = 125 - 52.8 \times 0.6222 = 92.1^{\circ}\text{C} \quad (9)$$

If external resistors are used, a portion of the power loss is incurred on the external resistors and the power loss in UCC24624 could be lower, allowing the device to operate at a higher temperature environment. For example, if R_{gate} = 2.2 Ω, the total power loss P_{DRV} is decreased to 403 mW, and it can support the maximum PCB temperature of 103.7°C.

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3 Turn-off Threshold Adjustment

As Figure 4 shows, the V_{DS} voltage of the SR MOSFET sensed by UCC24624 V_{SENSE} is the combination of the MOSFET on-state resistor voltage drop VSR, together with the voltage drops on parasitic inductors L_D and L_S. Thus, V_{SENSE} can be represented with Equation 10:

$$V_{SENSE} = -\left[I_{SR} \times R_{DS(ON)} + (L_D + L_S) \times \frac{dI_{SR}}{dt}\right] \quad (10)$$

During the SR current falling edge, the fast current slope (di/dt) creates a significant negative voltage drop across the package inductance and offset V_{SR}, causing the SR controller to detect a smaller voltage drop and turn off the SR MOSFET early, as Figure 5 shows.

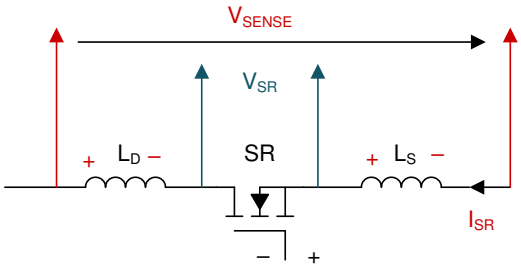

Figure 4. UCC24624 Sensed Voltage

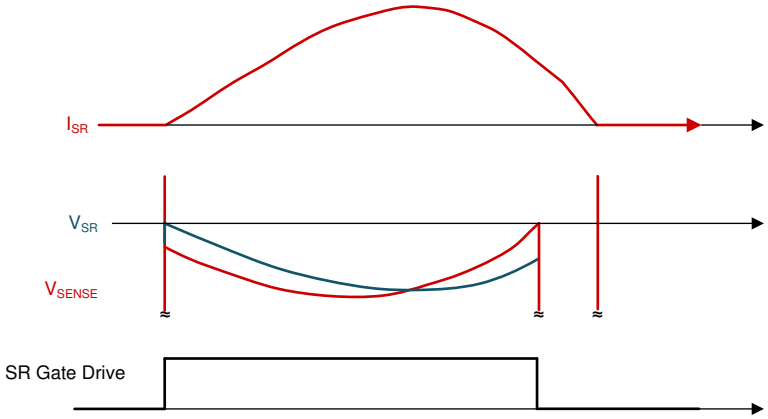

Figure 5. SR Early Turn Off

To compensate the effect of parasitic inductances, the turn-off threshold of the UCC24624 device is 10.5 mV by default, instead of typically being set as a negative threshold, since the positive voltage is always expected at zero SR current. However, with different packages for the MOSFET, this parasitic inductance could vary from 2 nH to 10 nH, and some applications might induce more parasitic inductors due to undesirable layout, so it is required to further increase the turn-off threshold to accommodate higher parasitic. As demonstrated in the *UCC24624 Dual-Channel Synchronous Rectifier Controller for LLC Resonant Converters Data Sheet*, by connecting a resistor R_{offset} from the VSS pin to the SR MOSFET source, the voltage drop across the external resistor increases the turn-off threshold. In this way, the desired turn-off threshold V_{THOFF} can be calculated as:

$$V_{THOFF} = 10.5 \text{ mV} + 330 \text{ } \mu\text{A} \times R_{offset} \quad (11)$$

Normally, less than 70-mV offset is recommended for TO-220 MOSFET packages. Due to different layout conditions in actual applications, it is recommended to adjust the R_{offset} value to maximize the SR MOSFET conduction time.

In some applications, some users would like to use a lower turn-off threshold than 10.5 mV. It is also possible to achieve it with the example circuits shown in Figure 6.

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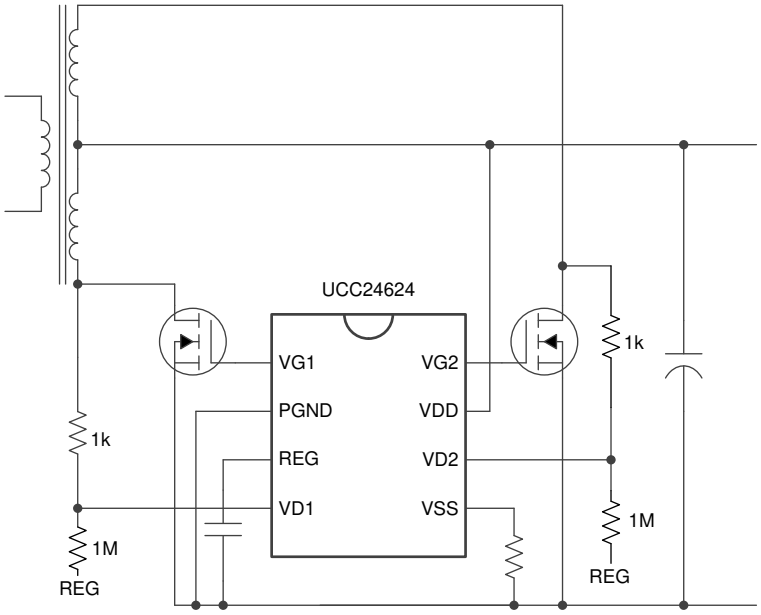

Figure 6. Decreasing Turn-off Threshold Circuit

In Figure 6, a 1-MΩ resistor is added from REG pin to VD pins. When the SR MOSFET is on, its drain voltage is close to 0 V, since the REG pin voltage is well regulated to 11 V, the added 1-MΩ resistor creates an offset current of approximately 11 µA from REG pin. In this example, another 1-kΩ resistor is added from MOSFET drain to the UCC24624 VD pin. The 11-µA current creates an 11-mV offset voltage on the 1-kΩ resistor, which changes the turn-off threshold from 10.5 mV to –0.5 mV. Using this circuit with different resistor values can create other turn-off thresholds. When the SR turns off, the high voltage appears on SR drain pin. This will not cause current flowing into the UCC24624 VD pin. However, because this voltage is much higher than the 11-V REG pin voltage, this could cause a current flowing from SR drain to REG. A diode can always be inserted to prevent the current but it adds extra system cost. To minimize this current, it is desired to keep the 1-MΩ resistor with relative high value.

4 Light Load Operation

In some designs, LLC enters PWM mode with reduced duty cycle or burst mode to save the switching loss during light load. The UCC24624 device detects the average operation frequency of channel 1 SR MOSFET and enters standby mode operation with no gate driver signals. It also reduces its current consumption to minimize the overall control loss. The light load mode detection interval is 7.5ms. If the detected average switching frequency drops below 9 kHz, the UCC24624 enters standby mode. Once it is detected more than 15.6 kHz, the SR driving is enabled again.

Note that for the purpose of noise immunity, after the SR is turned on, a minimum on-time blanking of 475 ns is implemented in the UCC24624. The SR keeps conducting regardless of its drain-to-source voltage. During light load operation, the duty cycle of LLC primary side might decease so much that there is not enough energy delivered to the secondary side. Thus, the minimum on-time of the UCC24624 might cause the SR MOSFETs to conduct longer than it is needed and induce a negative current from the output.

Considering such conditions, adaptive turn-on delay scheme takes effect to resolve the issue: UCC24624 monitors the SR conduction time all the time, and once its conduction time becomes less than the minimum on-time, UCC24624 increases the turn-on delay from 155ns to 275ns. Meanwhile, the minimum on-time decreases to 355ns to support light load operation, as shown in Figure 7. Additionally, the longer turn-on delay can provide better DCM ring rejection capability to avoid false turn on due to SR parasitic capacitance. Meanwhile, the minimum gate pullup time also decreases from 275 ns to 155 ns. Therefore, the final VGS amplitude could be lower than its value at heavy load conditions This further helps to reduce the switching loss during light load.

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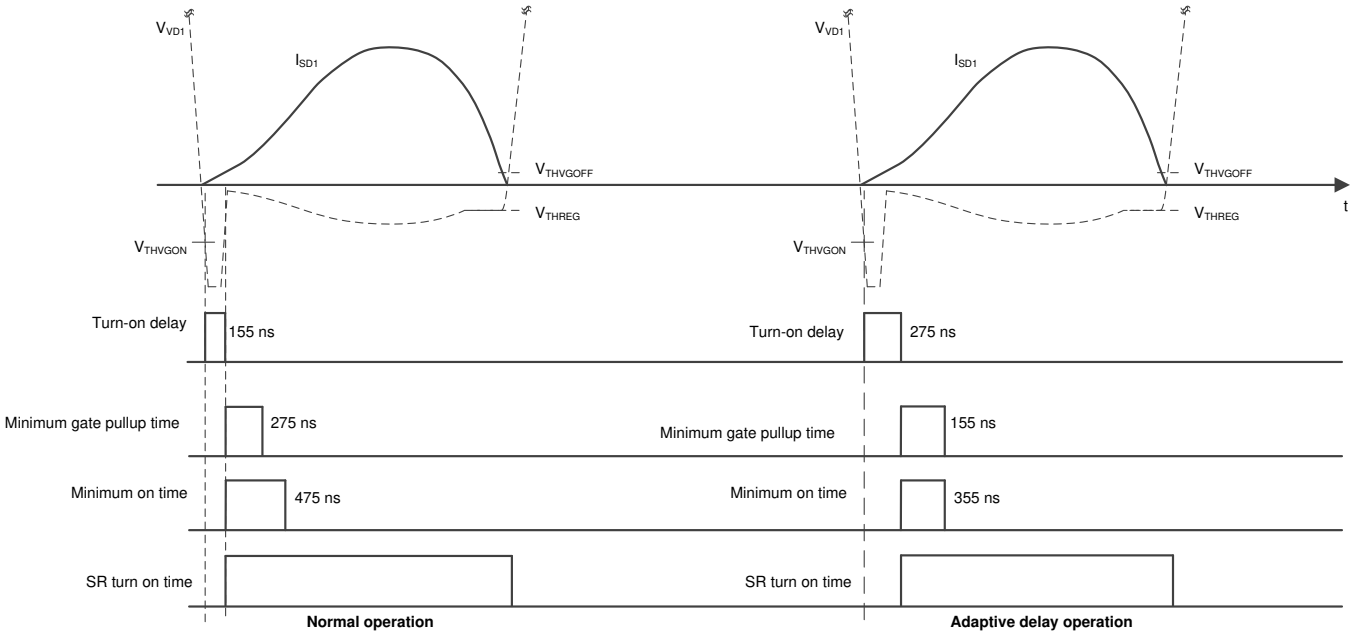

Figure 7. Adaptive Turn-on Delay

Another solution to further increase the turn-on delay and improve the noise immunity is to add an RC filter on VD pins, as Figure 8 shows. Note that the value of this RC filter should be carefully selected, since the added turn-on delay also increases the conduction loss during normal operation. A 1-kΩ resistor and < 100-pF capacitor are suggested. Besides, during some noise conditions, due to large parasitic inductances, the RC filter can also help absorb voltage spikes or negative current, so as to avoid the effect for the internal parasitic diode of UCC24624.

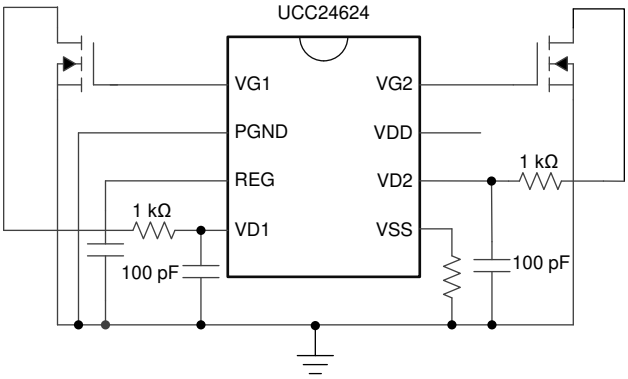

Figure 8. Adding RC Filter at VD Pins

5 References

- Texas Instruments, *Fundamentals of MOSFET and IGBT Gate Driver Circuits Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, UCC24624 LLC gated driver evaluation Module
- Texas Instruments, TIDA-010081: >95% Efficiency, 1-kW analog control AC/DC reference design for 5G telecom rectifier reference design
- Texas Instruments, TIDA-010038: 94% Peak efficiency, 150W norm, 240W peak industrial AC/DC power supply with CC/CV reference design

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