

TCAN1043-Q1 Functional Safety FIT Rate, FMD and Pin FMA



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1 Overview

This document contains information for TCAN1043-Q1 (as well as the TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1), a controller area network (CAN) transceiver, to aid in a functional safety system design. The TCAN1043-Q1 comes in the SOIC (D) and VSON (DMT) packages. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

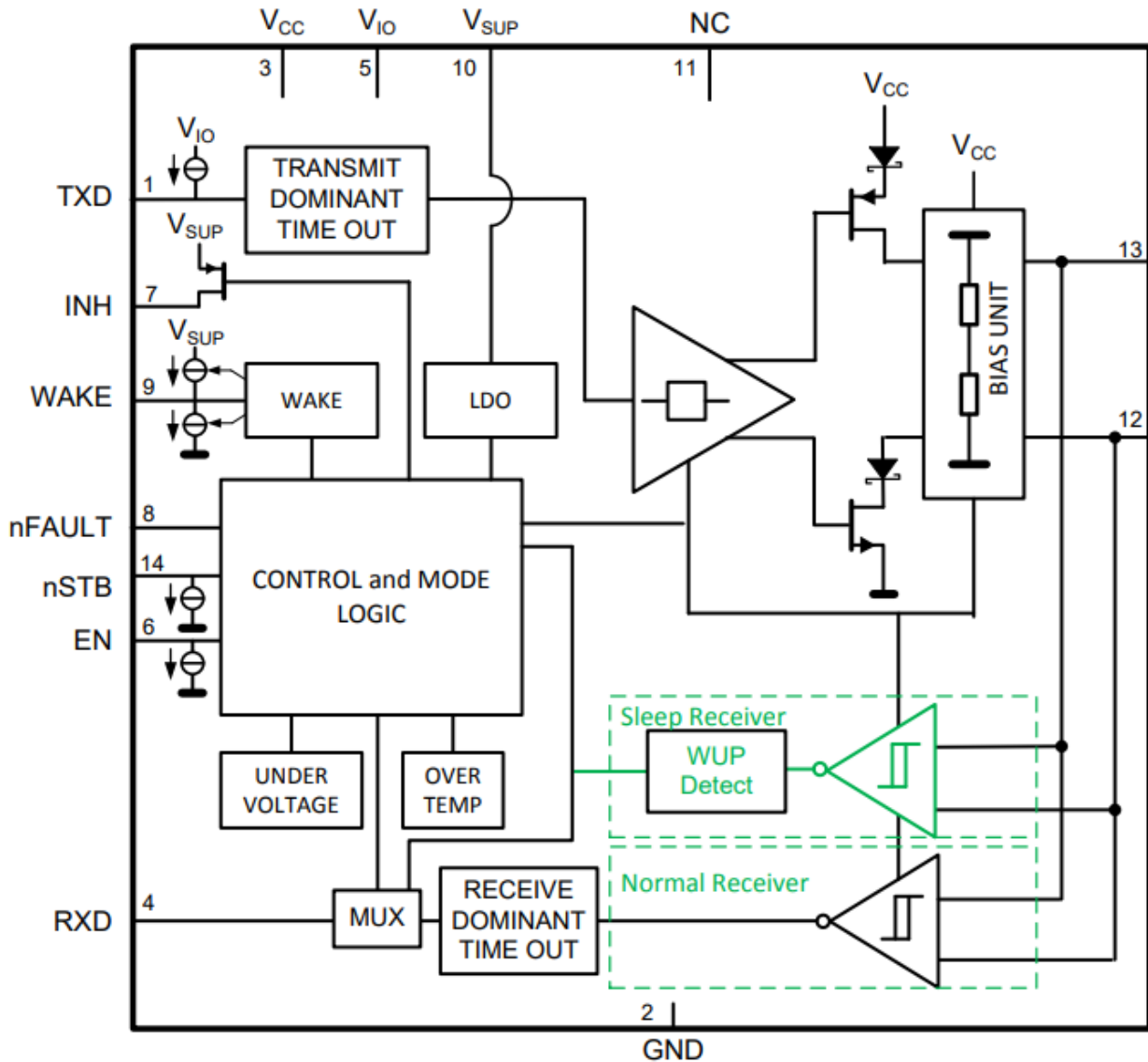


Figure 1-1. Functional Block Diagram

TCAN1043-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCAN1043-Q1 (as well as TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1) based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours) 14-pin SOIC (D)	FIT (Failures Per 10 ⁹ Hours) 14-pin VSON (DMT)
Total Component FIT Rate	21	9
Die FIT Rate	3	3
Package FIT Rate	18	6

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 126 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN1043-Q1 (as well as TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1) in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Receiver fail	35%
Transmitter fail	35%
System stuck in sleep mode	15%
CANL or CANH driver biased dominant indefinitely	5%
Short-circuit of any two pins	5%
Reports erroneous fault condition	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCAN1043-Q1 (as well as the TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VSUP (see [Table 4-5](#))
- Pin short-circuited to VCC (see [Table 4-6](#))
- Pin short-circuited to VIO (see [Table 4-7](#))

[Table 4-2](#) through [Table 4-7](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the TCAN1043-Q1 SOIC pin diagram. [Figure 4-2](#) shows the TCAN1043-Q1 VSON pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN1043-Q1 data sheet.

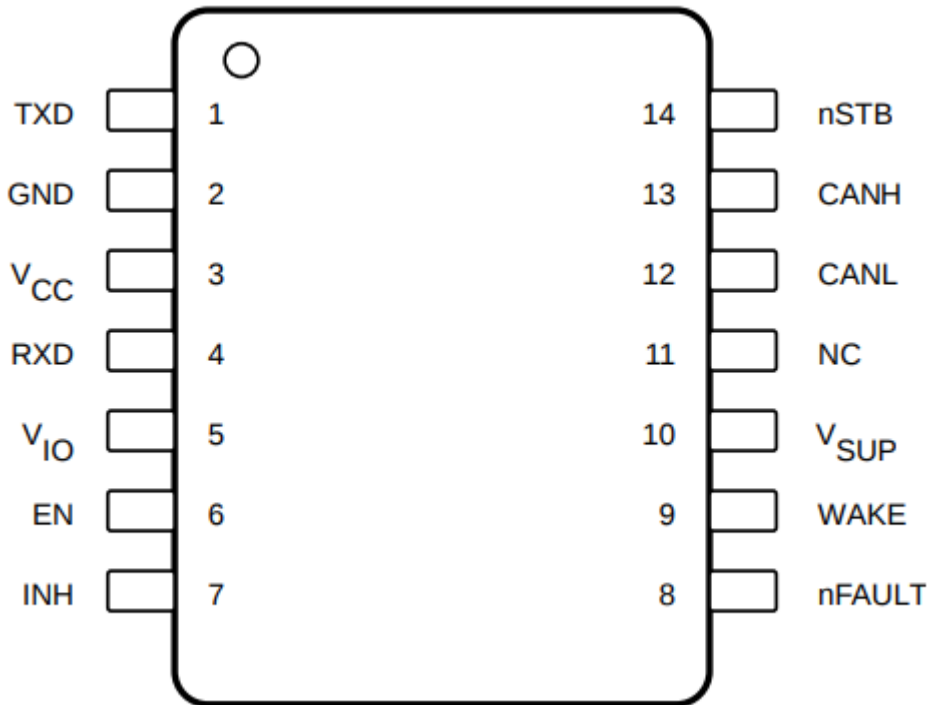
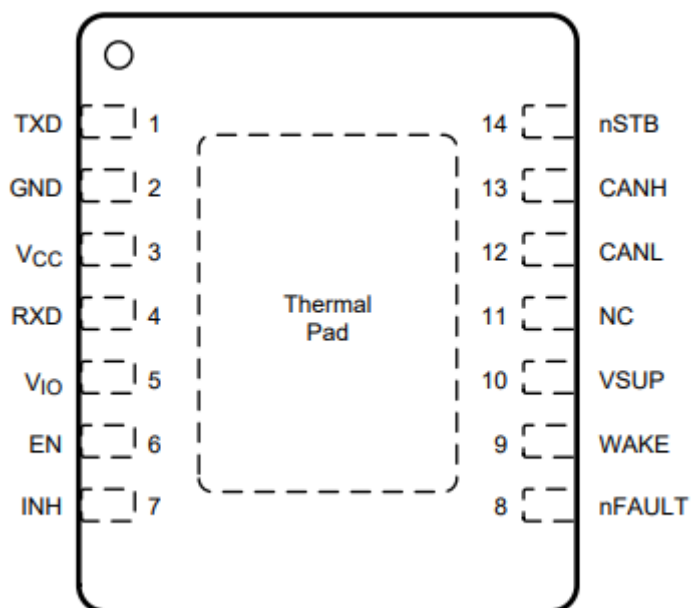


Figure 4-1. TCAN1043-Q1 SOIC Pin Diagram


Figure 4-2. TCAN1043-Q1 VSON Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- $V_{CC} = 4.5\text{ V to }5.5\text{ V}$
- $V_{SUP} = 4.5\text{ V to }45\text{ V}$ (4.5 to 60 V for the H-version)
- $V_{IO} = 2.8\text{ V to }5.5\text{ V}$

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD will be biased dominant indefinitely and device will enter dominant time out mode. Unable to transmit data.	B
GND	2	None	D
VCC	3	Device will be in protected mode, high current draw from external regulator supplying VCC.	B
RXD	4	Receiver output biased recessive indefinitely. Host unable to receive data from bus.	B
VIO	5	Device will be in protected mode. Transceiver passive on bus, and high current draw from external regulator supplying VIO.	B
EN	6	EN pin biased low, device will not be able to enter normal mode. Unable to communicate.	B
INH	7	High I_{SUP} current, INH pin may be damaged and indication from sleep mode transition not available.	A
nFAULT	8	nFAULT pin biased low indefinitely which indicates a fault indefinitely.	B
WAKE	9	WAKE pin biased low indefinitely, will not be able to utilize local wake-up function.	B
VSUP	10	Device unpowered, high I_{SUP} current.	B
NC	11	None	D
CANL	12	$V_{O(REC)}$ spec violated. Degraded EMC performance.	C
CANH	13	Device cannot drive dominant to the bus, no communication possible.	B
nSTB	14	nSTB biased low indefinitely, transceiver unable to enter normal mode. Unable to communicate.	B
Thermal Pad	-	None	D

Note

The VSON package includes a thermal pad.

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD pin defaults to a recessive bias, device is always recessive and unable to transmit data.	B
GND	2	Device unpowered.	B
VCC	3	Device in protected mode.	B
RXD	4	No RXD output, unable to receive data.	B
VIO	5	Device in protected mode.	B
EN	6	EN pin defaults to a logic-low bias, device will not be able to enter normal mode. Unable to communicate.	B
INH	7	None	D
nFAULT	8	No effect on performance, unable to monitor system faults.	B
WAKE	9	No effect on device performance, will not be able to utilize local wake-up function.	B
VSUP	10	Device unpowered.	B
NC	11	None	D
CANL	12	Device cannot drive dominant on bus, unable to communicate.	B
CANH	13	Device cannot drive dominant on bus, unable to communicate.	B
nSTB	14	nSTB defaults to a logic-low bias, device will not be able to enter normal mode. Unable to communicate.	B
Thermal Pad	-	None	D

Note

The VSON package includes a thermal pad.

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	GND	TXD will be biased dominant indefinitely and device will enter dominant time out mode. Unable to transmit data.	B
GND	2	VCC	Device will be in protected mode, high I_{CC} current.	B
VCC	3	RXD	RXD output biased recessive indefinitely, controller unable to receive data from CAN bus.	B
RXD	4	VIO	RXD output biased recessive indefinitely, controller unable to receive data from CAN bus.	B
VIO	5	EN	EN pin biased high indefinitely, device will be unable to enter standby and silent mode.	B
EN	6	INH	Absolute maximum violation on EN pin except in sleep mode. Transceiver may be damaged.	A
nFAULT	8	WAKE	Potential absolute maximum violation on nFAULT pin if WAKE is biased high. Transceiver may be damaged.	A
WAKE	9	VSUP	WAKE biased high indefinitely, unable to utilize local wake-up function.	B
VSUP	10	NC	None	D
NC	11	CANL	None	D
CANL	12	CANH	Bus biased recessive, no communication possible. I_{OS} current may be reached on CANH/CANL.	B
CANH	13	nSTB	Driver and receiver turn off when the CAN bus is recessive. May not enter normal mode.	B

Note

The VSON package includes a thermal pad. All devices pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad.

Table 4-5. Pin FMA for Device Pins Short-Circuited to VSUP

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Absolute maximum violation, transceiver may be damaged.	A
GND	2	Device unpowered, high I _{SUP} current.	B
VCC	3	Absolute maximum violation, transceiver may be damaged.	A
RXD	4	Absolute maximum violation, transceiver may be damaged.	A
VIO	5	Absolute maximum violation, transceiver may be damaged.	A
EN	6	Absolute maximum violation, transceiver may be damaged.	A
INH	7	Minimal current driven into the INH pin.	D
nFAULT	8	Absolute maximum violation, transceiver may be damaged.	A
WAKE	9	WAKE biased high, unable to utilize local wake-up function.	B
VSUP	10	None	D
NC	11	None	D
CANL	12	I _{OS} current may be reached. RXD always recessive.	B
CANH	13	V _{O(REC)} spec violated, degraded EMC performance and communication errors may result as well.	C
nSTB	14	Absolute maximum violation, transceiver may be damaged.	A

Note

The VSON package includes a thermal pad.

Table 4-6. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive indefinitely, unable to transmit data.	B
GND	2	Device unpowered, high current draw from external regulator supplying VCC.	B
VCC	3	None	D
RXD	4	Receiver output biased recessive indefinitely. Host unable to receive data from bus.	B
VIO	5	IO pins will operate as 5V input/outputs. Microcontroller may be damaged if VCC > VIO.	C
EN	6	EN biased high indefinitely, device will be unable to enter standby and silent mode.	B
INH	7	Absolute maximum violation on VCC pin, INH will be biased at VCC voltage, system may not wake up.	B
nFAULT	8	nFAULT biased high indefinitely, transceiver unable to report faults.	B
WAKE	9	None	D
VSUP	10	Absolute maximum violation on VCC.	B
NC	11	None	D
CANL	12	I _{OS} current may be reached, RXD always recessive.	B
CANH	13	V _{O(REC)} spec violated, degraded EMC performance.	C
nSTB	14	nSTB biased high indefinitely, transceiver unable to enter standby and sleep mode.	B

Note

The VSON package includes a thermal pad.

Table 4-7. Pin FMA for Device Pins Short-Circuited to VIO

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive indefinitely, unable to transmit data.	B
GND	2	Device unpowered, high current draw from external regulator supplying VIO.	B
VCC	3	IO pins will operate as 5V input/outputs. Microcontroller may be damaged if VCC > VIO.	C
RXD	4	Receiver output biased recessive indefinitely. Host unable to receive data from bus.	B
VIO	5	None	D
EN	6	EN biased high indefinitely, device will be unable to enter standby and silent mode.	B
INH	7	Absolute maximum violation on VIO pin, INH will be biased at VIO voltage, system may not wake up.	B
nFAULT	8	nFAULT biased high indefinitely, transceiver unable to report faults.	B
WAKE	9	None	D
VSUP	10	Absolute maximum violation on VIO.	B
NC	11	None	D
CANL	12	I _{OS} current may be reached, RXD always recessive.	B
CANH	13	V _{O(REC)} spec violated, degraded EMC performance.	C
nSTB	14	nSTB biased high indefinitely, transceiver unable to enter standby and sleep mode.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (March 2021)	Page
• Added TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1 to list of applicable devices.....	2
• Added references to TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1.....	3
• Added references for TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1.....	4
• Added references for TCAN1043G-Q1, TCAN1043H-Q1, and TCAN1043HG-Q1.....	5

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