Application Report
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TUSB1002A Schematic Checklist

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ABSTRACT

This application report is for the TUSB1002A, the industry's first dual-channel USB 3.1 Gen 2SuperSpeedPlus (SSP) redriver and signal conditioner. TUSB1002A is a linear redriver supporting up to 16 dB of loss due to Inter-Symbol Interference (ISI). This schematic checklist provides a brief explanation of each device pin and the recommended configuration of the device pin for default operation. Use this information to check the connectivity for each TUSB1002A on a system schematic.

This document aids the design at the system level for general applications. This document should not be the only resource used. In addition to this list, customers are advised to use the information in the TUSB1002A datasheet, TUSB1002A EVM User's Guide and associated documents to gain a full understanding of device functionality. ii. Project collateral discussed in this application report can be downloaded from the following URL: www.ti.com/lit/zip/SLLA398.

NOTE: TUSB1002A has a thermal pad that must be connected to GND

Trademarks

1 TUSB1002A Schematic Checklist

Table 1. Schematic Checklist

Pin Name	Pin Number(s)	Pin Description	Recommendation
Power Pins			
VCC	1,13	3.3-V (± 10%) Supply	One 4.7 µF and one 0.1 µF capacitor on each VCC pin to GND
GND	6,10,18,21	Ground	GND must be connected to GROUND. (RGE package: Pins 6, 10, 18 and 21) (RMQ package: Pins 9 and 21)
Configuration Pins			
EN	5	Device Enable.	EN can be left unconnected or tied to a 100nF capacitor to GND.
MODE	7	Selects Device Operation.	Sampled after rising edge of EN (See Figure 2 in datasheet). Leave unconnected for normal USB3.1 dual channel operation. (RGE package: Pin 7 and RMQ package: Pin 6)
CFG1	4	CFG1 and CFG2 select VOD linearity range and DC gain for both channels 1 and 2.	Sampled after rising edge of EN (See Figure 2 in datasheet). Leave CFG1 and CFG2 pins unconnected for 0 dB of DC gain and 1200 mVpp VOD Linear Range. (See Table 3 in datasheet)
CFG2	15		
CH1_EQ1	2	CH1_EQ1 and CH1_EQ2 select up to 16 EQ setting used to control Rx EQ level for RX1P/N.	Sampled after rising edge of EN (See Figure 2 in datasheet). Leave CH1_EQ1 and CH1_EQ2 pins unconnected for 8.4 dB EQ Gain at 2.5 GHz and 13.1 dB EQ Gain at 5 GHz. (See Table 2 in datasheet)
CH1_EQ2	3		
CH2_EQ1	16	CH2_EQ1 and CH2_EQ2 select up to 16 EQ setting used to control Rx EQ level for RX1P/N.	Sampled after rising edge of EN (See Figure 2 in datasheet). Leave CH1_EQ1 and CH1_EQ2 pins unconnected for 8.4 dB EQ Gain at 2.5 GHz and 13.1 dB EQ Gain at 5 GHz. (See Table 2 in datasheet)
CH2_EQ2	17		
DCBOOST#	14	Adds additional DC gain that is selected by CFG1 and CFG2.	Add a pull-up resistor of 400 kΩ to add +1 dB of DC gain, as specified in Table 3 of datasheet. Sampled after rising edge of EN (See Figure 2 in datasheet). Leave pin unconnected for no additonal DC boost needed.

Table 1. Schematic Checklist (continued)

Pin Name	Pin Number(s)	Pin Description	Recommendation
USB Data Lines			
RX1P	9	Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1	0.1 µF AC coupling capacitors on the RX1P/N and RX2P/N terminals ONLY if the TUSB1002A is connected directly to an Application Processor (AP). Otherwise (connector) place >330 nF AC capacitors on the RX differential pairs. (The recommended values are 330nF, 390nF, or 470nF +/-10%.) When connected to an AP, the RX differential pairs must be connected to the TX pairs from the application (AP). When when connected to a USB receptacle, the RX lines must be connected to the connector's RX pins. The polarity can be swapped since it is allowed by the USB specification.
RX1N	8		
RX2P	19	Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2	
RX2N	20		
TX1P	22	Differential onput for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1	Requires 0.1 µF AC coupling capacitors. When connected to an application (AP), the TX1P/N and TX2P/N terminals must be connected to the RX pairs from the AP. When connected to a USB receptacle, the TX1P/N and TX2P/N terminals must be connected to the connector's TX1P/N and TX2P/N terminals. The polarity can be swapped since it is allowed by the USB specification.
TX1N	23		
TX2P	12	Differential onput for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2	
TX2N	11		
Misc. Pins			
RSVD1	24	Reserved.	Under normal operation, this pin is driven low by TUSB1002A. Leave floating.

2 References

- TUSB1002A USB3.2 10Gbps Dual-channel Linear Redriver Datasheet
- TUSB1002A Evaluation Module

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