SN65DSI8x Video Configuration Guide and Configuration Tool Software Users Manual

Computer and Consumer Interface

ABSTRACT

This document contains information for configuring the SN65DSI83, SN65DSI84, and SN65DSI85 devices correctly for video system implementation. The document provides an overview of the SN65DSI8x video operation and information on the DSI Tuner video configuration tool used to obtain the requirements for video timing and the device configuration register values.

This document is not intended as a replacement for the datasheet.

Contents

Figures

Tables

1 Overview

SN65DSI83, SN65DSI84 and SN65DSI85; hereafter in this document referred to as SN65DSI8x, are MIPI DSI-to-LVDS bridge devices that support video modes in forward direction. These devices are primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSI8x can be used between a GPU with DSI output and a video panel with LVDS inputs.

Table 1 contains a summary of the feature sets on these devices.

Table 1. SN65DSI83, SN65DSI84, and SN65DSI85 Features Summary

Part Name	Description	Max Resolution
SN65DSI83	Single-Channel DSI to Single-Link LVDS	Suitable 1366 × 768 60 fps at 24 bpp/18 bpp, Max resolution up to 1920 × 1200 60 fps at 24 bpp with reduced blanking
SN65DSI84	Single-Channel DSI to two Single-Link LVDS	1920 × 1200 60 fps at 24 bpp/18 bpp
SN65DSI85	Dual-Channel DSI to two Single-Link LVDS	2560 × 1600 60 fps, 1920 × 1080p 120 fps at 24 bpp /18 bpp

1.1 Video Operation Overview

There are six major video mode configurations supported by the SN65DSI8x device family. The mode of operation is determined by the number of DSI and LVDS Channels in use and the DSI data input options configured in the CSR registers and the version of the device in use. Table 2 depicts the video modes supported by the SN65DSI83, SN65DSI84, and SN65DSI85. An 'X' indicates the supported mode for the device.

Table 2. SN65DSI83, SN65DSI84 and SN65DSI85 Video Configuration Comparison

Video Configurations	DSI Input Option – Left/Right(LR), Odd/Even(OE)	Number of DSI Input Channels	Number of DSI Output Channels	SN65DSI83	SN65DSI84	SN65DSI85
1 Ch DSI to 1 Ch LVDS	N/A	1	1	x	X	x
1 Ch DSI to 2 Ch LVDS	N/A	1	2	N/A	X	x
2 Ch LR DSI to 1 Ch LVDS	LR	2	1	N/A	N/A	x
2 Ch OE DSI to 1 Ch LVDS	OE	2	1	N/A	N/A	x
2 Ch LR DSI to 2 Ch LVDS	LR	2	2	N/A	N/A	x
2 Ch OE DSI to 2 Ch LVDS	OE	2	2	N/A	N/A	x

Each DSI Channel consists of 4 differential pairs of DSI data lanes and 1 differential pair of DSI CLK lanes. Each LVDS Channel consists of 4 LVDS data lanes and 1 LVDS CLK lane. When 2 DSI Channels are selected for use, the maximum number of data lanes is eight; the maximum number of clock lanes is two, yielding up to 8 Gbps of data throughput. The max resolution in Table 1 is calculated based on the maximum throughput supported by the corresponding device.

The video transfer is done on a line-by-line basis in the SN65DSI8x device. The rule of thumb for the DSI data transfer using the SN65DSI8x devices is to match the line time (Sync-to-Sync time) between the input and the output. It is also important to maintain the data rate so as not to underflow or overflow the internal buffer. The SN65DSI85 supports a programmable delay value to help maintain the data rate and the availability of data in internal buffers. The delay value, also referred as "sync delay", is used to delay the outgoing data, up to 0xFF number of pixels, by programming the corresponding register field. The sync delay value can be calculated based on the DSI input parameters and the LVDS output requirements. It is important to program the sync delay value to a properly calculated value for correct operation of the device.

The LVDS output timing is generated based on the CSR values programmed in the corresponding video parameter fields. The following values need to be programmed to create the timing for the LVDS panel; HSync pulse width, HSync Back Porch duration, and VSync pulse width.

The Left/Right (LR) or Odd/Even (OE) configuration is valid only in the dual-mode configuration where the device is configured to use 2 DSI Channels. The LR and OE configurations apply only to the DSI Input ports. When the LR mode is selected, the left portion of the frame should be presented on DSI Channel A, the right port on DSI Channel B. The number of pixels presented on each side is configurable in the corresponding CSR.

When the OE mode is selected, the odd number pixels should be presented on DSI Channel A, the even number pixels on DSI Channel B. The number of pixels presented on each side is configurable but should be half the total number of pixels per line.

1.2 How the Video Config Tool (DSI Tuner) Helps

The DSI Tuner video configuration tool generates the video timing and the configuration register values required to transfer the DSI data to the LVDS panel using the SN65DSI8x DSI-to-LVDS bridge device. The timing and the register values are calculated based on inputs entered in the input fields provided in the tool.

Note that the tool does not set the values that need to be set or cleared in a recommended sequence. For example, the PLL_EN bit (CSR 0x0D.0) and SOFT_RESET bit (CSR 0x09.0) are not set in the CSR tool as these bits need to be set in the recommended sequence.

The values generated can be programmed in the corresponding initialization sequence step where the CSR registers are set. – Init seq4 “Initialize all CSR registers to their appropriate values…”

2 Video Configuration Tool Users Guide

The Video configuration tool generates the video timing requirement and CSR values based upon the inputs entered for the panel and the DSI inputs

2.1 Device Selection

When the software is invoked, the Device Selection pop-up window appears. Select the device to be configured using the drop-down box as shown below.

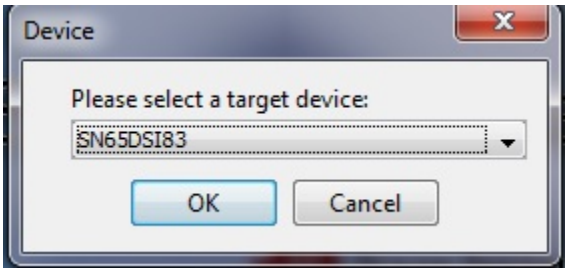

Figure 1. Device Selection Window

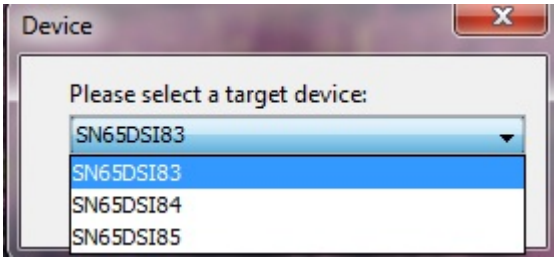

Figure 2. Device Selection Window with Drop-Down Box

2.2 Panel Inputs

The Panel Inputs window prompts to enter the LVDS panel parameters. All the required fields in the Panel Inputs window must be entered first.

Refer to the LVDS panel specification for the parameters. The parameters not applicable to the chosen mode of operation are automatically grayed out. Enter the values only into the white blank fields.

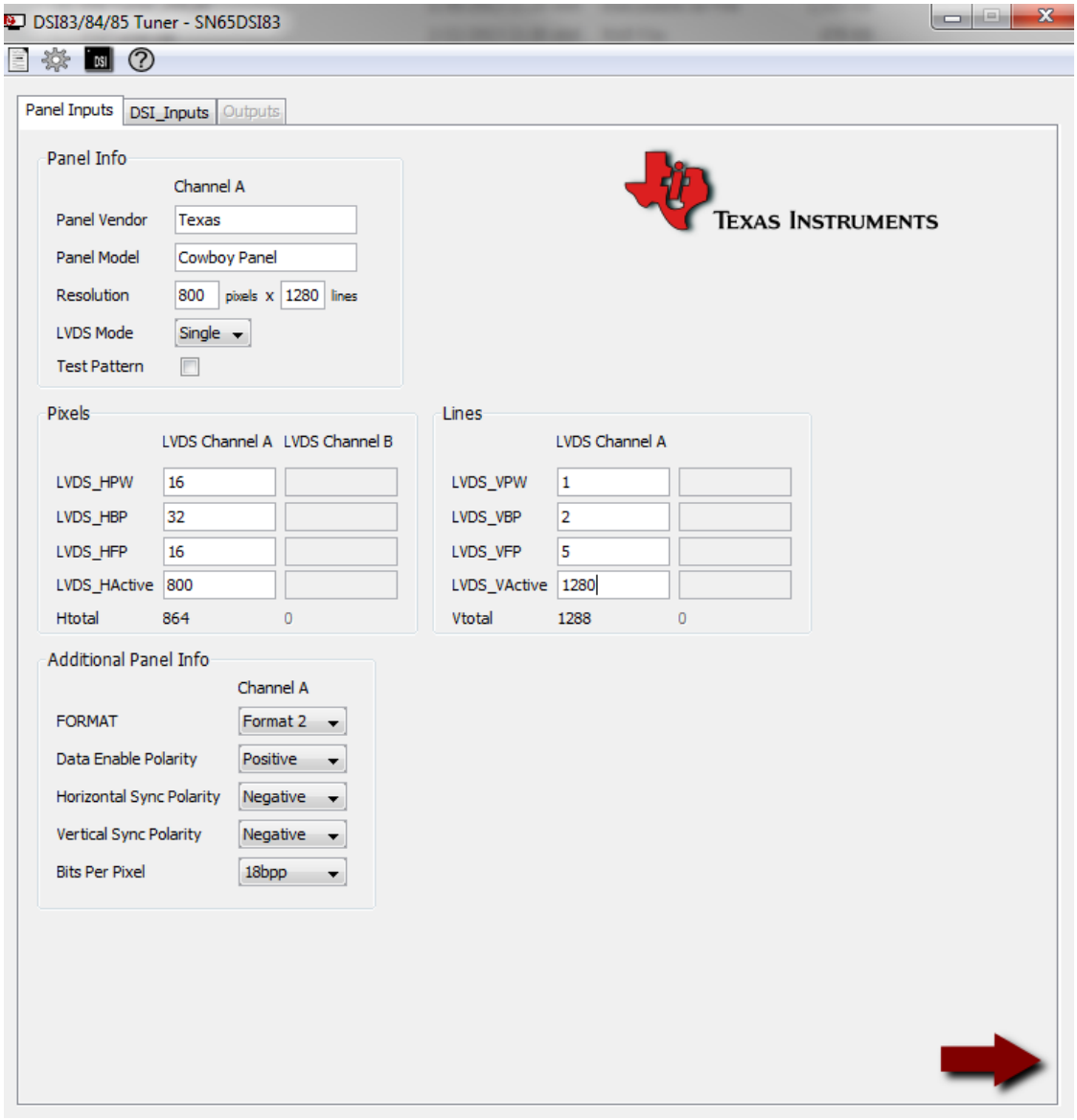

Figure 3. Panel Inputs Window

2.2.1 Panel Info

1. Enter Panel Vendor and the Panel Model number.
2. Enter Resolution field: Number of horizontal pixels × Number of vertical lines. When the resolution is entered, the LVDS_HActive and LVDS_VActive fields are updated automatically.
3. Select LVDS Mode: Single or Dual.
   For SN65DSI83 only, the “Single” LVDS Mode is valid.
4. The Test Pattern only needs to be checked to enable the Test Pattern Generation feature for debugging purposes. Leave the check box blank for normal operation mode.

2.2.2 Pixels and Lines

Enter all LVDS parameters for the chosen panel. The information for the number of pixels or lines should be available in the panel specification.

LVDS_HPW: LVDS Horizontal Pulse Width

LVDS_HBP: LVDS Back Porch

LVDS_HFP: LVDS Front Porch

LVDS_HActive: LVDS Horizontal Active pixels. This field should have already filled in, based on the Resolution field entry.

HTotal: Total Number of Horizontal pixels per line based upon parameters entered above.

LVDS_VPW: LVDS Vertical Pulse Width

LVDS_VBP: LVDS Vertical Back Porch

LVDS_VFP: LVDS Vertical Front Porch

LVDS_VActive: LVDS Vertical Active lines. This field should have already filled in, based on the Resolution field entry.

VTotal: Total Number of Vertical lines per frame, based upon parameters entered above.

2.2.3 Additional Panel Info

In this section of the Panel Inputs, information for the LVDS panel output such as the format, polarities and bpp is entered.

FORMAT: Select between Format 1 and Format 2. Refer to the individual SN65DSI8x datasheets (SN65DSI83, SN65DSI84, SN65DSI85) for Format 1 or Format 2 definition.

Format 2 must be selected, if RGB666 data is selected for DSI Video Mode.

Format 1 must be selected, if RGB888 24 bpp data is received from DSI while 18 bpp panel is selected and CH*_24BPP_MODE is 0 (default value).

Data Enable Polarity, Horizontal Sync Polarity, Vertical Sync Polarity: Select between Positive and Negative, based on panel requirements

Bits per Pixel: Select between 18 bpp and 24 bpp

Once all information has been filled in the Panel Inputs window, click  .

2.3 DSI Inputs

Once all information has been entered under Panel Inputs, the software prompts for the DSI inputs. All DSI-related input information is entered in this window. The parameters entered must match the actual DSI parameters transmitted by the DSI source to the SN65DSI85 DSI receiver.

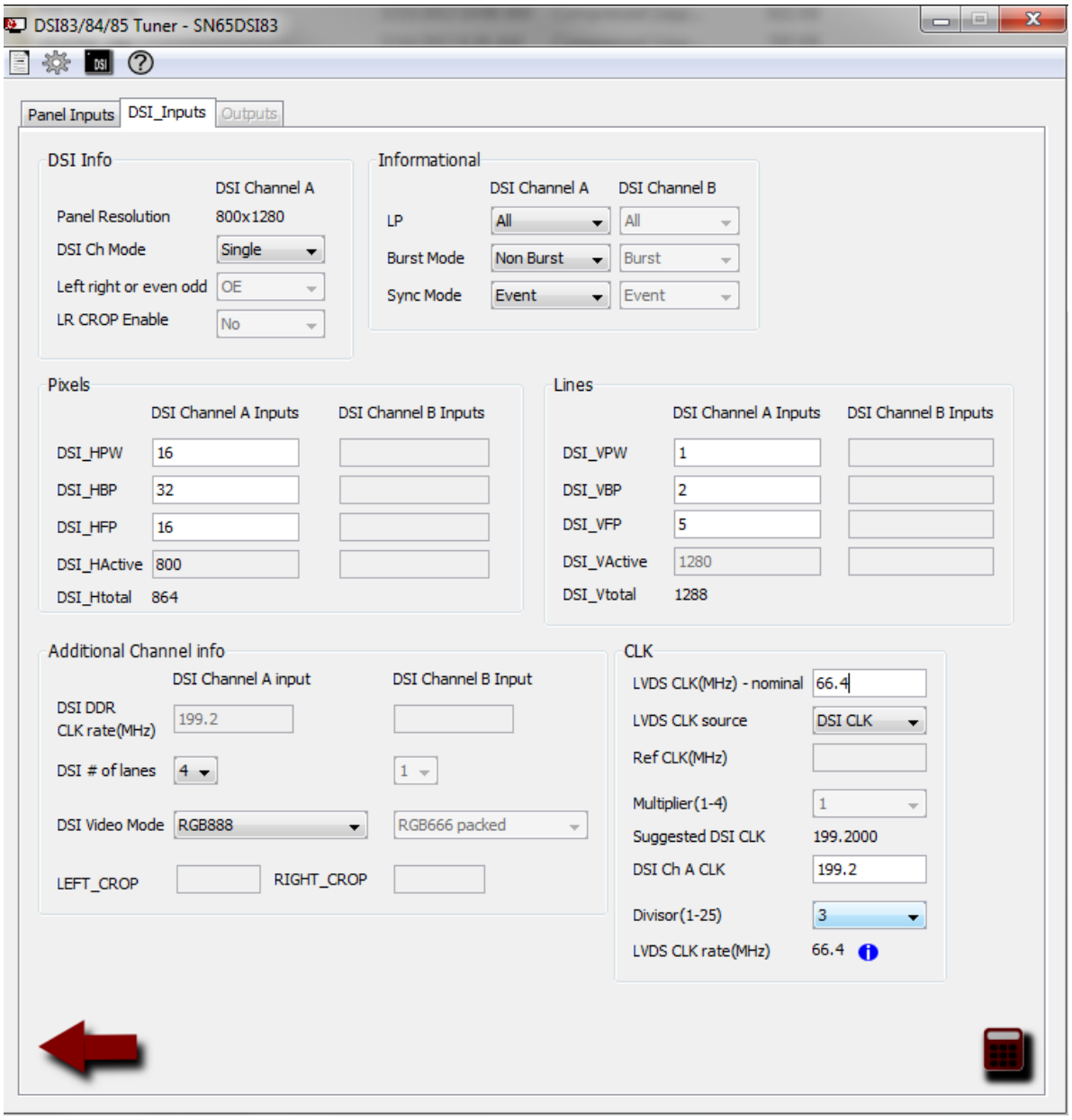

Figure 4. DSI Inputs Window

2.3.1 DSI Info

1. The Panel resolution appears based upon the LVDS panel resolution entered in the Panel Inputs window.
2. Select DSI Ch Mode: Single, Dual or Two Single.
   If Dual, go to step 3. If Single or Two Single, go to 2.3.2 Pixels.
   For SN65DSI83 and SN65DSI84, only Single mode is valid.

Steps 3 and 4 below are not applicable, if SN65DSI83 or SN65DSI84 are selected.

3. Select Left right(LR) or even odd(OE): Note this field is grayed out if DSI Ch Mode is not Dual. If LR, go to step 4, otherwise go to step 2.3.2 Pixels.
4. Select LR CROP Enable: Yes or No. For typical applications, LR CROP needs to be disabled (select No).

2.3.2 Pixels

Enter all horizontal pixels DSI input parameters into the white blank boxes.

DSI_HPW: DSI Horizontal Pulse Width

DSI_HBP: DSI Horizontal Back Porch

DSI_HFP: DSI Horizontal Front Porch

DSI_HActive: DSI Horizontal Active.
The DSI_HActive field defaults to the value updated, based upon the panel parameters entered in the Panel Inputs.

2.3.3 Lines

Enter all vertical line DSI input parameters into white blank boxes.

DSI_VPW: DSI Vertical Pulse Width

DSI_VBP: DSI Vertical Back Porch

DSI_VFP: DSI Vertical Front Porch

DSI_VActive: DSI Vertical Active.
The DSI_VActive field defaults to the value updated based upon the panel parameters entered in the Panel Inputs.

2.3.4 Additional Channel Info

1. The DSI DDR CLK rate (MHz) field for DSI Channel A Input defaults to the DSI Ch A CLK value entered in the CLK section of the Panel Inputs window. There is no need to enter DSI Channel B DDR CLK rate, unless the DSI Ch Mode = Two Single or Dual.
2. Select the number of lanes used for DSI TX for each channel: 1 to 4.
3. Select DSI Video Mode: RGB666 packed, RGB666 loosely packed or RGB888.
4. Enter LEFT_CROP and RIGHT_CROP value only if LR_CROP Enable = Yes in the DSI Info section.

2.3.5 CLK

In this section of the DSI Inputs Window, the CLK configuration is entered. The tool calculates the LVDS CLK rate (MHz) and suggested minimum DSI CLK rate, if non-burst mode is selected. The SN65DSI8x can be configured to use external reference CLK or DSI Channel A CLK as LVDS CLK source.

1. Enter the nominal LVDS CLK frequency of the panel in the *LVDS CLK (MHz)-nominal* field.

   The LVDS CLK rate (MHz) typically matches the nominal Pixel CLK (MHz) frequency in single LVDS channel configuration. The LVDS CLK is typically half the actual pixel CLK rate in dual LVDS Channel configuration. The LVDS CLK rate calculated should be close to the nominal LVDS CLK value of the panel. The nominal LVDS CLK(MHz) value is used to calculate the suggested DSI CLK rate if non-burst mode is selected. The actual DSI CLK rate required for the non-burst mode of operation varies depending on the actual LVDS CLK rate calculated, based upon the DSI Ch A CLK/Ref CLK(MHz) and Divisor/Multiplier inputs. The actual DSI CLK rate for the non-burst mode of operation is calculated in the Outputs window as MIN DSI CLK REQUIREMENT(MHz). The DSI CLK rate for the non-burst operation should be equal to the minimum DSI CLK frequency for the given data throughput and the line time.
2. Select the LVDS CLK source: DSI CLK or Ref CLK.
3. If Ref CLK is selected, enter the reference CLK frequency in the Ref CLK(MHz) field, then select the multiplier value(1-4) that satisfies the equation below:

Ref CLK (MHz) x Multiplier value = LVDS CLK rate (pixel CLK for the LVDS panel). If DSI CLK is selected, enter the DSI channel A CLK frequency in the DSI Ch a CLK field then select the Divisor value (1-25). The value entered in the DSI Ch A CLK field is automatically reflected in the DSI DDR CLK rate (MHz) field of the DSI Inputs window.

Once all information has been entered, CLICK the  icon.

2.4 Outputs

The Output window tab gets activated once all input parameters have been filled in both DSI and Panel Inputs window and the calculator icon is clicked. It outputs the following calculated values: Line Time (SYNC to SYNC) Requirement (us), MIN DSI Ch* CLK REQUIREMENT (MHz), Data Burst Time based on actual DSI Ch* CLK and data throughput in us.

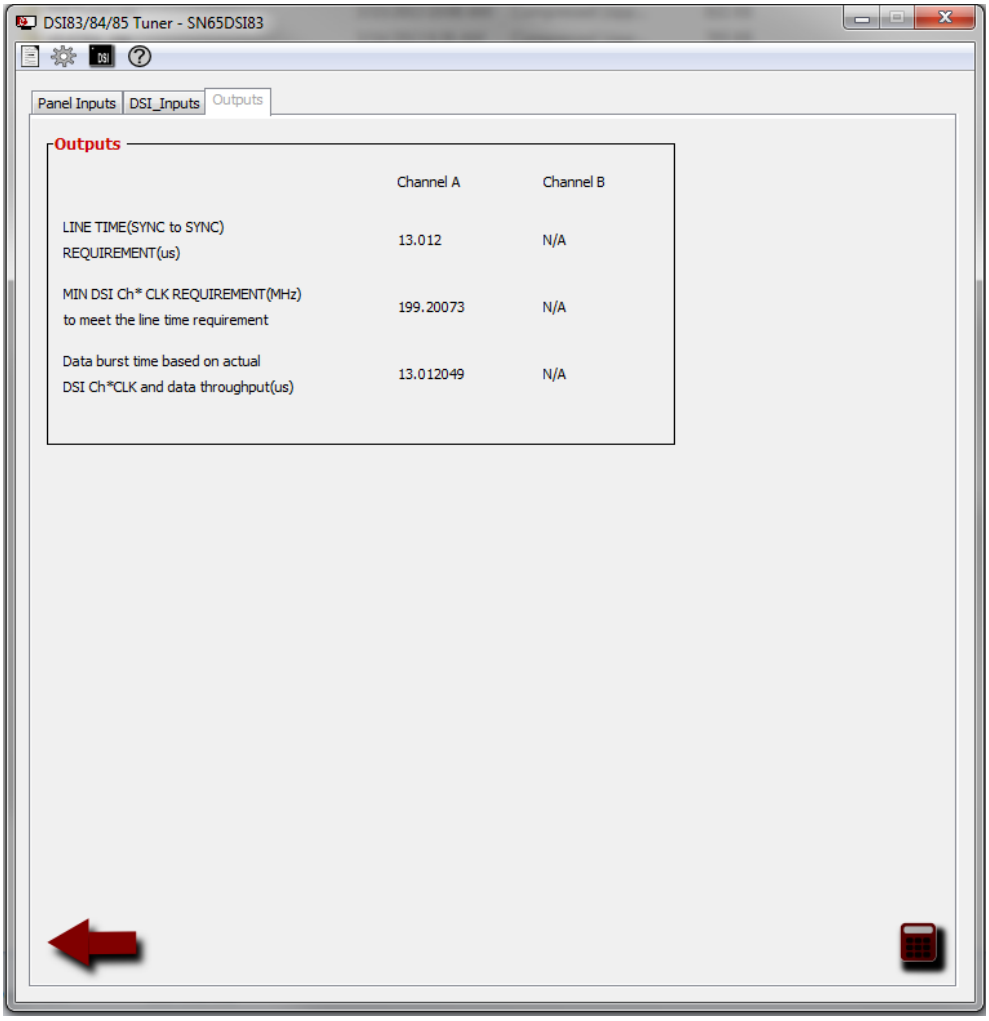

Figure 5. Output Window

2.4.1 Line Time (SYNC to SYNC) Requirement (us)

The line time (SYNC TO SYNC) requirement output value represents the HSYNC (or Vsync) to the next HSYNC line time requirement for both the panel and the DSI input side. This output value is calculated based upon the panel inputs. As mentioned in other sections of this document, it is critical to match the line time of the DSI input to the panel line time. The DSI source must ensure the line time meets the line time requirement calculated in this window.

2.4.2 MIN DSI Ch* CLK REQUIREMENT (MHz)

The MIN DSI Ch*CLK REQUIREMENT is the minimum calculated DSI CLK frequency required to sample in DSI data within a given line time (calculated above). This value is based upon the DSI throughput and the line time, calculated using the DSI input and panel input parameters. This value is equivalent to the DSI CLK rate that should be used in non-burst operation.

2.4.3 Data Burst Time

The Data burst rate is calculated based on the actual DSI DDR CLK rate and the DSI data throughput. If the burst time is smaller than the LINE TIME, the rest of the line time period must be filled in with blanking packets or by driving LP11 low power state. If the burst time is greater than the LINE TIME, the DSI DDR CLK rate needs to be increased to meet the line time. The data burst time is typically equal to the line time in non-burst mode of operation. It is less than the line time in burst mode operation.

Click the  icon for CSR generation.

2.5 Control and Status Registers (CSR)

Once the  icon is clicked, move the cursor to the main menu on the upper-left corner.

Click the  icon and then select **Generate CSR List** from the drop-down menu, Click **OK** when the pop-up message appears. The following CSR output window should now open.

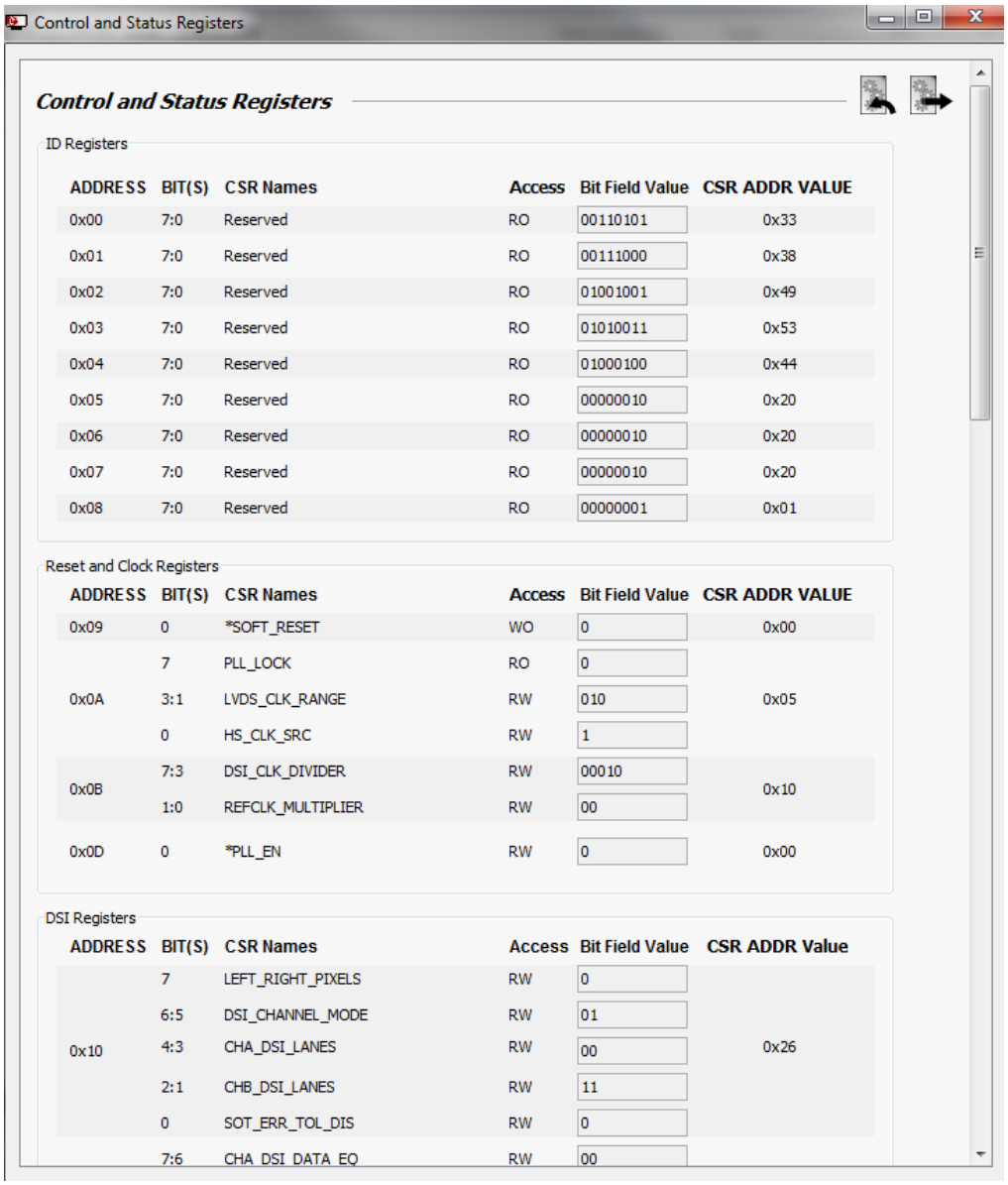

Figure 6. Control and Status Registers Window

Click the text output icon  at the upper-right corner of the Control and Status Registers window, if the CSR output is needed in text format. The text file generates the list of writeable CSRs as shown below:

```
//=====================================================================
// Filename   : CSR.txt
//
//   (C) Copyright 2013 by Texas Instruments Incorporated.
//   All rights reserved.
//
//=====================================================================
0x09              0x00
0x0A              0x05
0x0B              0x10
0x0D              0x00
0x10              0x26
0x11              0x00
0x12              0x00
0x13              0x00
0x18              0x70
0x19              0x00
0x1A              0x03
0x1B              0x00
0x20              0x20
0x21              0x03
0x22              0x00
0x23              0x00
0x24              0x00
0x25              0x00
0x26              0x00
0x27              0x00
0x28              0x21
0x29              0x00
0x2A              0x00
0x2B              0x00
0x2C              0x10
0x2D              0x00
0x2E              0x00
0x2F              0x00
0x30              0x01
0x31              0x00
0x32              0x00
0x33              0x00
0x34              0x20
0x35              0x00
0x36              0x00
0x37              0x00
0x38              0x00
0x39              0x00
0x3A              0x00
0x3B              0x00
0x3C              0x00
0x3D              0x00
0x3E              0x00
```

The PLL_EN bit and SOFT_RESET bit are not set as they need to be set per the recommended sequence defined in the datasheet

The text file can be imported to view the bit mapping in the Control and Status Registers window. Click  to import the text file. The CSR values are set and displayed in the Control and Status Registers window according to the values programmed in the imported text file.

2.6 Main Menu Options

2.6.1 File Option

2.6.1.1 Export/Import File

The DSI85 tool allows importing and exporting configuration files. The setup can be saved by selecting the *Export File* option. Save the file with a *dsi* extension: *.dsi. The *dsi* files can be imported back, then the tool automatically loads the configuration saved in the *dsi* file.

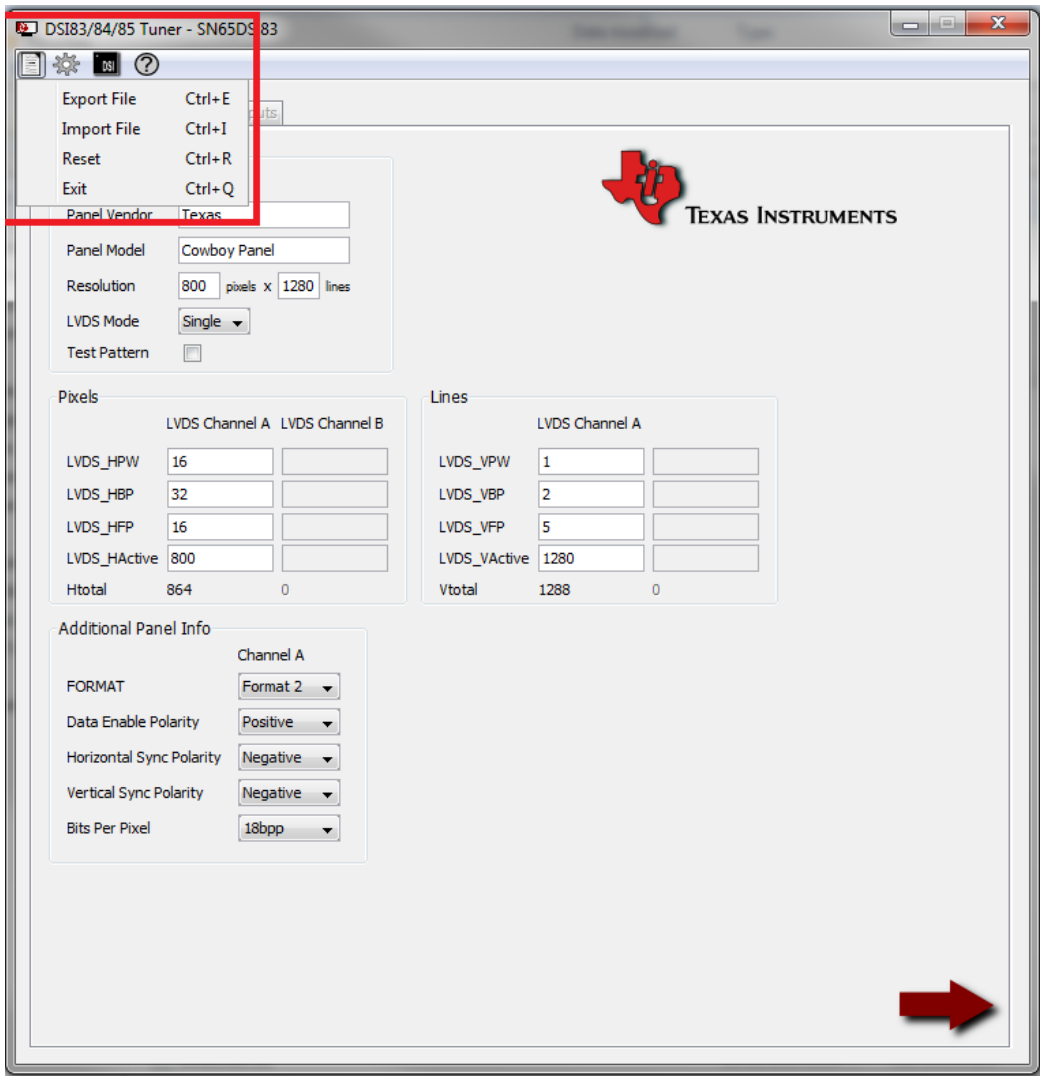

Figure 7. File Options

2.6.1.2 Reset

The Reset option resets the user-input fields to the initial state. When any configuration change is required, the Reset must be done by selecting *Reset* in the drop-down list, or Ctrl + R.

2.6.2 Control and Status Register Option

The *Control and Status Register* option generates the CSR values based upon the entry in the *Panel Inputs* and *DSI_Inputs*.

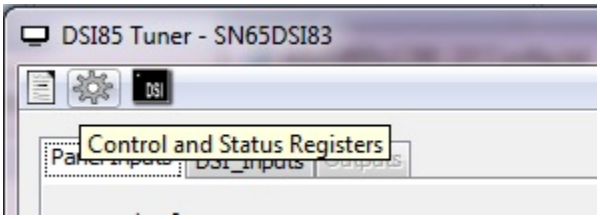

Figure 8. Control and Status Register Option

The *CSR* list window appears when the *Generate CSR List* is selected.

Should the CSR value need to be modified, enable *CSR Debug Mode* then select *Generate CSR List*. This allows modification of the CSR values in the CSR list window.

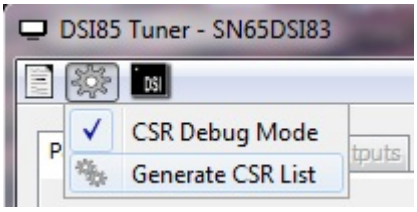

Figure 9. CSR Debug Mode and Generate CSR List Options

2.6.3 Device Selection Option

The device selection option is also available via the *Main Window* menu. The same drop-down list pop-up window appears when the icon is selected.

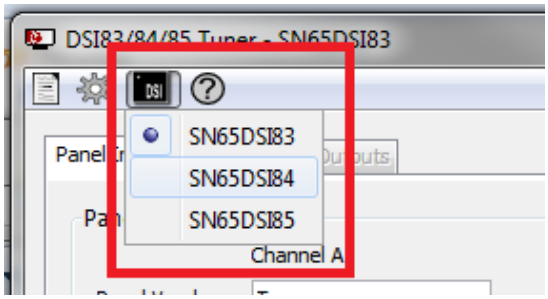

Figure 10. Device Selection Option

When the device is switched, make sure Reset is done by selecting *Reset* from the *File* drop-down menu, or Ctrl-R.

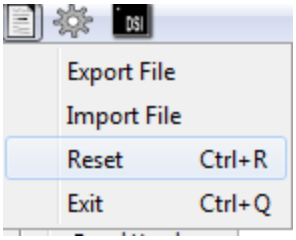

Figure 11. Reset Option

2.7 Example 1: 1024x600 Configuration

2.7.1 Panel Inputs

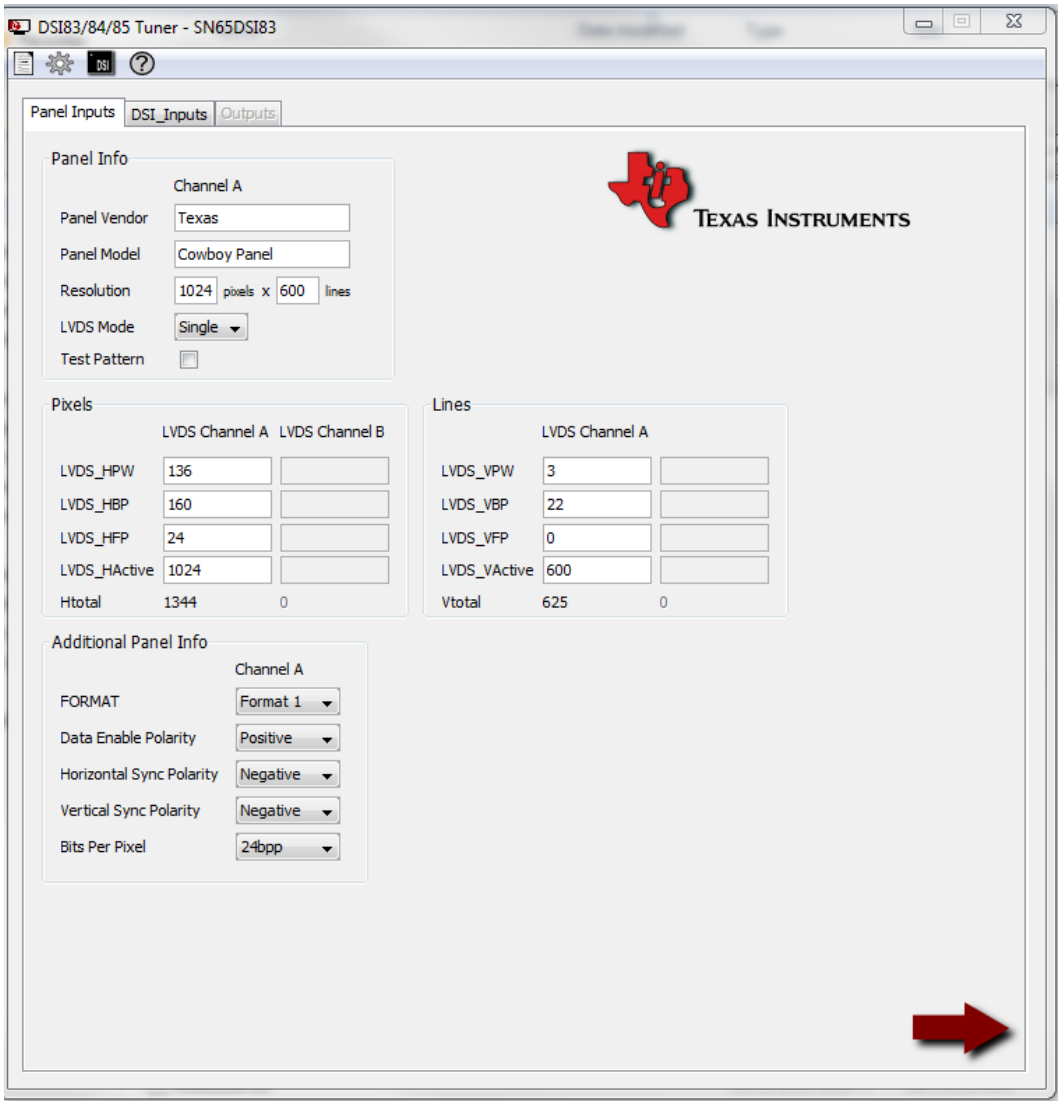

Figure 12. Panel Inputs for 1024x600 Resolution

2.7.3 DSI_Inputs

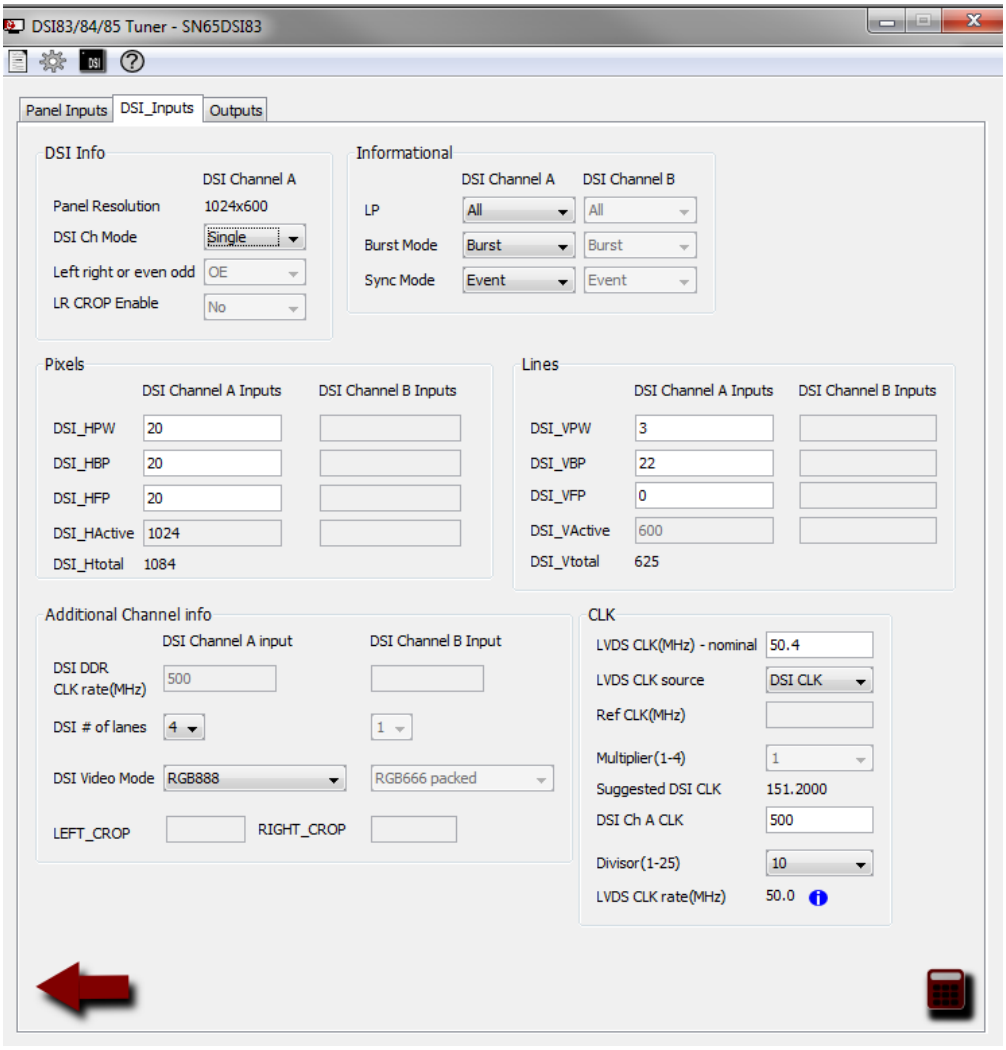

Figure 13. DSI Inputs for 1024x600 Resolution

2.7.4 Output

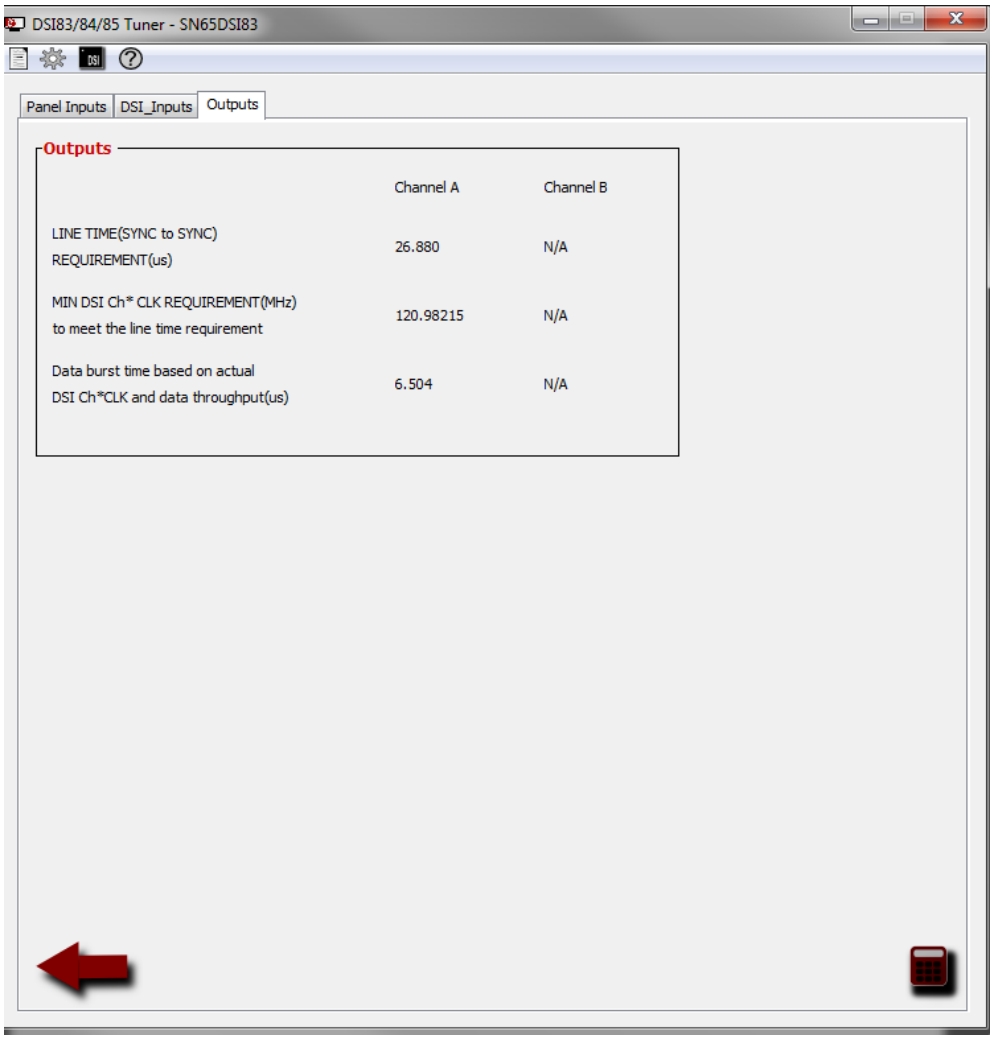

Figure 14. Outputs for 1024x600 Resolution

3 SN65DSI8x Video Operation General Rules

General rules for calculating video parameters for all video modes are:

1. Line time on DSI input and LVDS output MUST match while there is no need to match the horizontal sync or porch parameters.
2. There should always be data available in FIFO for LVDS output. For example, for the sync pulse transmit, the HSS should be available in the FIFO.
3. The LVDS output timing programmed in CSR MUST match the LVDS panel specification. There is no need to match horizontal or vertical video CSR configurations to the DSI input values except for the CH*_ACTIVE_LINE_LENGTH (=number of active pixels on DSI Input).
4. The number of active pixels presented on *DSI_Input* MUST match the programmed value in the CSR: CH*_ACTIVE_LINE_LENGTH_LOW/HIGH
5. In case of dual-DSI operation utilizing both DSI Channel A and B, it is recommended to minimize the delay between Ch A and Ch B below ~9 DSI CLK cycles. Timing skew of ~ line is allowed on Channel B in some cases, however, video parameters and DSI8X video configuration registers need to be programmed to accommodate the timing skew between two channels.

The following equations are used for DSI input rate in pixels and LVDS output rate in pixels:

DSI_pixel_rate = (DSICLK × 2 × # of lanes) / (18 or 24 bpp)

LVDS_pixel_rate = LVDS_OUT_CLK rate determined based on DSI CLK source or REF CLK with divisor or multiplier. Divisor or multiplier value is determined based on the programmed value in the corresponding CSRs.

ADDR	Description	7	6	5	4	3	2	1	0
0xB	DSI_CLK_DIVIDER REFCLK_MULTIPLIER	DSI_CLK_DIV	DSI_CLK_DIV	DSI_CLK_DIV	DSI_CLK_DIV	DSI_CLK_DIV		REFCLK_MULT	REFCLK_MULT

4 Notes on LVDS Panel Resolution and DSI Throughput

This section describes how the DSI throughput can be derived based upon the LVDS panel resolution or pixel CLK frequency.

Total Throughput(bits/sec) =
(Number of pixels per horizontal line) × (Number of lines per frame) × (# of frames/sec) × (Number of bits per pixel) =
(Total # of pixels/sec) × (Number of bits/pixel)

For LVDS panel resolution 1280 × 800 24bpp at 60 Hz:

Total Throughput for active video region = (1280 pixels) × (800 lines) × (60 frames/sec) × (24 bits/pixel) ~= 1.475 Gbps

This throughput number does not consider blanking period.

Table 3. VESA Display Monitor Timing Standard

Resolution	Refresh Rate (frames/sec)	Pixel Frequency (pixels/sec)	Reduced Blanking?
1280 × 800	60 Hz	71 MHz	Yes
1280 × 800	60 Hz	83.5 MHz	No

The total throughput including blanking with reduced blanking for 24bpp at 60Hz based upon the values given above,

(71 Mpixels/sec) × (24 bits/pixel) = 1.704 Gbps

The total throughput including blanking without reduced blanking for 24bpp at 60Hz based upon the values given above,

(83.5 Mpixels/sec) × (24 bits/pixel) = 2.004 Gbps

The SN65DSI8x supports 1 Gbps/sec throughput for each data lane.

Therefore, for the panel resolution of 1280 × 800 24 bpp at 60 Hz with reduced blanking, two or more number of lanes must be used to support the band width, three or more number of lanes without reduced blanking.

5 SN65DSI8x FAQ and Trouble Shooting Guide

In case of no video output, check the following items:

1. Does the actual number of active DSI data lanes match the SN65DSI8x register configuration?
2. Signal integrity on DSI CLK and HS data lanes
3. Does the LP to HS and HS to LP timing meet the requirements specified in the MIPI DPHY spec?
4. Is DSI_CLK range register programmed to match the actual DSI CLK rate?
5. Does the line time on the DSI input match the output line time requirement?
6. Is the recommended initialization sequence followed as described in the device datasheet?

There are error reporting registers that the system software can read to help with system debug. The error status registers are at offset 0xE5 and/or E6. Individual error conditions at address 0xE5 and/or 0xE6 can be reported via IRQ pulses by enabling the corresponding error status bits at offset 0xE1 and/or 0xE2. Refer to the datasheet for details in the IRQ operation and the error reporting mechanism.

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