

TUSB9261 Implementation Guide

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ABSTRACT

This document is provided to assist platform designers in implementing the TUSB9261 USB 3.0 to Serial ATA Bridge Controller. Detailed information can be found in the TUSB9261 Data Manual ([SLLSE67](#)). This document provides board design recommendations for the various device features when designing in the TUSB9261.

This document is intended for developers familiar with high-speed PCB design and layout. Knowledge of the USB 3.0 and SATA specifications and protocol is required as well. The following layout recommendations should not be considered the sole method of implementation, but rather as a guide. The preferences of the individual developer, requirements of the design, number of components in the circuit, as well as many other factors will influence each individual layout.

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1 TUSB9261 Typical System Implementation

Figure 1 represents a typical implementation of the TUSB9261 USB 3.0 to Serial ATA Bridge. The device serves as a bridge between a downstream USB 3.0 host port and a SATA device such as a hard disk drive. A crystal or oscillator supplies the required clock source. A SPI Flash device contains the firmware that is loaded into the TUSB9261 after the de-assertion of RESET. Push buttons or any other desired logic can be connected to the TUSB9261 GPIO terminals. The TUSB9261 can also output a pulse width modulated signal that can be used to drive an activity LED.

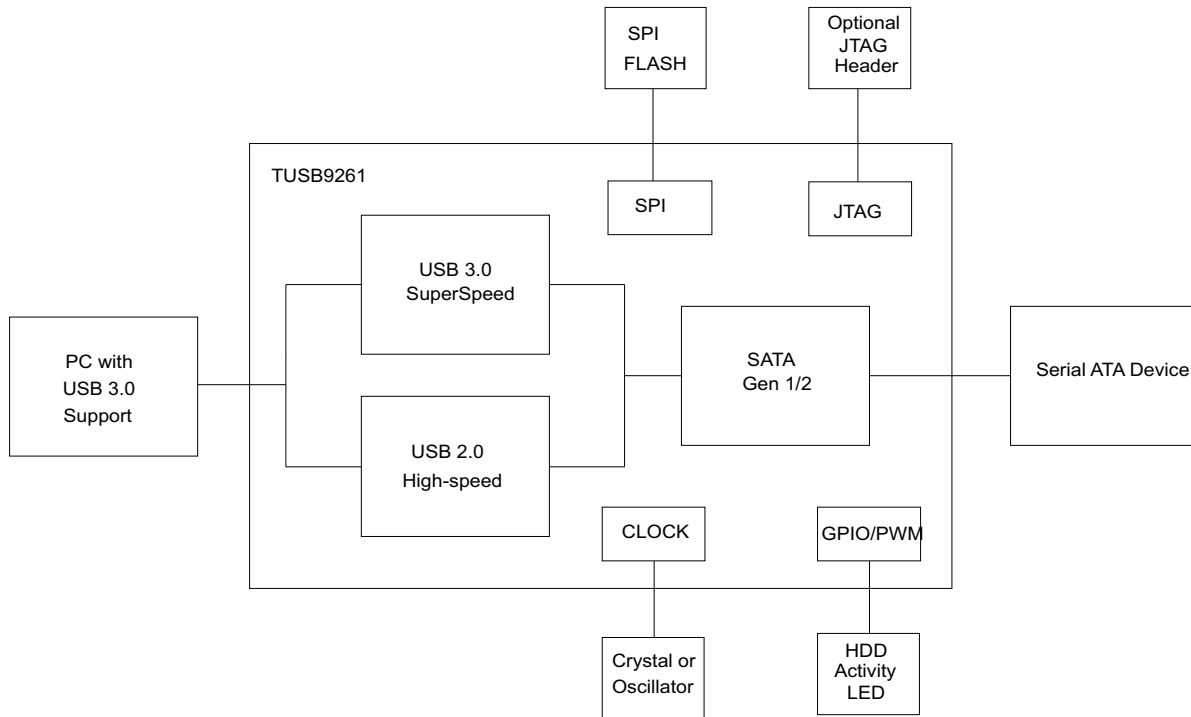


Figure 1. Typical System Implementation

2 Power Considerations

2.1 1.1-V and 3.3-V Digital Supplies

The TUSB9261 requires 1.1-V and 3.3-V digital power source.

The 1.1-V terminals are named VDD11. These terminals supply power to the digital core. The 1.1-V core allows for a significant reduction in both power consumption and logic switching noise.

The 3.3-V terminals are named VDD33 and supply power to most of the input and output cells.

Both VDD11 and VDD33 supplies must have 0.1- μ F bypass capacitors to VSS (ground) to ensure proper operation. One capacitor per power terminal is sufficient and should be placed as close to the terminal as possible to minimize trace length. Smaller value capacitors like 0.01- μ F are also recommended on the digital supply terminals.

When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

2.2 1.1-V and 3.3-V Analog Supplies

A Pi filter is recommended on all analog power terminals to minimize circuit noise. These filters can be combined on a per-rail basis for a total of two (VDDA11/VDDA11_USB2) + (VDDA33).

Analog power terminals must have a 1- μ F and a 10- μ F bypass capacitor connected to VSSA (ground) to ensure proper operation. Place the capacitor as close as possible to the associated terminal to minimize trace length. Smaller value capacitors such as 0.1- μ F and 0.01- μ F are also recommended on the analog supply terminals.

2.3 Ground Terminals

VSS, VSSA, and VSS33 can be connected together to form one ground plane. This technique allows for creating a large image plane for the signal layer directly adjacent to the ground plane.

2.4 Capacitor Selection Recommendations

When selecting bypass capacitors for the TUSB9261 device, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and low-cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low-frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell "D" size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce low-frequency power supply noise and ripple.

2.5 Power-Up/Down Sequencing

All TUSB9261 analog and digital power terminals must be controlled during the power-up and power-down sequence to ensure that absolute power terminal ratings are not exceeded as doing so can result in damage to the device.

No particular power-up or power-down sequencing of the power rails is required.

For additional power requirements, please refer to the TUSB9261 Data Manual ([SLLS962](#)).

2.6 External Voltage Regulator Recommendation

Since the TUSB9261 requires two voltage supplies (1.1-V and 3.3-V) a multi-channel voltage regulator is recommended. The TPS650061 or TPS65024x are good choices. The TPS650061 utilizes a DCDC converter and two LDO regulators in a single package. The DCDC converter can supply 1-A nominal current while the two LDO's can supply 300-mA nominal current. Since the 1.1-V supply can consume upwards of 340-mA of current the DCDC converter is ideal for supplying the 1.1-V current while the two LDO's can be used to supply 3.3- V current. Likewise the TPS65024x utilizes three DCDC converters and three LDO's. Both devices also have a built in supervisor circuit that can be connected to GRST# on the TUSB9261.

2.7 TUSB9261 Power Consumption

Table 1. SuperSpeed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA) ⁽¹⁾	TYPICAL SUSPEND CURRENT (mA) ⁽²⁾
VDD11	291	153
VDD33 ⁽³⁾	65	28

⁽¹⁾ Transferring data via SS USB to a SSD SATA Gen II device. No SATA power management, U0 only.

⁽²⁾ SATA Gen II SSD attached no active transfer. No SATA power management, U0 only.

⁽³⁾ All 3.3-V power rails connected together.

Table 2. High Speed USB Power Consumption

POWER RAIL	TYPICAL ACTIVE CURRENT (mA) ⁽¹⁾	TYPICAL SUSPEND CURRENT (mA) ⁽²⁾
VDD11	172	153
VDD33 ⁽³⁾	56	28

⁽¹⁾ Transferring data via HS USB to a SSD SATA Gen II device. No SATA power management.

⁽²⁾ SATA Gen II SSD attached no active transfer. No SATA power management.

⁽³⁾ All 3.3-V power rails connected together.

2.8 USB VBUS

Power can be supplied via a USB cable on the terminal VBUS. VBUS is a 5-V source that is connected to the USB_VBUS terminal on the TUSB9261 via a voltage divider. Connect a 90.9-k Ω , 1% resistor from the cable VBUS connector to the USB_VBUS terminal on the TUSB9261 and a 10-k Ω , 1% resistor from USB_VBUS to ground.

2.8.1 Limiting Inrush Current on VBUS

To prevent inrush current the TI TPS2560/61 is recommended. Inrush current can occur on VBUS when a function is plugged into the network. For example the bulk capacitance used to supply power to the SATA device can be quite large, causing inrush current when the USB cable is connected. The TPS2560/61 power-distribution switches are intended for applications where heavy capacitive loads are likely to be encountered. The TPS2560/61 has two controllable outputs that can be controlled via the TUSB9261 GPIO terminals. In the example implementation the TUSB9261 is used to switch power on or off to the SATA device by controlling the EN2 terminal on the TPS2561.

3 USB Connection

There are three sets of differential pairs for connecting the USB port; one set for High-Speed and two sets for SuperSpeed.

3.1 High-Speed Differential Routing

The high-speed differential pair (USB_DM and USB_DP) is connected to a USB type B connector. The differential pair traces should be routed with 90- Ω , $\pm 15\%$ differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between High-Speed USB signal pairs should be no greater than 150 mils. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. No termination or coupling caps are required. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins. Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).

In order to minimize cross-talk on the USB2/3 differential signal pairs, it is recommended that the spacing between the two interfaces be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs and the DP/DM differential pair.

If this 5W rule cannot be implemented, then the space between the TX/RX differential pairs and DP/DM differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

3.2 SuperSpeed Differential Routing

SuperSpeed consists of two differential routing pairs, a transmit pair (USB_SSTXM and USB_SSTXP) and a receive pair (USB_SSRXM and USB_SSRXP). Each differential pair's traces should be routed with 90- Ω , $\pm 15\%$ differential impedance. The high-speed signal pair should be trace length matched. Maximum trace length mismatch between SuperSpeed USB signal pairs should be no greater than 2.5 mils. The transmit differential pair does not have to be the same length as the receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. The transmitter differential pair requires 0.1- μF coupling caps for proper operation. The package/case size of these caps should be no bigger than 0402. C-packs are not allowed. The caps should be placed symmetrically as close as possible to the USB connector signal pins. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins (closer than the transmitter caps). Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter caps).

It is permissible to swap the plus and minus on either or both of the SuperSpeed differential pairs. This may be necessary to prevent the differential traces from crossing over one another. However it is not permissible to swap the transmitter differential pair with receive differential pair.

In order to minimize cross-talk on the SS USB differential signal pairs, it is recommended that the spacing between the TX and RX signal pairs be five times the width of the trace (5W rule). For instance, if the SS USB TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

4 SATA Connection

The TUSB9261 supports one 3G SATA port operating at 1.5 GHz or 3 GHz depending on the maximum speed of the attached device.

4.1 SATA Differential Routing

The SATA traces (SATA_TXP and SATA_TXM) should be routed with 100- Ω , $\pm 15\%$ differential impedance. Maximum trace length mismatch between SATA signal pairs should be no greater than

2.5 mils. Transmit differential pair does not have to be the same length as receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. Each SATA trace requires a coupling capacitor be placed inline. The package/case size of these caps should be no bigger than 0402. C-packs are not allowed. The caps should be placed symmetrically as close as possible to the SATA connector signal pins.

It is permissible to swap the plus and minus on the SATA differential pair. This may be necessary to prevent the differential traces from crossing over one another. However it is not permissible to swap the transmitter diff pair with the receive diff pair.

In order to minimize cross-talk on the SATA differential signal pairs, it is recommended that the spacing between the TX and RX signal pairs for each interface be five times the width of the trace (5W rule). For instance, if the SATA TX/RX differential pair trace widths are 5 mils, then there should be 25 mils of space (air gap) between the TX and RX differential pairs.

If this 5W rule cannot be implemented, then the space between the TX and RX differential pairs should be maximized as much as possible and ground-fill should be placed between the two. In this case, it is better to route each differential pair on opposite sides of the board with a ground plane between them.

5 ESD Protection

The TUSB9261 provides ESD protection on all signal and power pins up to 1500 V using the human body model and 500 V using the charged device model. If more protection is required, the TI TPD2EUB30 can be used as this device meets or exceeds IEC61000-4-2 (Level 4) requirements. This device can be used on any of the differential pairs of the TUSB9261. Place the device as close as possible to the signal pins of the connector. Refer to the datasheet for more information regarding this device.

6 GPIO Terminals

The TUSB9261 can support a maximum of 12 GPIOs. Some GPIO terminals have dual functionality depending on how they are configured. Unused terminals should be left unconnected.

The default firmware configuration of GPIOs is as follows in [Table 3](#).

Output GPIOs for LEDs are driven Low when the LED should be ON.

Table 3. Default Firmware Configuration of GPIOs

GPIO	DIRECTION	USAGE
0	Out	Firmware Heartbeat LED
1	Out	SuperSpeed USB Link State 0 LED
2	Out	HS/FS Suspend LED
3	In	Push-Button to signal remote wake. Internal Pull-Down enabled.
4	In	Bus or Self-powered indicator. Level should be High when self-powered and Low if bus-powered. Internal Pull-Down enabled.
5	Out	SuperSpeed USB Link State 1 LED
6	Out	USB 2.0 Connection LED
7	Out	SuperSpeed Connection LED
8	In	UART Rx. Alternate usage for an output GPIO with default logic level High can be enabled in custom firmware.
9	Out	UART Tx (for debug msgs)
10	In	Undefined. Internal Pull-Up enabled. Alternate usage for SATA power switch control can be enabled in custom firmware.
11	In	Power fault input. Internal Pull-Up enabled.

6.1 GPIO[7:0]

GPIO terminals 7 through 0 can be used for general purpose use such as connecting activity LEDs, used as a push-button input, or connected to various signals from other devices. Input GPIO terminals have internal pull-down resistors. If a GPIO terminal is not used it should be left unconnected.

6.2 GPIO[8/UART_RX:9/UART_TX]

GPIO terminals 8 and 9 are dual function terminals. They can be used as general purpose input/output terminals like GPIO[7:0] or they can be configured as an UART interface. Both terminals have internal pull-up resistors, so they can be left unconnected if not used.

6.3 GPIO[10/SPI_CS2:11/SPI_CS1]

GPIO terminals 10 and 11 are dual function terminals. They can be used as general purpose input/output terminals like GPIO[7:0] or they can be configured as SPI chip select terminals for additional peripherals such as an LCD driver. Both terminals have internal pull-up resistors, so they should be left unconnected if not used.

7 PWM Terminals

The TUSB9261 has two pulse width modulated (PWM) output terminals.

The default firmware configuration of PWMs is as follows in [Table 4](#).

Table 4. Default Firmware Configuration of PWMs

PWM	USAGE
0	Primary Indicator LED: ON when there is a USB connection. OFF when there is no connection. Blinks during disk activity (Frequency: 10Hz for USB2 or 20Hz for USB3). Fades when USB is in Suspend or U3 state.
1	Power Indicator LED.

PWM duty cycle will be 0% when the LED should be fully ON.

8 JTAG Interface

The TUSB9261 supports JTAG for board level test and debug support. Typically these terminals are left unconnected or routed to a header to plug in an external JTAG controller. [Table 5](#) shows the JTAG terminal names and internal resistor connection. The JTAG interface should be left unconnected if JTAG support is not required.

Table 5. Internal JTAG Resistor Termination

NAME	PULL-UP OR PULL-DOWN	DESCRIPTION
JTAG_TCK	Pull-down	JTAG test clock
JTAG_TDI	Pull-up	JTAG test data in
JTAG_TDO	Pull-down	JTAG test data out
JTAG_TMS	Pull-up	JTAG test mode select
JTAG_RSTZ	Pull-down	JTAG reset

9 External Reference Clock

The TUSB9261 requires an external reference clock. This clock can be derived from an existing clock, crystal, or oscillator. The TUSB9261 supports 40 MHz. FREQSEL[1:0] terminals must be tied to VDD33.

9.1 Crystal Selection

Select a fundamental mode crystal with load capacitance of 12 pF – 24 pF and PPM rating of ± 100 PPM or better. Connect the crystal between the XI and XO terminals with a 1-M Ω shunt resistor as shown in Figure 2. Place the crystal near the XI and XO terminals. Try to keep the XI and XO traces to a minimum length with few or no vias as shown in Figure 3.

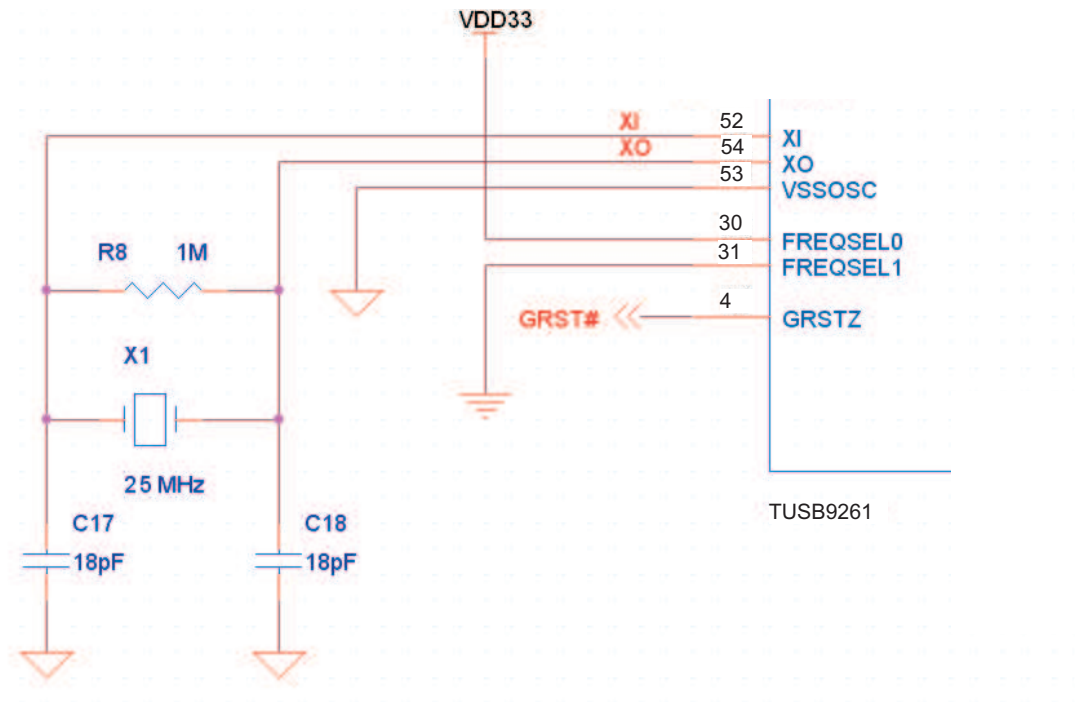


Figure 2. Example Crystal Implementation

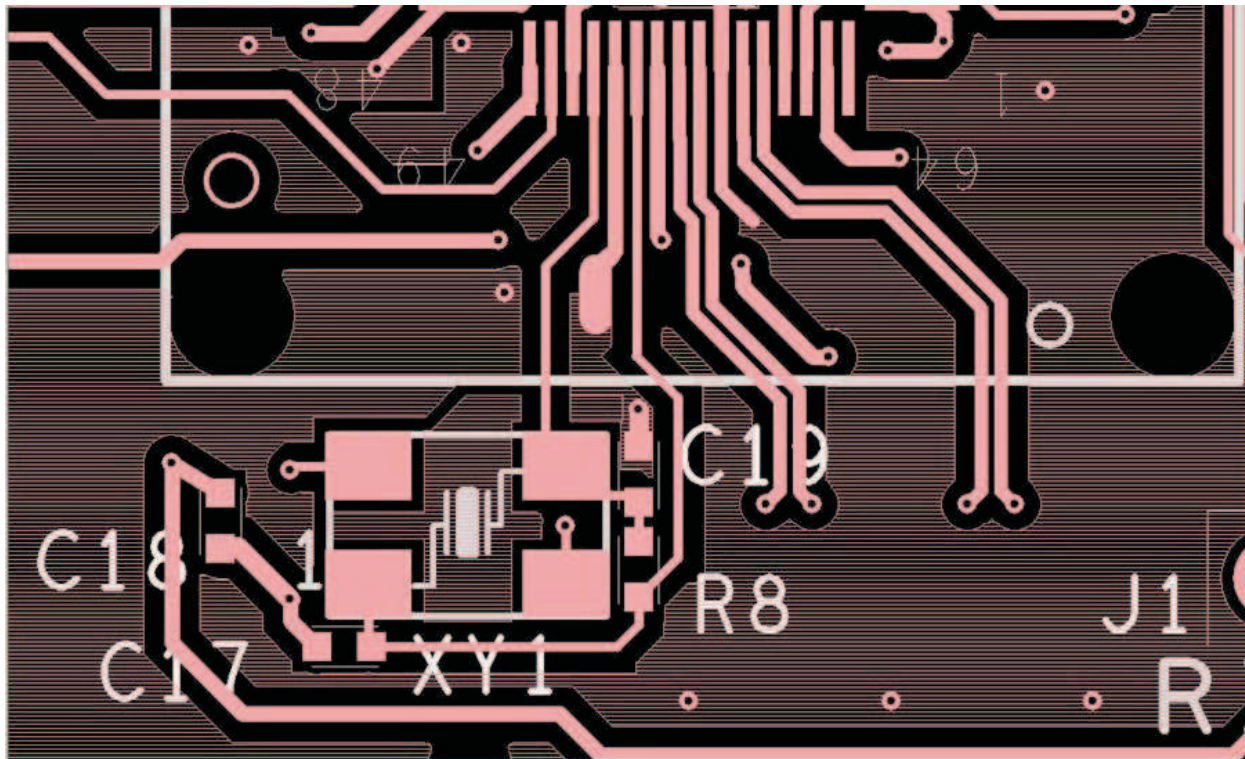


Figure 3. Example Reference Clock Layout

9.2 External Clock/Oscillator Selection

When using an external clock source such as an oscillator, the reference clock should have ± 100 PPM (or better) frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function.

Connect the output of the clock source or oscillator to the XI terminal. Leave the XO terminal unconnected as shown in [Figure 4](#). Try to keep the clock trace to a minimum length with few or no vias.

Note that the TUSB9261 has a VSSOSC terminal. This terminal is the reference ground for the internal oscillator. This reference ground should be used for the crystal circuit, which is also shown in [Figure 4](#).

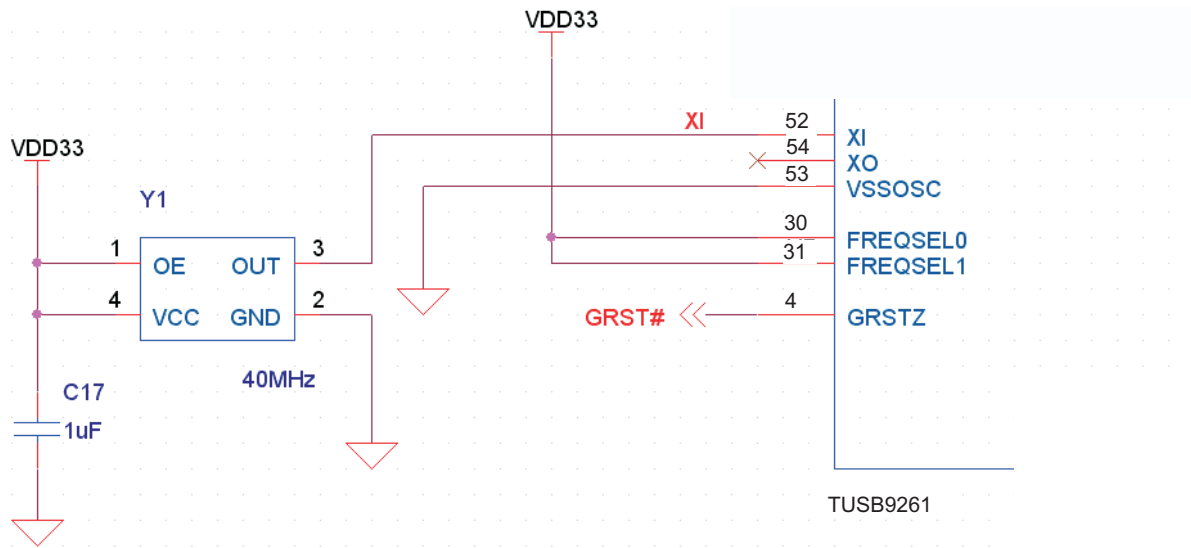


Figure 4. Example Oscillator Implementation

10 Serial Peripheral Interface (SPI)

A SPI system consists of one master device and one or more slave devices. The TUSB9261 is a SPI master providing the SPI clock, data-in, data-out and up to three chip select terminals.

The SPI has a 4-wire synchronous serial interface. Data communication is enabled with a low active Chip Select terminal (SPI_CS[2:0]#). Data is transmitted with a 3-terminal interface consisting of terminals for serial data input (SPI_DATA_IN), serial data output (SPI_DATA_OUT) and serial clock (SPI_SCLK). All SPI terminals have integrated pull-up resistors. No external components are required to connect the SPI interface to an external SPI flash device. See Figure 5 for an example implementation of the SPI interface using one SPI slave device.

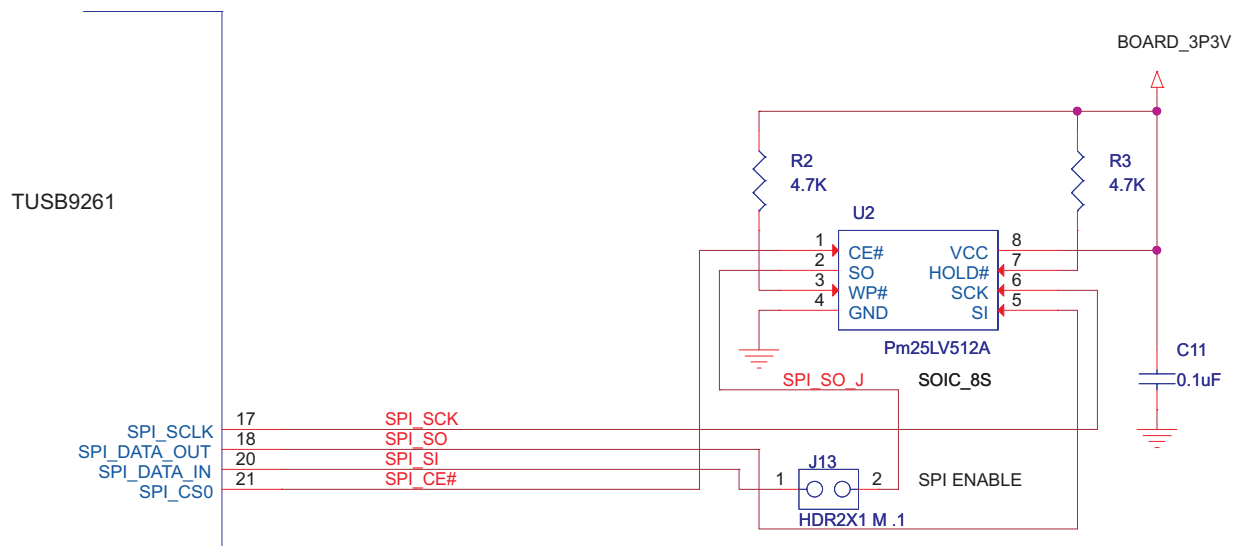
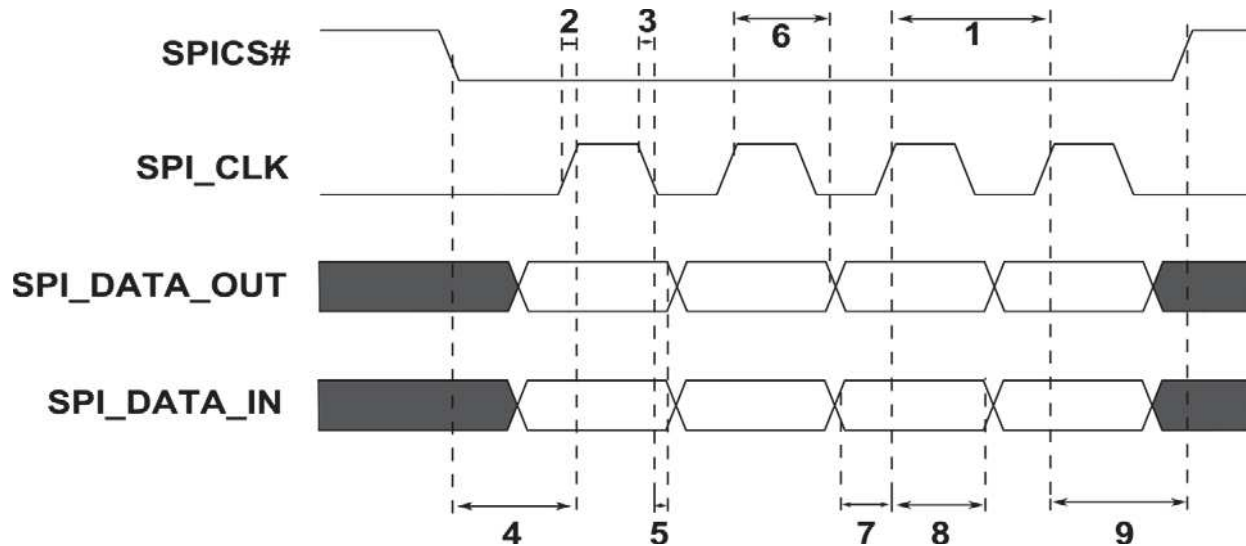


Figure 5. SPI Connection

The SPI_CLK is running at a fixed frequency of 18.75 MHz and its clocking mode is configured with a POLARITY of 0 and a PHASE of 1, this means that the SPI interface sends the data output one half-cycle before the first rising edges of SPI_CLK and on subsequent falling edges, meanwhile the input data is latched on the rising edge of SPI_CLK (see Figure 6 and Table 6 for a detailed timing description). The flash memory is erased by the bootloader prior to programming and must use a word size of 8 bits with an address length of 24 bits and its program instruction must allow 256 bytes to be written in one operation. A minimum flash size of 512 kbits (64 k x 8) is recommended. Table 7 shows SPI flash devices that have been tested with the TUSB9261.


Figure 6. SPI Characterization
Table 6. SPI Characterization

NUMBER	TIME REFERENCE	THEORETICAL VALUE
1	Cycle Time SPICLK	53.3ns
2	Positive SPI_CLK slope	2ns
3	Negative SPI_CLK slope	3ns
4	SPICCS - SPICLK edge (PHASE= 1)	min: 53.3ns typ: 80ns Max: 93.3ns
5	Output Delay time, SPICLK TX edge to SPISIMO valid	260ps
6	Output Hold time, SPICLK RX edge to SPISIMO valid	26.7ns
7	Setup time	22ns
8	Hold Time	500ps
9	"SPICLK -SPICCS Phase = '1', Master"	13.3ns

Table 7. Flash Devices Tested on the TUSB9261

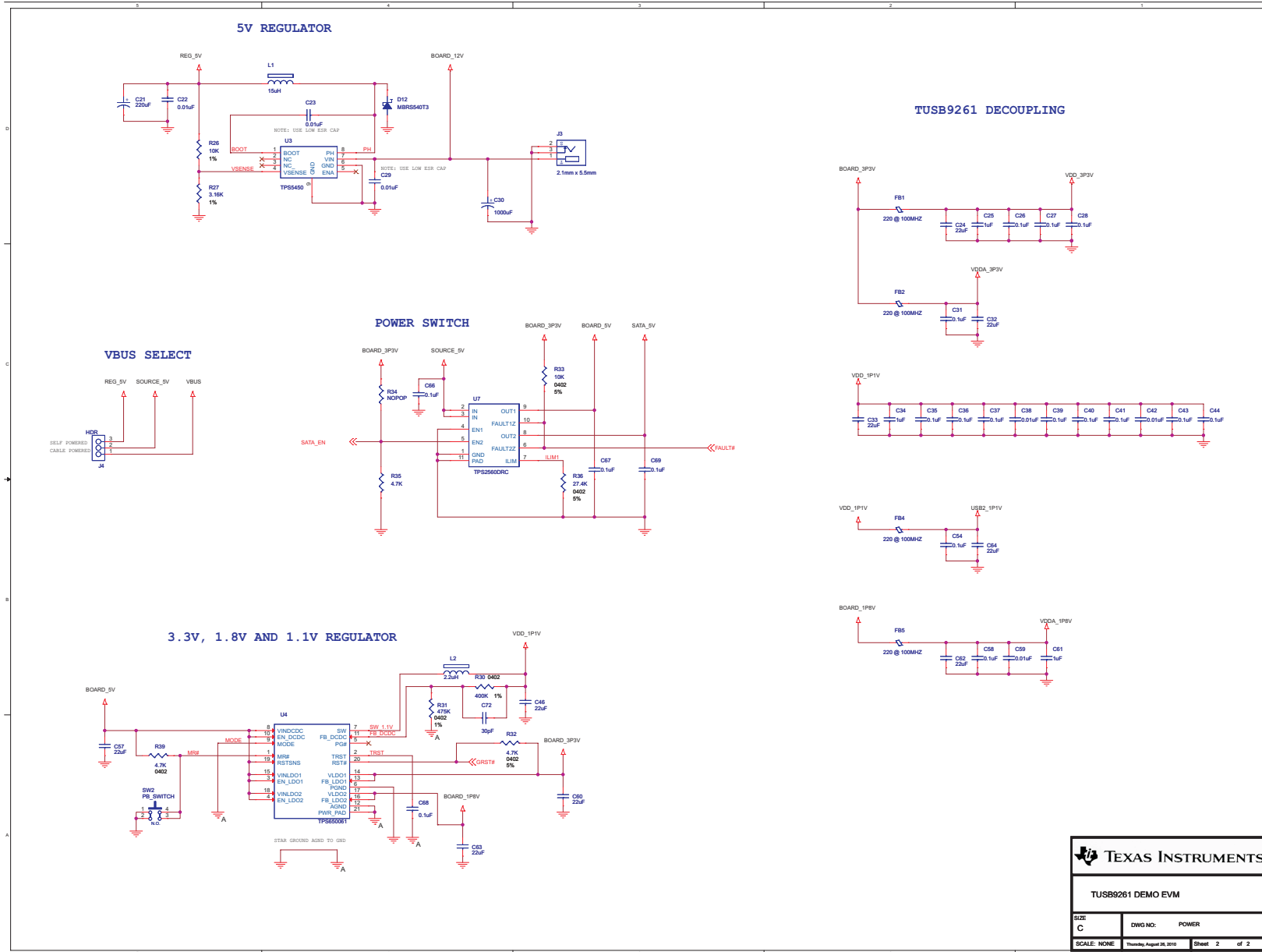
MANUFACTURER	PART NUMBER	DENSITY (kbit)	PAGE SIZE (bytes)	MAX CLOCK FREQUENCY READ COMMAND (MHz)
Numonyx/ST	M25P05A	512	256	20 / 25
Numonyx/ST	M25P10A	1024	256	20 / 25
Atmel	AT25FS010	1024	256	50
Pflash	Pm25LV512A	512	256	33
Pflash	Pm25LV010A	1024	256	33

11 Precision Reference Return Resistor

The TUSB9261 requires an external precision reference return resistor. This resistor is part of the USB2.0 PHY core used for internal calibration. A 10-k Ω , $\pm 1\%$ (1/20 W or greater) precision resistor should be placed between terminals USB_R1 and USB_R1RTN. This resistor should be placed no further than 500 mils from the two terminals.

12 Example Schematics

The following schematic is provided as a reference design. There is one user configurable jumper (J4) on the board. A jumper must be placed across pins 1 and 2 or across pins 2 and 3 depending on the desired power option. When the jumper is placed across pins 1 and 2 a flash drive can be powered directly from the USB cable power eliminating the need for an external wall-wart. However it should be noted that SATA devices that require 12 V will not operate in this mode. To support all SATA devices place the jumper across pins 2 and 3 and connect a 12-V / 2-A wall-wart to DC jack J3 (positive tip).



TEXAS INSTRUMENTS	
TUSB9261 DEMO EVM	
SIZE C	DWG NO.: POWER
SCALE: NONE	Thursday, August 26, 2010 Sheet 2 of 2

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