Application Note
SLLA135 – March 2003

TFP410/TFP510 Design Notes

Digital Visual Interface

ABSTRACT

The Texas Instruments TFP410/TFP510 is one device in a family of TI *PanelBus*™ digital display products that simplifies digital display systems design by offering value added flexibility and reliability to the system designer. The TFP410 /TFP510 is a DVI 1.0 compliant digital transmitter that supports display resolutions ranging from VGA to UXGA in 24-bit, true-color pixel format. The TFP410/TFP510 offers design flexibility in that it can be configured to support 12-bit (dual edge) and 24-bit (single edge) input modes.

The TFP410/TFP510 combines *PanelBus*™ circuit innovation with TI's advanced 0.18-um EPIC-5™ CMOS process technology along with TI PowerPAD™ package technology to achieve a reliable, low-powered, low noise, high-speed digital solution to digital visual interfacing.

Fundamental Operation

The TFP410/TFP510 is a DVI (Digital Visual Interface) compliant digital transmitter that is used in PC and consumer electronics applications to encode and transmit T.M.D.S. encoded RGB pixel data streams. In a digital display system a host, usually a PC or workstation, contains a DVI compliant transmitter, like the TFP410/TFP510. The TFP410/TFP510 receives 24-bit pixel data along with appropriate control signals and encodes them into a high-speed low-voltage differential serial bit stream fit for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor or digital projector, requires a DVI compliant receiver like the TI TFP401 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the display drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred. The TFP410/TFP510 supports resolutions up to UXGA (1600x1200.)

Routing High-Speed Differential Signal Traces

(TxC-, TxC+, Tx0-, Tx0+, Tx1-, Tx1+, Tx2-, Tx2+)

Trace impedance should be controlled for optimal performance, 50 ohms recommended. Each differential pair should be equal in length and symmetrical and should have equal impedance to ground with a trace separation of 2x to 4x Height. A differential trace separation of 4x Height yields about 6% cross-talk (6% effect on impedance).

We recommend that differential trace routing should be side-by-side, though it is not important that the differential traces be tightly coupled together because tight coupling is not achievable on PCB traces. Typical ratios on PCB's are only 20-50%; 99.9% is the value of a well-balanced twisted-pair cable.

Each differential trace should be as short as possible (< 2” preferably) with no 90° angles. These high-speed transmission traces should be on an outer layer with a continuous ground plane on the next plane layer.

TxC-, TxC+, Tx0-, Tx0+, Tx1-, Tx1+, Tx2-, Tx2+ signals all route directly from the device to the DVI connector pins, no external components are needed.

Operation at UXGA resolution will require careful construction of the transmission lines and selection of high quality cables and connectors.

DVI Connector Routing

Clear-out holes for connector pins should leave space between pins to allow continuous ground through the pin field. Allow enough spacing in ground plane around signal pin vias, however. Keep enough copper between vias to allow for ground current to flow between the vias. Avoid creating a large ground plane slot around the entire connector; minimizing the via capacitance is the goal.

Data and Control Signal Output Routing

The trace length of data and control signals out of the transmitter should be kept as close to equal as possible. Trace separation should be ~5x Height. Fast edges from data sources are expected to require consideration of these traces as transmission lines. The transmitter does not provide termination of the signal lines internal to the chip. Refer to routing and termination recommendations from the provider of the data source.

Power Supply De-coupling

Use solid ground planes, tie ground planes together with as many vias as is practical. This provides a desirable return path for current. Each supply should be on separate split power planes, where each power plane should be as large an area as possible. Connect PanelBus transmitter power and ground pins and all by-pass caps to the appropriate power or ground plane with a via. Vias should be as fat and short as practical; the goal is to minimize the inductance.

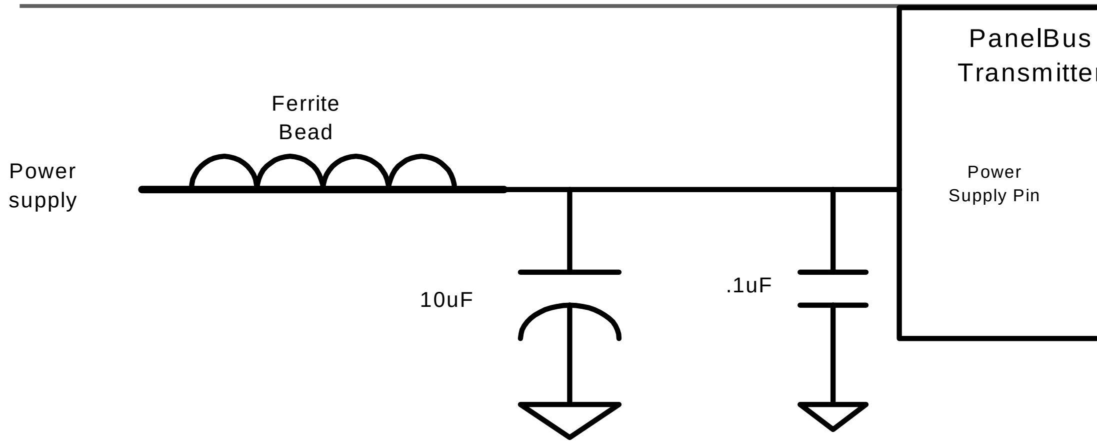
The number and size of the decoupling capacitors required will depend on the design of the circuit board. The three power supplies for the chip, DVDD, PVDD, and TVDD should be treated similarly:

Place one 0.1-uF capacitor as close as possible between each device power pin and ground.

A bulk decoupling capacitor such as a 10-uF or 22-uF tantalum capacitor should be placed on the sub-plane between the supply and 0.1-uF capacitors.

A ferrite bead should be used to separate the sub-plane from the source.

Additional capacitors may be needed depending on the size of the sub-planes and impedance of the ferrite beads and capacitors.



PowerPad™ Connection

Designing boards for PowerPad™ connection is optional, there are benefits with the use of TI's PowerPad™ Technology.

Ground plane dimensions for TI's 64-Pin PAP package are 10 x 10 mm.

Maximum land area = 10 mm

Reference the following website for detailed PowerPad™ information:

http://www-s.ti.com/sc/psheets/slma002/slma002.pdf

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