

Errata  
**MSP430G2544 Microcontroller**



**ABSTRACT**

This document describes the known exceptions to the functional specifications (advisories).

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**Table of Contents**

<b>1 Functional Advisories</b> .....	<b>2</b>
<b>2 Preprogrammed Software Advisories</b> .....	<b>2</b>
<b>3 Debug Only Advisories</b> .....	<b>2</b>
<b>4 Fixed by Compiler Advisories</b> .....	<b>3</b>
<b>5 Nomenclature, Package Symbolization, and Revision Identification</b> .....	<b>4</b>
5.1 Device Nomenclature.....	4
5.2 Package Markings.....	4
5.3 Memory-Mapped Hardware Revision (TLV Structure).....	5
<b>6 Advisory Descriptions</b> .....	<b>6</b>
<b>7 Revision History</b> .....	<b>19</b>

## 1 Functional Advisories

Advisories that affect the device's operation, function, or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev J	Rev H
<a href="#">BCL12</a>	✓	✓
<a href="#">BCL16</a>	✓	✓
<a href="#">CPU45</a>	✓	✓
<a href="#">FLASH24</a>	✓	✓
<a href="#">FLASH27</a>	✓	✓
<a href="#">FLASH36</a>	✓	✓
<a href="#">PORT10</a>	✓	✓
<a href="#">SYS15</a>	✓	✓
<a href="#">TA12</a>	✓	✓
<a href="#">TA16</a>	✓	✓
<a href="#">TA21</a>	✓	✓
<a href="#">TAB22</a>	✓	✓
<a href="#">TB2</a>	✓	✓
<a href="#">TB16</a>	✓	✓
<a href="#">TB24</a>	✓	✓
<a href="#">USCI20</a>	✓	✓
<a href="#">USCI21</a>	✓	✓
<a href="#">USCI22</a>	✓	✓
<a href="#">USCI23</a>	✓	✓
<a href="#">USCI24</a>	✓	✓
<a href="#">USCI25</a>	✓	✓
<a href="#">USCI26</a>	✓	✓
<a href="#">USCI27</a>	✓	✓
<a href="#">USCI30</a>	✓	✓
<a href="#">USCI34</a>	✓	✓
<a href="#">USCI35</a>	✓	✓
<a href="#">USCI40</a>	✓	✓
<a href="#">XOSC5</a>	✓	✓

## 2 Preprogrammed Software Advisories

Advisories that affect factory-programmed software.

✓ The check mark indicates that the issue is present in the specified revision.

The device does not have any errata for this category.

## 3 Debug Only Advisories

Advisories that affect only debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev J	Rev H
<a href="#">EEM20</a>	✓	✓

## 4 Fixed by Compiler Advisories

Advisories that are resolved by compiler workaround. Refer to each advisory for the IDE and compiler versions with a workaround.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev J	Rev H
<a href="#">CPU19</a>	✓	✓

Refer to the following MSP430 compiler documentation for more details about the CPU bugs workarounds.

### TI MSP430 Compiler Tools (Code Composer Studio IDE)

- [MSP430 Optimizing C/C++ Compiler](#): Check the --silicon\_errata option
- [MSP430 Assembly Language Tools](#)

### MSP430 GNU Compiler (MSP430-GCC)

- [MSP430 GCC Options](#): Check -msilicon-errata= and -msilicon-errata-warn= options
- [MSP430 GCC User's Guide](#)

### IAR Embedded Workbench

- [IAR workarounds for msp430 hardware issues](#)

## 5 Nomenclature, Package Symbolization, and Revision Identification

The revision of the device can be identified by the revision letter on the [Package Markings](#) or by the [HW\\_ID](#) located inside the TLV structure of the device.

### 5.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

Support tool naming prefixes:

**X**: Development-support product that has not yet completed Texas Instruments internal qualification testing.

**null**: Fully-qualified development-support product.

XMS devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

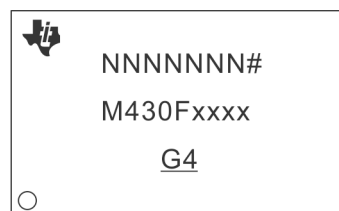
Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format.

### 5.2 Package Markings

**DA38**

**TSSOP (DA), 38 Pin**



# = Die revision  
○ = Pin 1 location  
N = Lot trace code

**RHA40**

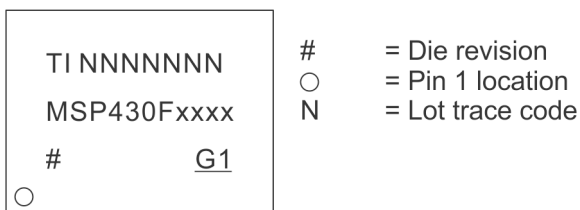
**QFN (RHA), 40 Pin**



# = Die revision  
○ = Pin 1 location  
N = Lot trace code

**YFF49**

**DSBGA (YFF), 49 Pin**



### 5.3 Memory-Mapped Hardware Revision (TLV Structure)

This device does not support reading the hardware revision from memory.

Further guidance on how to locate the TLV structure and read out the HW\_ID can be found in the device User's Guide.

## 6 Advisory Descriptions

### BCL12 *BCL Module*

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**Category** Functional

**Function** Switching RSELx or modifying DCOCTL can cause DCO dead time or a complete DCO stop

**Description** After switching RSELx bits (located in register BCSTL1) from a value of >13 to a value of <12 OR from a value of <12 to a value of >13, the resulting clock delivered by the DCO can stop before the new clock frequency is applied. This dead time is approximately 20 us. In some instances, the DCO may completely stop, requiring a power cycle.

Furthermore, if all of the RSELx bits in the BCSTL1 register are set, modifying the DCOCTL register to change the DCOx or the MODx bits could also result in DCO dead time or DCO hang up.

**Workaround** - When switching RSEL from >13 to <12, use an intermediate frequency step. The intermediate RSEL value should be 13.

Current RSEL	Target RSEL	Recommended Transition Sequence
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

AND

- When switching RSEL from <12 to >13 it's recommended to set RSEL to its default value first (RSEL = 7) before switching to the desired target frequency.

AND

- In case RSEL is at 15 (highest setting) it's recommended to set RSEL to its default value first (RSEL = 7) before accessing DCOCTL to modify the DCOx and MODx bits. After the DCOCTL register modification the RSEL bits can be manipulated in an additional step.

In the majority of cases switching directly to intermediate RSEL steps as described above will prevent the occurrence of BCL12. However, a more reliable method can be implemented by changing the RSEL bits step by step in order to guarantee safe function without any dead time of the DCO.

Note that the 3-step clock startup sequence consisting of clearing DCOCTL, loading the BCSTL1 target value, and finally loading the DCOCTL target value as suggested in the in the "TLV Structure" chapter of the [MSP430x2xx Family User's Guide](#) is not affected by BCL12 if (and only if) it is executed after a device reset (PUC) prior to any other modifications being made to BCSTL1 since in this case RSEL still is at its default value of 7. However any further changes to the DCOx and MODx bits will require the consideration of the workaround outlined above.

### BCL16 *BCL Module*

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**Category** Functional

**Function** SMCLK clock source selection from XT1/VLO to DCO

**Description** When the MCLK and the SMCLK do not use the DCO, the DCO is off. The DCO does not start if the clock source for SMCLK is changed from XT1/VLO to DCO. As a result, the SMCLK remains high. Note: This is only true for SMCLK. The DCO starts if the clock source of MCLK is set to DCO.

**Workaround** Set clock source of MCLK to DCO by either:

1)setting the selection bits SELMx of BCSCTL2 register to '00' or '01'.

OR

2)setting the OFIFG bit of IFG1 register. Note: This triggers the oscillator fault logic that automatically starts the DCO. Reset the OFIFG bit to further use the XT1/VLO.

For both options, if the XT1/VLO is still required to source MCLK, revert the clock source of MCLK back to XT1/VLO afterwards.

## CPU19

### CPU Module

**Category** Compiler-Fixed

**Function** CPUOFF modification may result in unintentional register read

**Description** If an instruction that modifies the CPUOFF bit in the Status Register is followed by an instruction with an indirect addressed operand (e.g. MOV @R8, R9, RET, POP, POPM), an unintentional register read operation can occur during the wakeup of the CPU. If the unintentional read occurs to a read sensitive register (e.g. UCB0RXBUF, TAIV), which changes its value or the value of other registers (IFG's), the bug leads to lost interrupts or wrong register read values.

**Workaround** Insert a NOP instruction after each CPUOFF instruction.

OR

Refer to the table below for compiler-specific fix implementation information. Note that compilers implementing the fix may lead to double stack usage when RET/RETA follows the compiler-inserted NOP.

IDE/Compiler	Version Number	Notes
IAR Embedded Workbench	IAR EW430 v6.20.1 until v6.40	User is required to add the compiler or assembler flag option below. --hw_workaround=nop_after_lpm
IAR Embedded Workbench	IAR EW430 v6.40 or later	Workaround is automatically enabled
TI MSP430 Compiler Tools (Code Composer Studio)	15.12.0.LTS	User is required to add the compiler or assembler flag option below. --silicon_errata=CPU19
MSP430 GNU Compiler (MSP430-GCC)	MSP430-GCC 4.9 build 389 or later	User is required to add the compiler or assembler flag option below. -msilicon-errata=cpu19 -msilicon-errata-warn=cpu19 generates a warning in addition

IDE/Compiler	Version Number	Notes
MSP430 GNU Compiler (MSP430-GCC)	MSP430-GCC 5.x build 14 or later	User is required to add the compiler or assembler flag option below. -msilicon-errata=cpu19 -msilicon-errata-warn=cpu19 generates a warning in addition

**CPU45*****CPU Module*****Category**

Functional

**Function**

CPU speed performance limitation

**Description**

The CPU register contents may become unpredictable during CPU register operations if the device operates at minimum Vcc required for system speed performance above 4.15MHz under certain conditions. This is dependent on voltage and CPU clock (MCLK) frequency and duty-cycle.

**Workaround**

With respect to the system speed performance above 4.15MHz versus minimum required Vcc

1. Increase Vcc by 200mV for DCO calibrated frequencies when sourced to MCLK  
OR
2. Use internally divided clock for MCLK (BCSCTL2.DIVMx > 00)  
OR
3. Use external clock with 50% positive duty cycle when sourced to MCLK  
OR
4. Reduce LFXT1 (used in HF mode) or external clock frequency by 20% when sourced to MCLK  
OR
5. Reduce DCO speed by 20% when DCO is sourced to MCLK

**EEM20*****EEM Module*****Category**

Debug

**Function**

Debugger might clear interrupt flags

**Description**

During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes.

**Workaround**

None.

**FLASH24*****FLASH Module*****Category**

Functional

**Function**

Write or erase emergency exit can cause failures

**Description**

When a flash write or erase is abruptly terminated, the following flash accesses by the CPU may be unreliable resulting in erroneous code execution. The abrupt termination can be the result of one the following events:

- 1) The flash controller clock is configured to be sourced by an external crystal. An oscillator fault occurs thus stopping this clock abruptly.  
or
- 2) The Emergency Exit bit (EMEX in FCTL3) when set forces a write or an erase



operation to be terminated before normal completion.

or

3) The Enable Emergency Interrupt Exit bit (EEIEX in FCTL1) when set with GIE=1 can lead to an interrupt causing an emergency exit during a Flash operation.

**Workaround**

1) Use the internal DCO as the flash controller clock provided from MCLK or SMCLK.

or

2) After setting EMEX = 1, wait for a sufficient amount of time before Flash is accessed again.

or

3) No Workaround. Do not use EEIEX bit.

**FLASH27**

***FLASH Module***

**Category**

Functional

**Function**

EI feature can disrupt segment erase

**Description**

When a flash segment erase operation is active with EEI feature selected (EEI=1 in FLCTL1) and GIE=0, the following can occur:

An interrupt event causes the flash erase to be stopped, and the flash controller expects an RETI to resume the erase. Because GIE=0, interrupts are not serviced and RETI will never happen.

**Workaround**

1) Do not set bit EEI=1 when GIE = 0.

or,

2) Force an RETI instruction during the erase operation during the check for BUSY=1 (FCTL3).

Sample code:

```
MOV R5, 0(R5) ; Dummy write, erase segment
LOOP: BIT #BUSY, &FCTL3 ; test busy bit
JMP SUB_RETI ; Force RETI instruction
JNZ LOOP ; loop while BUSY=1
```

```
SUB_RETI: PUSH SR
RETI
```

**FLASH36**

***FLASH Module***

**Category**

Functional

**Function**

Flash content may degrade due to aborted page erases

**Description**

If a page erase is aborted by EEIEX, the flash page containing the last instruction before erase operation will start to degrade. This effect is incremental and, after repetitions, may lead to corrupted flash content.

**Workaround**

- Use the EEI (interrupted erasing) feature instead of EEIEX (abort erasing).

or

- A PSA checksum can be calculated over affected flash page using the marginal read mode (marginal 0). If PSA sum differs from expected PSA value the affected flash page has to be reprogrammed.

or

- Start flash erasing from RAM and limit system frequency to <1MHz (to ensure 6-us delay

after EEIEX). If the last instruction before erasing is located in RAM, flash cell degradation does not occur.

**PORT10*****PORT Module*****Category**

Functional

**Function**

Pull-up/down resistor selection when module pin function is selected

**Description**

When the pull-up/down resistor for a certain port pin is enabled (PxREN.y=1) and the module port pin function is selected (PxSEL.y=1), the pull-up/down resistor configuration of this pin is controlled by the respective module output signal (Module X OUT) instead of the port output register (PxOUT.y).

**Workaround**

None. Do not set PxSEL.y and PxREN.y at the same time.

**SYS15*****SYS Module*****Category**

Functional

**Function**

LPM3 and LPM4 currents exceed specified limits

**Description**

LPM3 and LPM4 currents may exceed specified limits if the SMCLK source is switched from DCO to VLO or LFXT1 just before the instruction to enter LPM3 or LPM4 mode.

**Workaround**

After clock switching, a delay of at least four new clock cycles (VLO or LFXT1) must be implemented to complete the clock synchronization before going into LPM3 or LPM4.

**TA12*****TA Module*****Category**

Functional

**Function**

Interrupt is lost (slow ACLK)

**Description**

Timer\_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer\_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer\_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

**Workaround**

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

**TA16*****TA Module*****Category**

Functional

**Function**

First increment of TAR erroneous when IDx &gt; 00

**Description**

The first increment of TAR after any timer clear event (POR/TACLK) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

**Workaround**

None

<b>TA21</b>	<b>TA Module</b>
<b>Category</b>	Functional
<b>Function</b>	TAIFG Flag is erroneously set after Timer A restarts in Up Mode
<b>Description</b>	In Up Mode, the TAIFG flag should only be set when the timer counts from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLRL bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.
	<p>The diagram shows four signals over time: Timer Clock, Timer counter, Set TAIFG, and Set TACCR0 CCIFG. The timer counter starts at CCR0-1, reaches CCR0, and then counts down to 0h. It is then restarted to 1h and counts down to CCR0-1, then CCR0, and finally 0h. The Set TAIFG signal is set at the rising edge of the timer clock when the counter reaches 0h. The Set TACCR0 CCIFG signal is set at the rising edge of the timer clock when the counter reaches CCR0. Red arrows indicate the timer being stopped at CCR0 and restarted at 1h. A red arrow points to the Set TAIFG signal, labeled 'fault TAIFG'.</p>

<b>Workaround</b>	None.
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<b>TAB22</b>	<b>TAB Module</b>
<b>Category</b>	Functional
<b>Function</b>	Timer_A/Timer_B register modification after Watchdog Timer PUC
<b>Description</b>	Unwanted modification of the Timer_A/Timer_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer_A/Timer_B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/Timer_B does not need to be running).
<b>Workaround</b>	Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
or
MOV.W #VAL, &TBCTL
```

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

<b>TB2</b>	<b>TB Module</b>
<b>Category</b>	Functional
<b>Function</b>	Interrupt is lost (slow ACLK)
<b>Description</b>	Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx). Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should

happen at once with the next Timer\_B counter increment (if  $TBR = CCRx + 1$ ). This interrupt is lost.

**Workaround** Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

## TB16 *TB Module*

**Category** Functional

**Function** First increment of TBR erroneous when  $IDx > 00$

**Description** The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.

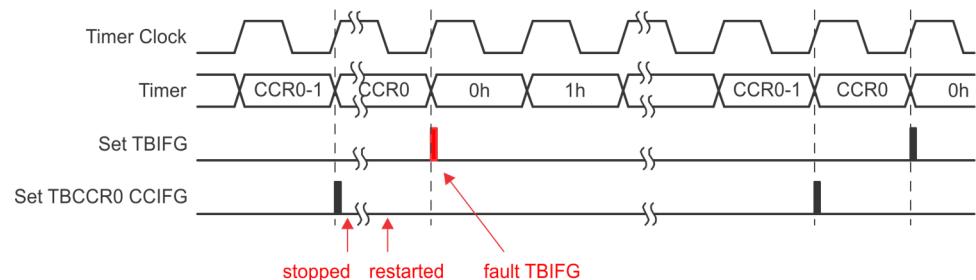
**Workaround** None

## TB24 *TB Module*

**Category** Functional

**Function** TBIFG Flag is erroneously set after Timer B restarts in Up Mode

**Description** In Up Mode, the TBIFG flag should only be set when the timer resets from TBCCR0 to zero. However, if the Timer B is stopped at  $TBR = TBCCR0$ , then cleared ( $TBR=0$ ) by setting the TBCLR bit, and finally restarted in Up Mode, the next rising edge of the TBCLK will erroneously set the TBIFG flag.



**Workaround** None.

## USCI20 *USCI Module*

**Category** Functional

**Function** I2C Mode Multi-master transmitter issue

**Description** When configured for I2C master-transmitter mode, and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following four conditions are true:

- 1 - Two masters are generating SCL
- And
- 2 - The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA
- And
- 3 - The slave drives ACK on SDA after the USCI has already released SCL, and then the

SCL bus line gets released  
 And  
 4 - The transmit buffer has not been loaded before the other master continues communication by driving SCL low

The USCI will remain in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI will interfere with the current bus activity and may cause unpredictable bus behavior.

- Workaround**
- 1 - Ensure that slave doesn't stretch the SCL low phase of an ACK period
  - Or
  - 2 - Ensure that the transmit buffer is loaded in time
  - Or
  - 3 - Do not use the multi-master transmitter mode

**USCI21** *USCI Module*

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**Category** Functional

**Function** UART IrDA receive filter

**Description** The IrDA receive filter can be used to filter pulses with length UCAIRRXFL configured in UCAXIRRCTL register. If UCIRRxFE is set the IrDA receive decoder may filter out pulses longer than the configured filter length depending on frequency of BRCLK. This is resulting in framing errors or corrupted data on the receiver side.

**Workaround** Depending on the used baud rate and the configured filter length a maximum frequency for BRCLK needs to be set to avoid this issue:

For baud rates equal and higher than 115.000 the maximum allowed BRCLK frequency is equal to the max specified system frequency.

$$\text{Max BRCLK} = \frac{\text{Filter Length} + 64}{2} \times \frac{\text{Baud Rate} \times 16}{3 \times 10^6}$$

Baud Rate	Filter Length UCIRRXFL (dec)	Max BRCLK (MHz)
9600	64	3.28
	32	2.46
	16	2.05
	8	1.84
	4	1.74
	2	1.69
	1	1.66
	0	1.64
19200	64	6.55
	32	4.92
	16	4.1
	8	3.69
	4	3.48
	2	3.38
	1	3.33
0	3.28	
38400	64	13.11
	32	9.83
	16	8.19
	8	7.37
	4	6.96
	2	6.76
	1	6.66
	0	6.55
56000	64	19.11
	32	14.34
	16	11.95
	8	10.75
	4	10.15
	2	9.86
	1	9.71
	0	9.56

**USCI22*****USCI Module*****Category**

Functional

**Function**

I2C Master Receiver with 10-bit slave addressing

**Description**

Unexpected behavior of the USCI\_B can occur when configured in I2C master receive mode with 10-bit slave addressing under the following conditions:

- 1) The USCI sends first byte of slave address, the slave sends an ACK and when second address byte is sent, the slave sends a NACK.
- 2) Master sends a repeat start condition (If UCTXSTT=1).
- 3) The first address byte following the repeated start is acknowledged.

However, the second address byte is not sent, instead the Master incorrectly starts to receive data and sets UCBxRXIFG=1.

**Workaround**

Do not use repeated start condition instead set the stop condition UCTXSTP=1 in the NACK ISR prior to the following start condition (USTXSTT=1).

**USCI23*****USCI Module*****Category**

Functional

**Function**

UART transmit mode with automatic baud rate detection

<b>Description</b>	Erroneous behavior of the USCI_A can occur when configured in UART transmit mode with automatic baud rate detection. During transmission if a "Transmit break" is initiated (UCTXBRK=1), the USCI_A will not deliver a stop bit of logic high, instead, it will send a logic low during the subsequent synch period.
<b>Workaround</b>	1) Follow User's Guide instructions for transmitting a break/synch field following UCSWRST=1. Or, 2) Set UCTXBRK=1 before an active transmission, i.e. check for bit UCBUSY=0 and then set UCTXBRK=1.

**USCI24** *USCI Module*

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<b>Category</b>	Functional
<b>Function</b>	Incorrect baud rate information during UART automatic baud rate detection mode
<b>Description</b>	Erroneous behavior of the USCI_A can occur when configured in UART mode with automatic baud rate detection. After automatic baud rate measurement is complete, the UART updates UCAXBR0 and UCAXBR1. Under Oversampling mode (UCOS16=1), for baud rates that should result in UCAXBRx=0x0002, the UART incorrectly reports it as UCAXBRx=0x5555.
<b>Workaround</b>	When break/synch is detected following the automatic baud rate detection, the flag UCBRK flag is set to 1. Check if UCAXBRx=0x5555 and correct it to 0x0002.

**USCI25** *USCI Module*

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<b>Category</b>	Functional
<b>Function</b>	TXIFG is not reset when NACK is received in I2C mode
<b>Description</b>	When the USCI_B module is configured as an I2C master transmitter the TXIFG is not reset after a NACK is received if the master is configured to send a restart (UCTXSTT=1 & UCTXSTP=0).
<b>Workaround</b>	Reset TXIFG in software within the NACKIFG interrupt service routine

**USCI26** *USCI Module*

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<b>Category</b>	Functional
<b>Function</b>	Tbuf parameter violation in I2C multi-master mode
<b>Description</b>	In multi-master I2C systems the timing parameter Tbuf (bus free time between a stop condition and the following start) is not guaranteed to match the I2C specification of 4.7us in standard mode and 1.3us in fast mode. If the UCTXSTT bit is set during a running I2C transaction, the USCI module waits and issues the start condition on bus release causing the violation to occur. Note: It is recommended to check if UCBBUSY bit is cleared before setting UCTXSTT=1.
<b>Workaround</b>	None

**USCI27** *USCI Module*

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<b>Category</b>	Functional
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<b>Function</b>	Timing of USCI I2C interrupts may cause device reset due to automatic clear of an IFG.
<b>Description</b>	<p>When certain USCI I2C interrupt flags (IFG) are set and an automatic flag-clearing event on the I2C bus occurs, the program counter may become corrupted. This will only happen when the IFG is cleared within a critical time window (~6 CPU clock cycles) after a USCI interrupt request occurs and before the interrupt servicing is initiated. The affected interrupts are UCBxTXIFG, UCSTPIFG, UCSTTIFG and UCNACKIFG.</p> <p>The automatic flag-clearing scenarios are described in the following situations:</p> <p>(1) A pending UCBxTXIFG interrupt request is cleared on the falling SCL clock edge following a NACK.</p> <p>(2) A pending UCSTPIFG, UCSTTIFG, or UCNACKIFG interrupt request is cleared by a following Start condition.</p>
<b>Workaround</b>	<p>(1) Polling the affected flags instead of enabling the interrupts.</p> <p>or</p> <p>(2) Ensuring the above mentioned flag-clearing events occur after a time delay of 6 CPU clock cycles has elapsed since the interrupt request occurred and was accepted.</p>

<b>USCI30</b>	<b><i>USCI Module</i></b>
<b>Category</b>	Functional
<b>Function</b>	I2C mode master receiver / slave receiver
<b>Description</b>	<p>When the USCI I2C module is configured as a receiver (master or slave), it performs a double-buffered receive operation. In a transaction of two bytes, once the first byte is moved from the receive shift register to the receive buffer the byte is acknowledged and the state machine allows the reception of the next byte.</p> <p>If the receive buffer has not been cleared of its contents by reading the UCBxRXBUF register while the 7th bit of the following data byte is being received, an error condition may occur on the I2C bus. Depending on the USCI configuration the following may occur:</p> <p>1) If the USCI is configured as an I2C master receiver, an unintentional repeated start condition can be triggered or the master switches into an idle state (I2C communication aborted). The reception of the current data byte is not successful in this case.</p> <p>2) If the USCI is configured as I2C slave receiver, the slave can switch to an idle state stalling I2C communication. The reception of the current data byte is not successful in this case. The USCI I2C state machine will notify the master of the aborted reception with a NACK.</p> <p>Note that the error condition described above occurs only within a limited window of the 7th bit of the current byte being received. If the receive buffer is read outside of this window (before or after), then the error condition will not occur.</p>
<b>Workaround</b>	<p>a) The error condition can be avoided altogether by servicing the UCBxRXIFG in a timely manner. This can be done by (a) servicing the interrupt and ensuring UCBxRXBUF is read promptly or (b) Using the DMA to automatically read bytes from receive buffer upon UCBxRXIFG being set.</p> <p>OR</p> <p>b) In case the receive buffer cannot be read out in time, test the I2C clock line before the UCBxRXBUF is read out to ensure that the critical window has elapsed. This is done by checking if the clock line low status indicator bit UCSCLLOW is set for atleast three USCI bit clock cycles i.e. <math>3 \times t(\text{BitClock})</math>.</p>



Note that the last byte of the transaction must be read directly from UCBxRXBUF. For all other bytes follow the workaround:

Code flow for workaround

- (1) Enter RX ISR for reading receiving bytes
- (2) Check if UCSCLLLOW.UCBxSTAT == 1
- (3) If no, repeat step 2 until set
- (4) If yes, repeat step 2 for a time period  $> 3 \times t$  (BitClock) where  $t$  (BitClock) =  $1/f$  (BitClock)
- (5) If window of  $3 \times t$  (BitClock) cycles has elapsed, it is safe to read UCBxRXBUF

## USCI34

### *USCI Module*

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#### Category

Functional

#### Function

I2C multi-master transmit may lose first few bytes.

#### Description

In an I2C multi-master system (UCMM =1), under the following conditions:

(1)the master is configured as a transmitter (UCTR =1)

AND

(2)the start bit is set (UCTXSTT =1);

if the I2C bus is unavailable, then the USCI module enters an idle state where it waits and checks for bus release. While in the idle state it is possible that the USCI master updates its TXIFG based on clock line activity due to other master/slave communication on the bus. The data byte(s) loaded in TXBUF while in idle state are lost and transmit pointers initialized by the user in the transmit ISR are updated incorrectly.

#### Workaround

Verify that the START condition has been sent (UCTXSTT =0) before loading TXBUF with data.

Example:

```
#pragma vector = USCIAB0TX_VECTOR
__interrupt void USCIAB0TX_ISR(void)
{
// Workaround for USCI34
if(UCB0CTL1&UCTXSTT)
{
// TXData = pointer to the transmit buffer start
// PTxData = pointer to transmit in the ISR
PTxData = TXData; // restore the transmit buffer pointer if the Start bit is set
}
//
if(IFG2&UCB0TXIFG)
{
if (PTxData <= PTxDataEnd) // Check TX byte counter
{
UCB0TXBUF = *PTxData++; // Load TX buffer
}
else
{
UCB0CTL1 |= UCTXSTP; // I2C stop condition
```

```

IFG2 &= ~UCB0TXIFG; // Clear USCI_B0 TX int flag
__bic_SR_register_on_exit(CPUOFF); // Exit LPM0
}
}
}

```

**USCI35*****USCI Module*****Category**

Functional

**Function**

Violation of setup and hold times for (repeated) start in I2C master mode

**Description**

In I2C master mode, the setup and hold times for a (repeated) START,  $t_{SU,STA}$  and  $t_{HD,STA}$  respectively, can be violated if SCL clock frequency is greater than 50kHz in standard mode (100kbps). As a result, a slave can receive incorrect data or the I2C bus can be stalled due to clock stretching by the slave.

**Workaround**

If using repeated start, ensure SCL clock frequencies is < 50kHz in I2C standard mode (100 kbps).

**USCI40*****USCI Module*****Category**

Functional

**Function**

SPI Slave Transmit with clock phase select = 1

**Description**

In SPI slave mode with clock phase select set to 1 (UCAxCTLW0.UCCKPH=1), after the first TX byte, all following bytes are shifted by one bit with shift direction dependent on UCMSB. This is due to the internal shift register getting pre-loaded asynchronously when writing to the USCIA TXBUF register. TX data in the internal buffer is shifted by one bit after the RX data is received.

**Workaround**

Reinitialize TXBUF before using SPI and after each transmission.  
If transmit data needs to be repeated with the next transmission, then write back previously read value:

```
UCAxTXBUF = UCAxTXBUF;
```

**XOSC5*****XOSC Module*****Category**

Functional

**Function**

LF crystal failures may not be properly detected by the oscillator fault circuitry

**Description**

The oscillator fault error detection of the LFXT1 oscillator in low frequency mode (XTS = 0) may not work reliably causing a failing crystal to go undetected by the CPU, i.e. OFIFG will not be set.

**Workaround**

None

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from October 9, 2019 to May 11, 2021

**Page**

- Changed the document format and structure; updated the numbering format for tables, figures, and cross references throughout the document.....6

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