

Ultra Low Power Stereo Audio Codec With miniDSP, DirectPath Headphone, and Class-D Speaker Amplifier

Check for Samples: [TLV320AIC3263](#)

FEATURES

- Stereo Audio DAC with 101dB SNR
- 2.7mW Stereo 48kHz DAC Playback
- Stereo Audio ADC with 93dB SNR
- 6.1mW Stereo 48kHz ADC Record
- 8-192kHz Playback and Record
- 30mW DirectPath™ Headphone Driver Eliminates Large Output DC-Blocking Capacitors
- 128mW Differential Receiver Output Driver
- Class-D Speaker Driver
 - 1.7 W (8Ω , 5.5V, 10% THDN)
 - 1.4 W (8Ω , 5.5V, 1% THDN)
- Stereo Line Outputs
- PowerTune™ - Adjusts Power versus SNR
- Extensive Signal Processing Options
- Eight Single-Ended or 4 Fully-Differential Analog Inputs
- Analog Microphone Inputs, and Up to 4 Simultaneous Digital Microphone Channels
- Low Power Analog Bypass Mode
- Fully-programmable Enhanced miniDSP with PurePath™ Studio Support
 - Extensive Algorithm Support for Voice and Audio Applications
- Three Independent Digital Audio Serial Interfaces with Separate I/O Power Voltages
 - TDM and mono PCM support on all Audio Serial Interfaces
 - 8-channel Input and Output on Audio Serial Interface 1
- Programmable PLL, plus Low-Frequency Clocking
- Programmable 12-Bit SAR ADC
- SPI and I²C Control Interfaces
- 4.81 mm x 4.81 mm x 0.625 mm 81-Ball WCSP (DSBGA) Package

APPLICATIONS

- Mobile Handsets
- Tablets, eBooks
- Portable Navigation Devices (PND)
- Portable Media Player (PMP)
- Portable Gaming Systems
- Portable Computing
- Active Noise Cancellation (ANC)
- Speaker Protection
- Advanced DSP algorithms



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DESCRIPTION

The TLV320AIC3263 (also referred to as the AIC3263) is a flexible, highly-integrated, low-power, low-voltage stereo audio codec. The AIC3263 features four digital microphone inputs, plus programmable outputs, PowerTune capabilities, enhanced fully-programmable miniDSP, predefined and parameterizable signal processing blocks, integrated PLL, and flexible digital audio interfaces. Extensive register-based control of power, input and output channel configuration, gains, effects, pin-multiplexing and clocks are included, allowing the device to be precisely targeted to its application.

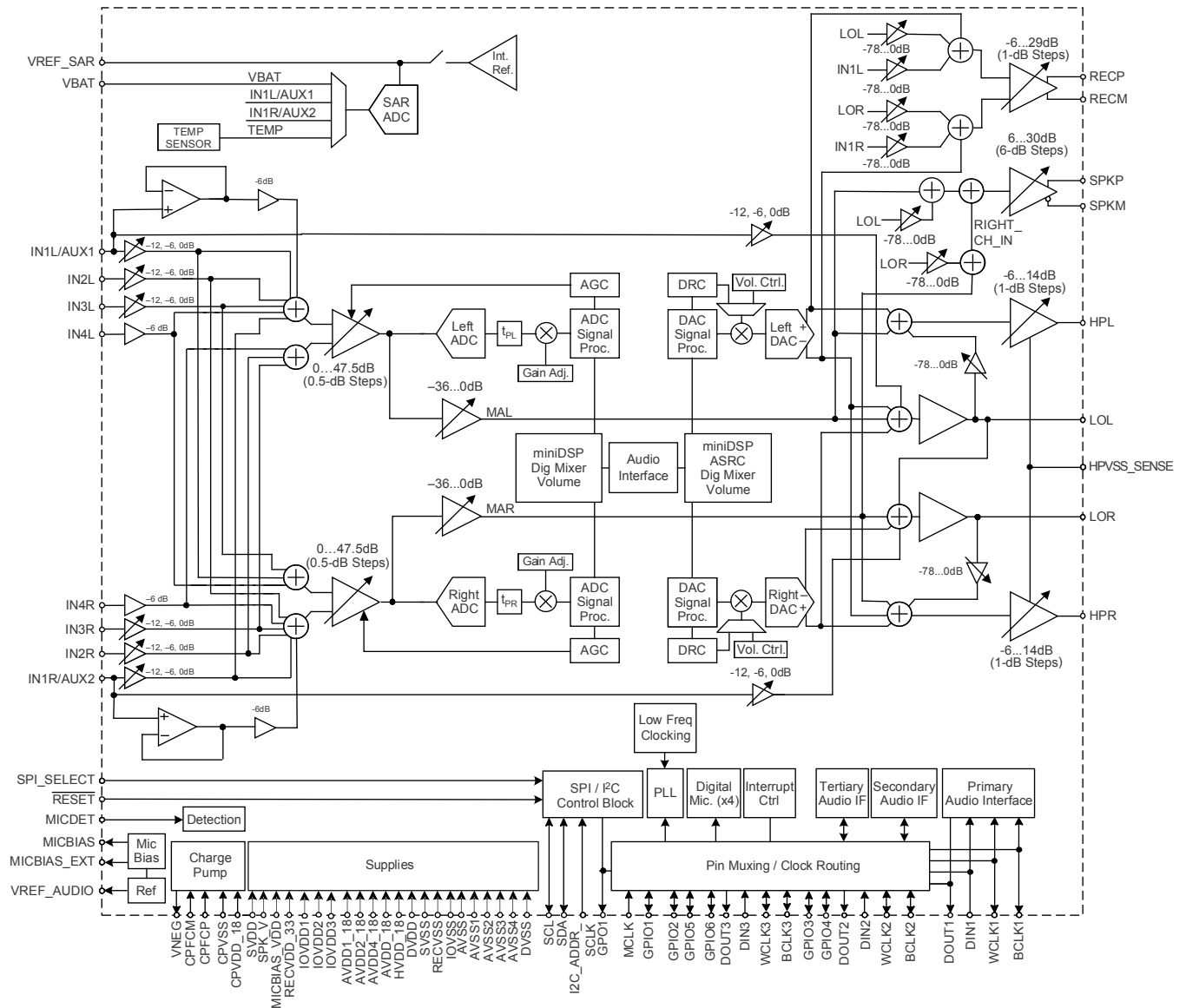


Figure 1. Simplified Block Diagram



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The TLV320AIC3263 features two fully-programmable miniDSP cores that support application-specific algorithms in the record and/or the playback path of the device. The miniDSP cores are fully software programmable. Targeted miniDSP algorithms, such as active noise cancellation, acoustic echo cancellation or advanced DSP filtering are loaded into the device after power-up.

Combined with the advanced PowerTune technology, the device can execute operations from 8kHz mono voice playback to stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC3263 covers operations from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations which cover single-ended and differential setups, as well as floating or mixing input signals. It also provides a digitally-controlled stereo microphone preamplifier and integrated microphone bias. One application of the digital signal processing blocks is removable of audible noise that may be introduced by mechanical coupling, such as optical zooming in a digital camera. The record path can also be configured for up to two stereo (such as up to 4) simultaneous digital microphone Pulse Density Modulation (PDM) interfaces typically used at 64Fs or 128Fs.

The playback path offers signal processing blocks for filtering and effects; headphone, line, receiver, and Class-D speaker output; flexible mixing of DAC; and analog input signals as well as programmable volume controls. The playback path contains two high-power DirectPath™ headphone output drivers which eliminate the need for ac coupling capacitors. A built in charge pump generates the negative supply for the ground centered headphone drivers. These headphone output drivers can be configured in multiple ways, including stereo, and mono BTL. In addition, playback audio can be routed to an integrated Class-D speaker driver or a differential receiver amplifier.

The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern while lowest possible noise is important. With PowerTune the TLV320AIC3263 can address both cases.

The required internal clock of the TLV320AIC3263 can be derived from multiple sources, including the MCLK pin, the BCLK1 pin, the BCLK2 pin, several general purpose I/O pins or the output of the internal PLL, where the input to the PLL again can be derived from similar pins. Although using the internal fractional PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz. To enable even lower clock frequencies, an integrated low-frequency clock multiplier can also be used as an input to the PLL.

The TLV320AIC3263 has a 12-bit SAR ADC converter that supports system voltage measurements. These system voltage measurements can be sourced from three dedicated analog inputs (IN1L/AUX1, IN1R/AUX2, or VBAT pins), or, alternatively, an on-chip temperature sensor that can be read by the SAR ADC.

The device also features three full Digital Audio Serial Interfaces, each supporting I2S, DSP/TDM, RJF, LJF, and mono PCM formats. This enables three simultaneous digital playback and record paths to three independent digital audio buses or chips. Additionally, the general purpose interrupt pins can be used to connect to a fourth digital audio bus, allowing the end system to easily switch in this fourth audio bus to one of the three Digital Audio Serial Interfaces. Each of the three Digital Audio Serial Interfaces can be run using separate power voltages to enable easy integration with separate chips with different I/O voltages.

The device is available in the 4.81 mm x 4.81 mm x 0.625 mm 81-Ball WCSP (DSBGA) Package.

Package and Signal Descriptions

Packaging/Ordering Information

| PRODUCT ⁽¹⁾ | PACKAGE | PACKAGE DESIGNATOR | OPERATING TEMPERATURE RANGE | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|------------------------|-----------------|--------------------|-----------------------------|----------------------|---------------------------|
| TLV320AIC3263 | WCSP-81 (DSBGA) | YZF | -40°C to 85°C | TLV320AIC3263 I YZFT | Tape and Reel, 250 |
| | | | | TLV320AIC3263 I YZFR | Tape and Reel, 3000 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

Pin Assignments

**WCSP Package
(Top View)**

| | | | | | | | | | | |
|---|--------|-------|----------|-------------|---------------|-----------|-------------|----------|-------------|---|
| J | DVDD | WCLK2 | WCLK3 | BCLK3 | SDA | IOVSS | DVDD | WCLK1 | DIN1 | |
| H | IOVDD2 | DIN2 | DIN3 | IOVDD3 | GPIO5 | SCL | IOVDD1 | DOUT1 | BCLK1 | |
| G | BCLK2 | IOVSS | DOUT3 | GPO1 | GPIO6 | RESET | GPIO2 | GPIO1 | MCLK | |
| F | DVSS | GPIO4 | GPIO3 | SPI_SELECT | I2C_ADDR_SCLK | DVSS | AVDD_18 | IN2R | IN2L | |
| E | DVSS | DOUT2 | DVDD | AVSS2 | AVSS3 | AVSS1 | AVSS | IN3L | IN3R | |
| D | DVSS | VBAT | LOR | HPVSS_SENSE | IN4R | IN1R/AUX2 | IN1L/AUX1 | VREF_SAR | VREF_AUDIO | |
| C | SPK_V | SPKM | AVDD4_18 | LOL | AVDD2_18 | MICBIAS | MICBIAS_EXT | AVDD1_18 | IN4L | |
| B | SVSS | SVDD | CPFCP | CPVSS | HPL | HVDD_18 | RECM | RECP | MICDET | |
| A | SPKP | AVSS4 | CPVDD_18 | CPFCM | VNEG | HPR | RECVDD_33 | RECVSS | MICBIAS_VDD | |
| | | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

Figure 2. WCSP-81 (DSBGA) (YZF) Package Ball Assignments, Top View

Table 1. TERMINAL FUNCTIONS – 81 Ball WCSP (YZF) Package

| WCSP (YZF) BALL LOCATION | NAME | I/O/P | POWER DOMAIN | DESCRIPTION |
|--------------------------------|-------------|-------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| A1 | MICBIAS_VDD | P | Analog | Power Supply for Micbias |
| A2 | RECVSS | P | Analog | Receiver Driver Ground |
| A3 | RECVDD_33 | P | Analog | 3.3V Power Supply for Receiver Driver |
| A4 | HPR | O | Analog | Right Headphone Output |
| A5 | VNEG | I/O | Analog | Charge Pump Negative Supply |
| A6 | CPFCM | I/O | Analog | Charge Pump Flying Capacitor M terminal |
| A7 | CPVDD_18 | P | Analog | Power Supply Input for Charge Pump |
| A8 | AVSS4 | P | Analog | Analog Ground for Class-D |
| A9 | SPKP | O | Speaker | Left Channel P side Class-D Output |
| B1 | MICDET | I/O | Analog | Headset Detection Pin |
| B2 | RECP | O | Analog | Receiver Driver P side Output |
| B3 | RECM | O | Analog | Receiver Driver M side Output |
| B4 | HVDD_18 | P | Analog | Headphone Amp Power Supply |
| B5 | HPL | O | Analog | Left Headphone Output |
| B6 | CPVSS | P | Analog | Charge Pump Ground |
| B7 | CPFCP | I/O | Analog | Charge Pump Flying Capacitor P Terminal |
| B8 | SVDD | P | Speaker | Class-D Output Stage Power Supply |
| B9 | SVSS | P | Speaker | Class-D Output Stage Ground |
| C1 | IN4L | I | Analog | Analog Input 4 Left |
| C2 | AVDD1_18 | P | Analog | 1.8V Analog Power Supply |
| C3 | MICBIAS_EXT | O | Analog | Output Bias Voltage for Headset Microphone. |
| C4 | MICBIAS | O | Analog | Output Bias Voltage for Microphone to be used for on-board Microphones |
| C5 | AVDD2_18 | P | Analog | 1.8V Analog Power Supply |
| C6 | LOL | O | Analog | Left Line Output |
| C7 | AVDD4_18 | P | Analog | 1.8V Analog Power Supply for Class-D |
| C8 | SPKM | O | Speaker | M side Class-D Output |
| C9 | SPK_V | P | Speaker | Class-D Output Stage Power Supply (Connect to SVDD through a Resistor) |
| D1 | VREF_AUDIO | O | Analog | Analog Reference Filter Output |
| D2 | VREF_SAR | I/O | Analog | SAR ADC Voltage Reference Input or Internal SAR ADC Voltage Reference Bypass Capacitor Pin |
| D3 | IN1L/AUX1 | I | Analog | Analog Input 1 Left, Auxiliary 1 Input to SAR ADC (Special Function: Left Channel High Impedance Input for Capacitive Sensor Measurement) |
| D4 | IN1R/AUX2 | I | Analog | Analog Input 1 Right, Auxiliary 2 Input to SAR ADC (Special Function: Right Channel High Impedance Input for Capacitive Sensor Measurement) |
| D5 | IN4R | I | Analog | Analog Input 4 Right |
| D6 | HPVSS_SENSE | I | Analog | Headphone Ground Sense Terminal |
| D7 | LOR | O | Analog | Right Line Output |
| D8 | VBAT | I | Speaker | Battery Monitor Voltage Input |
| D9 | DVSS | P | Digital | Digital Ground |
| E1 | IN3R | I | Analog | Analog Input 3 Right |
| E2 | IN3L | I | Analog | Analog Input 3 Left |
| E3 | AVSS | P | Analog | Analog Ground |
| E4 | AVSS1 | P | Analog | Analog Ground |
| E5 | AVSS3 | P | Analog | Analog Ground |
| E6 | AVSS2 | P | Analog | Analog Ground |
| E7 | DVDD | P | Digital | 1.8V Digital Power Supply |

Table 1. TERMINAL FUNCTIONS – 81 Ball WCSP (YZF) Package (continued)

| WCSP (YZF) BALL LOCATION | NAME | I/O/P | POWER DOMAIN | DESCRIPTION |
|--------------------------------|---------------|-------|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| E8 | DOUT2 | O | IOVDD2 | Primary: Audio Serial Data Bus 2 Data Output Secondary: See Table 8 |
| E9 | DVSS | P | Digital | Digital Ground |
| F1 | IN2L | I | Analog | Analog Input 2 Left |
| F2 | IN2R | I | Analog | Analog Input 2 Right |
| F3 | AVDD_18 | P | Analog | 1.8V Analog Power Supply |
| F4 | DVSS | P | Digital | Digital Ground |
| F5 | I2C_ADDR_SCLK | I | IOVDD1 | Primary: (SPI_SELECT = 1) SPI Serial Clock Secondary: (SPI_SELECT = 0) I ² C Address Bit (I2C_ADDR) |
| F6 | SPI_SELECT | I | IOVDD1 | Control Interface Select SPI_SELECT = '1': SPI Interface selected SPI_SELECT = '0': I ² C Interface selected |
| F7 | GPIO3 | I/O | IOVDD2 | Multi Function Digital IO 3 See Table 9 |
| F8 | GPIO4 | I/O | IOVDD2 | Multi Function Digital IO 4 See Table 9 |
| F9 | DVSS | P | Digital | Digital Ground |
| G1 | MCLK | I | IOVDD1 | Master Clock Input |
| G2 | GPIO1 | I/O | IOVDD1 | Multi Function Digital IO 1 See Table 9 |
| G3 | GPIO2 | I/O | IOVDD1 | Multi Function Digital IO 2 See Table 9 |
| G4 | RESET | I | IOVDD1 | Active Low Reset |
| G5 | GPIO6 | I/O | IOVDD1 | Multi Function Digital IO 6 See Table 9 |
| G6 | GPO1 | O | IOVDD1 | Multifunction Digital Output 1 Primary: (SPI_SELECT = 1) Serial Data Output Secondary: (SPI_SELECT = 0) See Table 9 |
| G7 | DOUT3 | O | IOVDD3 | Primary: Audio Serial Data Bus 3 Data Output Secondary: See Table 9 |
| G8 | IOVSS | P | Common for all IO Domains | Digital I/O Buffer Ground |
| G9 | BCLK2 | I/O | IOVDD2 | Primary: Audio Serial Data Bus 2 Bit Clock Secondary: See Table 8 |

Table 1. TERMINAL FUNCTIONS – 81 Ball WCSP (YZF) Package (continued)

| WCSP (YZF) BALL LOCATION | NAME | I/O/P | POWER DOMAIN | DESCRIPTION |
|--------------------------------|--------|-------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| H1 | BCLK1 | I/O | IOVDD1 | Primary: Audio Serial Data Bus 1 Bit Clock Secondary: See Table 8 |
| H2 | DOUT1 | O | IOVDD1 | Primary: Audio Serial Data Bus 1 Data Output Secondary: See Table 8 |
| H3 | IOVDD1 | P | IOVDD1 | Digital I/O Buffer Supply 1 |
| H4 | SCL | I/O | IOVDD1 | I ² C Interface Serial Clock (SPI_SELECT = 0) SPI interface mode chip-select signal (SPI_SELECT = 1) |
| H5 | GPIO5 | I/O | IOVDD1 | Multifunction Digital IO 5 See Table 8 |
| H6 | IOVDD3 | P | IOVDD3 | Digital I/O Buffer Supply 3 |
| H7 | DIN3 | I | IOVDD3 | Primary: Audio Serial Data Bus 3 Data Input Secondary: See Table 9 |
| H8 | DIN2 | I | IOVDD2 | Primary: Audio Serial Data Bus 2 Data Input Secondary: See Table 8 |
| H9 | IOVDD2 | P | IOVDD2 | Digital I/O Buffer Supply 2 |
| J1 | DIN1 | I | IOVDD1 | Primary: Audio Serial Data Bus 1 Data Input Secondary: See Table 8 |
| J2 | WCLK1 | I/O | IOVDD1 | Primary: Audio Serial Data Bus 1 Word Clock Secondary: See Table 8 |
| J3 | DVDD | P | Digital | 1.8V Digital Power Supply |
| J4 | IOVSS | P | Common for all IO Domains | Digital I/O Buffer Ground |
| J5 | SDA | I/O | IOVDD1 | I ² C interface mode serial data input (SPI_SELECT = 0) SPI interface mode serial data input (SPI_SELECT = 1) |
| J6 | BCLK3 | I/O | IOVDD3 | Primary: Audio Serial Data Bus 3 Bit Clock Secondary: See Table 9 |
| J7 | WCLK3 | I/O | IOVDD3 | Primary: Audio Serial Data Bus 3 Word Clock Secondary: See Table 9 |

Table 1. TERMINAL FUNCTIONS – 81 Ball WCSP (YZF) Package (continued)

| WCSP (YZF) BALL LOCATION | NAME | I/O/P | POWER DOMAIN | DESCRIPTION |
|--------------------------------|-------|-------|-----------------|---------------------------------------------------------------------------------------------|
| J8 | WCLK2 | I/O | IOVDD2 | Primary: Audio Serial Data Bus 2 Word Clock Secondary: See Table 8 |
| J9 | DVDD | P | Digital | 1.8V Digital Power Supply |

Electrical Characteristics

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | VALUE | UNIT | |
|------------------------------------------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------|------|
| AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18 to AVSS1, AVSS2, AVSS4, AVSS respectively ⁽²⁾ | –0.3 to 2.2 | V | |
| RECVDD_33 to RECVSS | –0.3 to 3.9 | V | |
| DVDD to DVSS | –0.3 to 2.2 | V | |
| IOVDDx to IOVSS | –0.3 to 3.9 | V | |
| HVDD_18 to AVSS | –0.3 to 2.2 | V | |
| CPVDD_18 to CPVSS | –0.3 to 2.2 | V | |
| SVDD to SVSS, SPK_V to SVSS, and MICBIAS_VDD to AVSS3 ⁽³⁾ | –0.3 to 6.0 | V | |
| Digital Input voltage to ground | IOVSS – 0.3 to IOVDDx + 0.3 | V | |
| Analog input voltage to ground | AVSS – 0.3 to AVDDx_18 + 0.3 | V | |
| VBAT | –0.3 to 6 | V | |
| Operating temperature range | –40 to 85 | °C | |
| Storage temperature range | –55 to 125 | °C | |
| Junction temperature (T _J Max) | 105 | °C | |
| WCSP-81 (DSBGA) package (YZF) | Power dissipation | (T _J Max – TA) / θ _{JA} | W |
| | θ _{JA} Junction-to-ambient thermal resistance | 39.1 | °C/W |
| | θ _{JCtop} Junction-to-case (top) thermal resistance | 0.1 | |
| | θ _{JB} Junction-to-board thermal resistance | 12.0 | |
| | Ψ _{JT} Junction-to-top characterization parameter | 0.7 | |
| | Ψ _{JB} Junction-to-board characterization parameter | 11.5 | |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) It's recommended to keep all AVDDx_18 supplies within ± 50 mV of each other.
- (3) It's recommended to keep SVDD and SPK_V supplies within ± 50 mV of each other.

Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---------------------------------------|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|------|------|
| AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18 | Power Supply Voltage Range | Referenced to AVSS1, AVSS2, AVSS4, AVSS respectively ⁽¹⁾ It is recommended to connect each of these supplies to a single supply rail. | 1.5 ⁽²⁾ | 1.8 | 1.95 | V |
| RECVDD_33 | | | 1.65 ⁽³⁾ | 3.3 | 3.6 | |
| IOVDD1, IOVDD2, IOVDD3 | | | 1.1 | | 3.6 | |
| DVDD ⁽⁴⁾ | Power Supply Voltage Range | Referenced to DVSS ⁽¹⁾ | 1.26 | 1.8 | 1.95 | V |
| CPVDD_18 | Power Supply Voltage Range | Referenced to CPVSS ⁽¹⁾ | 1.26 | 1.8 | 1.95 | |
| HVDD_18 | | Referenced to AVSS ⁽¹⁾ | 1.5 ⁽³⁾ | 1.8 | 1.95 | |
| | | Ground-centered Configuration | | | | |
| | | Unipolar Configuration | 1.65 ⁽³⁾ | | 1.95 | |

- (1) All grounds on board are tied together, so they should not differ in voltage by more than 0.1V max, for any combination of ground signals. AVDDx_18 are within +/- 0.05 V of each other. SVDD and SPK_V are within +/- 0.05 V of each other.
- (2) For optimal performance with CM=0.9V, min AVDD = 1.8V.
- (3) Minimum voltage for HVDD_18 should be greater than or equal to AVDD2_18.
- (4) At DVDD values lower than 1.65V, the PLL and SAR ADC do not function. Please see table in SLAU475, *Maximum TLV320AIC3263 Clock Frequencies* for details on maximum clock frequencies.

Recommended Operating Conditions (continued)

| | | | MIN | NOM | MAX | UNIT |
|----------------------|---------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|----------|------|
| SVDD ⁽¹⁾ | Power Supply Voltage Range | Referenced to SVSS ⁽¹⁾ | 2.7 | | 5.5 | V |
| SPK_V ⁽¹⁾ | Power Supply Voltage Range | Referenced to SVSS ⁽¹⁾ | 2.7 | | 5.5 | V |
| MICBIAS_VDD | Power Supply Voltage Range | Referenced to AVSS3 ⁽¹⁾ | 2.7 | | 5.5 | V |
| VREF_SAR | External voltage reference for SAR | Referenced to AVSS | | 1.8 | AVDDx_18 | V |
| | PLL Input Frequency ⁽⁵⁾ | Clock divider uses fractional divide (D > 0), P=1, PLL_CLKIN_DIV=1, DVDD ≥ 1.65V (Refer to table in SLAU475, <i>Maximum TLV320AIC3263 Clock Frequencies</i>) | 10 | | 20 | MHz |
| | | Clock divider uses integer divide (D = 0), P=1, PLL_CLKIN_DIV=1, DVDD ≥ 1.65V (Refer to table in SLAU475, <i>Maximum TLV320AIC3263 Clock Frequencies</i>) | 0.512 | | 20 | MHz |
| MCLK | Master Clock Frequency | MCLK; Master Clock Frequency; IOVDD ≥ 1.65V | | | 50 | MHz |
| | | MCLK; Master Clock Frequency; IOVDD ≥ 1.1V | | | 33 | |
| SCL | SCL Clock Frequency | | | | 400 | kHz |
| LOL, LOR | Stereo line output load resistance | | 0.6 | 10 | | kΩ |
| HPL, HPR | Stereo headphone output load resistance | Single-ended configuration | 14.4 | 16 | | Ω |
| SPKP-SPKM | Speaker output load resistance | Differential | 7.2 | 8 | | Ω |
| RECP-RECM | Receiver output resistance | Differential | 24.4 | 32 | | Ω |
| C _{IN} | Charge pump input capacitor (CPVDD to CPVSS terminals) | | | 10 | | μF |
| C _O | Charge pump output capacitor (VNEG terminal) | Type X7R | | 2.2 | | μF |
| C _F | Charge pump flying capacitor (CPFCP to CPFCM terminals) | Type X7R | | 2.2 | | μF |
| TOPR | Operating Temperature Range | | -40 | | 85 | °C |

(5) The PLL Input Frequency refers to clock frequency after PLL_CLKIN_DIV divider. Frequencies higher than 20MHz can be sent as an input to this PLL_CLKIN_DIV and reduced in frequency prior to input to the PLL.

Electrical Characteristics, SAR ADC

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{\text{ext}} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|-----------------|----------|----------------------------|
| SAR ADC Inputs | | | | | | |
| Analog Input | Input voltage range | IN1L/AUX1 or IN1R/AUX2 Selected | 0 | VREF_SAR | | V |
| | Input impedance | | $1 \div (f \times C_{\text{SAR_IN}})^{(1)}$ | | | k Ω |
| | Input capacitance, $C_{\text{SAR_IN}}$ | | 25 | | | pF |
| | Input leakage current | | 1 | | | μA |
| Battery Input | VBAT Input voltage range | VBAT (Battery measurement) selected ⁽²⁾ | 2.2 | | 5.5 | V |
| | VBAT Input impedance | | 5 | | | k Ω |
| | VBAT Input capacitance | | 25 | | | pF |
| | VBAT Input leakage current | | 1 | | | μA |
| SAR ADC Conversion | | | | | | |
| | Resolution | Programmable: 8-bit, 10-bit, 12-bit | 8 | | 12 | Bits |
| | No missing codes | 12-bit resolution | | 11 | | Bits |
| IN1L/AUX1 | Integral linearity | 12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, External Reference = 1.8V ⁽³⁾ | | ± 1 | | LSB |
| | Offset error | | | ± 1 | | LSB |
| | Gain error | | | -0.09 | | % |
| | Noise | DC voltage applied to IN1L/AUX1 = 1 V, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, External Reference = 1.8V ⁽⁴⁾⁽³⁾ | | ± 1 | | LSB |
| VBAT | Accuracy | 12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, Internal Reference = 1.25V | | 2 | | % |
| | Offset error | | | ± 2 | | LSB |
| | Gain error | | | 1.5 | | % |
| | Noise | DC voltage applied to VBAT = 3.6 V, 12-bit resolution, SAR ADC clock = Internal Oscillator Clock, Conversion clock = Internal Oscillator / 4, Internal Reference = 1.25V | | ± 0.5 | | LSB |
| Conversion Rate | | | | | | |
| | Normal conversion operation | 12-bit resolution, SAR ADC clock = 12 MHz External Clock, Conversion clock = External Clock / 4, External Reference = 1.8V ⁽³⁾ . With Fast SPI reading of data. | | | 119 | kHz |
| | High-speed conversion operation | 8-bit resolution, SAR ADC clock = 12 MHz External Clock, Internal Conversion clock = External Clock (Conversion accuracy is reduced.), External Reference = 1.8V ⁽³⁾ . With Fast SPI reading of data. | | | 250 | kHz |
| Voltage Reference - VREF_SAR | | | | | | |
| Voltage range | Internal VREF_SAR | | | 1.25 \pm 0.05 | | V |
| | External VREF_SAR | | 1.25 | | AVDDx_18 | V |
| Reference Noise | CM=0.9V, $C_{\text{ref}} = 1\mu\text{F}$ | | | 46 | | μV_{RMS} |
| Decoupling Capacitor | | | | 1 | | μF |

(1) SAR input impedance is dependent on the sampling frequency (f designated in Hz), and the sampling capacitor is $C_{\text{SAR_IN}} = 25\text{pF}$.

(2) When VBAT is not being sampled/converted. When VBAT is being sampled, effective input impedance to GND is 5.24k Ω .

(3) When utilizing External SAR reference, this external reference should be restricted $V_{\text{EXT_SAR_REF}} \leq \text{AVDD}_{18}$ and AVDD_{2_18} .

(4) Noise from external reference voltage is excluded from this measurement.

Electrical Characteristics, ADC

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1μF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------------------|
| AUDIO ADC (CM = 0.9V) | | | | | | |
| | Input signal level (0dB) | Single-ended, CM = 0.9V | | 0.5 | | V _{RMS} |
| | Device Setup | 1kHz sine wave input, Single-ended Configuration IN2R to Right ADC and IN2L to Left ADC, R _{in} = 20kΩ, f _s = 48kHz, AOSR = 128, MCLK = 256*f _s , PLL Disabled; AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4 | | | | |
| SNR | Signal-to-noise ratio, A-weighted ⁽¹⁾ (2) | Inputs ac-shorted to ground | 85 | 94 | | dB |
| | | IN1R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and ac-shorted to ground IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and ac-shorted to ground | | 94 | | |
| DR | Dynamic range A-weighted ⁽¹⁾ (2) | −60dB full-scale, 1-kHz input signal | | 94 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | −3 dB full-scale, 1-kHz input signal | | −89 | −75 | dB |
| | | IN1R, IN3R, IN4R each exclusively routed in separate tests to Right ADC IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC −3dB full-scale, 1-kHz input signal | | −88 | | |
| | Gain Error | 1kHz sine wave input at −3dBFS, Single-ended configuration R _{in} = 20K f _s = 48kHz, AOSR=128, MCLK = 256* f _s , PLL Disabled AGC = OFF, Channel Gain=0dB, Processing Block = PRB_R1, Power Tune = PTM_R4, CM=0.9V | | 0.02 | | dB |
| | Input Channel Separation | 1kHz sine wave input at −3dBFS, Single-ended configuration IN1L routed to Left ADC, IN1R routed to Right ADC, R _{in} = 20K AGC = OFF, AOSR = 128, Channel Gain=0dB, CM=0.9V | | 110 | | dB |
| | Input Pin Crosstalk | 1kHz sine wave input at −3dBFS on IN2L, IN2L internally not routed. IN1L routed to Left ADC, ac-coupled to ground 1kHz sine wave input at −3dBFS on IN2R, IN2R internally not routed. IN1R routed to Right ADC, ac-coupled to ground Single-ended configuration R _{in} = 20kΩ, AOSR=128 Channel Gain=0dB, CM=0.9V | | 112 | | dB |
| | PSRR | 217Hz, 100mVpp signal on AVDD_18, AVDDx_18 Single-ended configuration, Rin=20kΩ, Channel Gain=0dB; CM=0.9V | | 59 | | dB |

- (1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
- (2) All performance measurements done with pre-analyzer 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, ADC (continued)

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_s (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{\text{ext}} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| AUDIO ADC (CM = 0.75V) | | | | | | |
| | Input signal level (0dB) | Single-ended, CM=0.75V, AVDD_18, AVDDx_18 = 1.5V | | 0.375 | | V _{RMS} |
| | Device Setup | 1kHz sine wave input, Single-ended Configuration IN2R to Right ADC and IN2L to Left ADC, $R_{\text{in}} = 20\text{K}$, $f_s = 48\text{kHz}$, AOSR = 128, MCLK = $256 \cdot f_s$, PLL Disabled; AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4 | | | | |
| SNR | Signal-to-noise ratio, A-weighted ⁽³⁾ ⁽⁴⁾ | Inputs ac-shortened to ground | | 91 | | dB |
| | | IN1R, IN3R, IN4R each exclusively routed in separate tests to Right ADC and ac-shortened to ground IN1L, IN3L, IN4L each exclusively routed in separate tests to Left ADC and ac-shortened to ground | | 91 | | dB |
| DR | Dynamic range A-weighted ⁽³⁾ ⁽⁴⁾ | −60dB full-scale, 1-kHz input signal | | 92 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | −3dB full-scale, 1-kHz input signal | | −85 | | dB |

- (3) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
- (4) All performance measurements done with pre-analyzer 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, ADC (continued)

T_A = 25°C; AVDD₁₈, AVDDx₁₈, HVDD₁₈, CPVDD₁₈, DVDD, IOVDDx = 1.8V; RECVD₃₃ = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------------------|
| AUDIO ADC (Differential Input, CM = 0.9V) | | | | | |
| Input signal level (0dB) | Differential, CM=0.9V, AVDD ₁₈ , AVDDx ₁₈ = 1.8V | | 1 | | V _{RMS} |
| Device Setup | 1kHz sine wave input, Differential Configuration IN1L, IN1R Routed to Right ADC, IN2L, IN2R Routed to Left ADC R _{in} = 20kΩ, f _s = 48kHz, AOSR=128, MCLK = 256* f _s , PLL Disabled, AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4 | | | | |
| SNR | Signal-to-noise ratio, A-weighted ⁽⁵⁾ ⁽⁶⁾ Inputs ac-shortcd to ground | | 94 | | dB |
| DR | Dynamic range A-weighted ⁽⁵⁾ ⁽⁶⁾ -60dB full-scale, 1-kHz input signal | | 95 | | dB |
| THD+N | Total Harmonic Distortion plus Noise -3dB full-scale, 1-kHz input signal | | -89 | | dB |
| Gain Error | 1kHz sine wave input at -3dBFS, Differential configuration R _{in} = 20kΩ, f _s = 48kHz, AOSR=128, MCLK = 256* f _s , PLL Disabled AGC = OFF, Channel Gain=0dB, Processing Block = PRB_R1, Power Tune = PTM_R4, CM=0.9V | | 0.04 | | dB |
| Input Channel Separation | 1kHz sine wave input at -3dBFS, Differential configuration IN1L/IN1R differential signal routed to Right ADC, IN2L/IN2R differential signal routed to Left ADC, R _{in} = 20kΩ AGC = OFF, AOSR = 128, Channel Gain=0dB, CM=0.9V | | 108 | | dB |
| Input Pin Crosstalk | 1kHz sine wave input at -3dBFS on IN2L/IN2R, IN2L/IN2R internally not routed. IN1L/IN1R differentially routed to Right ADC, ac-coupled to ground 1kHz sine wave input at -3dBFS on IN2L/IN2R, IN2L/IN2R internally not routed. IN3L/IN3R differentially routed to Left ADC, ac-coupled to ground Differential configuration R _{in} = 20kΩ, AOSR=128 Channel Gain=0dB, CM=0.9V | | 110 | | dB |
| PSRR | 217Hz, 100mVpp signal on AVDD ₁₈ , AVDDx ₁₈ Differential configuration, Rin=20K, Channel Gain=0dB; CM=0.9V | | 52 | | dB |
| AUDIO ADC | | | | | |
| ADC programmable gain amplifier gain | IN1 - IN3, Single-Ended, Rin = 10K, PGA gain set to 0dB | | 0 | | dB |
| | IN1 - IN3, Single-Ended, Rin = 10K, PGA gain set to 47.5dB | | 47.5 | | dB |
| | IN1 - IN3, Single-Ended, Rin = 20K, PGA gain set to 0dB | | -6 | | dB |
| | IN1 - IN3, Single-Ended, Rin = 20K, PGA gain set to 47.5dB | | 41.5 | | dB |
| | IN1 - IN3, Single-Ended, Rin = 40K, PGA gain set to 0dB | | -12 | | dB |
| | IN1 - IN3, Single-Ended, Rin = 40K, PGA gain set to 47.5dB | | 35.5 | | dB |
| | IN4, Single-Ended, Rin = 20K, PGA gain set to 0dB | | -6 | | dB |
| | IN4, Single-Ended, Rin = 20K, PGA gain set to 47.5dB | | 41.5 | | dB |
| ADC programmable gain amplifier step size | 1-kHz tone | | 0.5 | | dB |

- (5) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
- (6) All performance measurements done with pre-analyzer 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Bypass Outputs

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{ext} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|----------------------------|
| ANALOG BYPASS TO RECEIVER AMPLIFIER, DIRECT MODE | | | | | |
| Device Setup | Load = 32 Ω (differential), 56pF; Input CM=0.9V; Output CM=1.65V; IN1L routed to RECP and IN1R routed to RECM; Channel Gain=0dB | | | | |
| Full scale differential input voltage (0dB) | | | 1 | | V _{RMS} |
| Gain Error | 707mVrms (-3dBFS), 1-kHz input signal | | -0.7 | | dB |
| Noise, A-weighted ⁽¹⁾ | Idle Channel, IN1L and IN1R ac-shortened to ground | | 12 | | μV_{RMS} |
| THD+N Total Harmonic Distortion plus Noise | 707mVrms (-3dBFS), 1-kHz input signal | | -89 | | dB |
| ANALOG BYPASS TO HEADPHONE AMPLIFIER, PGA MODE | | | | | |
| Device Setup | Load = 16 Ω (single-ended), 56pF; HVDD_18 = 3.3V Input CM=0.9V; Output CM=1.65V IN1L routed to ADCPGA_L, ADCPGA_L routed through MAL to HPL; and IN1R routed to ADCPGA_R, ADCPGA_R routed through MAR to HPR; R _{in} = 20K; Channel Gain = 0dB | | | | |
| Full scale differential input voltage (0dB) | | | 0.5 | | V _{RMS} |
| Gain Error | 446mVrms (-1dBFS), 1-kHz input signal | | -1.1 | | dB |
| Noise, A-weighted ⁽¹⁾ | Idle Channel, IN1L and IN1R ac-shortened to ground | | 6.0 | | μV_{RMS} |
| THD+N Total Harmonic Distortion plus Noise | 446mVrms (-1dBFS), 1-kHz input signal | | -83 | | dB |
| ANALOG BYPASS TO HEADPHONE AMPLIFIER (GROUND-CENTERED CIRCUIT CONFIGURATION), PGA MODE | | | | | |
| Device Setup | Load = 16 Ω (single-ended), 56pF; Input CM=0.9V; IN1L routed to ADCPGA_L, ADCPGA_L routed through MAL to HPL; and IN1R routed to ADCPGA_R, ADCPGA_R routed through MAR to HPR; R _{in} = 20K; Channel Gain = 0dB | | | | |
| Full scale input voltage (0dB) | | | 0.5 | | V _{RMS} |
| Gain Error | 446mVrms (-1dBFS), 1-kHz input signal | | -1.0 | | dB |
| Noise, A-weighted ⁽¹⁾ | Idle Channel, IN1L and IN1R ac-shortened to ground | | 11 | | μV_{RMS} |
| THD+N Total Harmonic Distortion plus Noise | 446mVrms (-1dBFS), 1-kHz input signal | | -71 | | dB |

- (1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Bypass Outputs (continued)

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{\text{ext}} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|----------------------------|
| ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE | | | | | |
| Device Setup | Load = 10KOhm (single-ended), 56pF; Input and Output CM=0.9V; IN1L routed to ADCPGA_L and IN1R routed to ADCPGA_R; Rin = 20k ADCPGA_L routed through MAL to LOL and ADCPGA_R routed through MAR to LOR; Channel Gain = 0dB | | | | |
| Full scale input voltage (0dB) | | | 0.5 | | V _{RMS} |
| Gain Error | 446mVrms (-1dBFS), 1-kHz input signal | | -0.9 | | dB |
| Noise, A-weighted ⁽²⁾ | Idle Channel, IN1L and IN1R ac-shortcd to ground | | 5.9 | | μV_{RMS} |
| | Channel Gain=40dB, Inputs ac-shortcd to ground, Input Referred | | 3.0 | | μV_{RMS} |
| ANALOG BYPASS TO LINE-OUT AMPLIFIER, DIRECT MODE | | | | | |
| Device Setup | Load = 10KOhm (single-ended), 56pF; Input and Output CM=0.9V; IN1L routed to LOL and IN1R routed to LOR; Channel Gain = 0dB | | | | |
| Full scale input voltage (0dB) | | | 0.5 | | V _{RMS} |
| Gain Error | 446mVrms (-1dBFS), 1-kHz input signal | | -0.4 | | dB |
| Noise, A-weighted ⁽²⁾ | Idle Channel, IN1L and IN1R ac-shortcd to ground | | 3.0 | | μV_{RMS} |

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Microphone Interface

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{\text{ext}} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------------------|-----------------------------------------------------------------------------------|-----|-------|-----|----------------------------|
| MICROPHONE BIAS (MICBIAS or MICBIAS_EXT) | | | | | |
| Bias voltage | CM=0.9V, MICBIAS_VDD = 3.3V | | | | |
| | Micbias Mode 0 | | 1.80 | | V |
| | Micbias Mode 1 | | 2.00 | | V |
| | Micbias Mode 2 | | 2.15 | | V |
| | Micbias Mode 3 | | 2.49 | | V |
| | Micbias Mode 4 ⁽¹⁾ | | 2.85 | | V |
| | Micbias Mode 5 ⁽¹⁾ | | 3.00 | | V |
| | CM=0.75V, MICBIAS_VDD = 3.3V | | | | |
| | Micbias Mode 0 | | 1.50 | | V |
| | Micbias Mode 1 | | 1.67 | | V |
| | Micbias Mode 2 | | 1.79 | | V |
| | Micbias Mode 3 | | 2.08 | | V |
| | Micbias Mode 4 | | 2.37 | | V |
| | Micbias Mode 5 | | 2.50 | | V |
| Output Noise | CM=0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA. | | 10.04 | | μV_{RMS} |
| | | | 70.99 | | nV/ $\sqrt{\text{Hz}}$ |
| Current Sourcing | Micbias Mode 0, 1, 2, 3, 4, or 5 (CM=0.9V) | | 8 | | mA |
| Maximum Line Capacitance | Micbias Mode 0, 1, 2, 3, 4, or 5 (CM=0.9V) ⁽²⁾ | | | 10 | pF |
| PSRR | 217Hz, 100mVpp signal on AVDDx_18, DVDD, IOVDDx, MICBIAS_VDD=3.6V, CM=0.75V | | 48 | | dB |
| | 217Hz, 100mVpp signal on MICBIAS_VDD, MICBIAS_VDD=3.6V, CM=0.75V | | 90 | | dB |
| | 1kHz, 100mVpp signal on AVDDx_18, DVDD, IOVDDx, MICBIAS_VDD=3.6V, CM=0.75V | | 47 | | dB |
| | 1kHz, 100mVpp signal on MICBIAS_VDD, MICBIAS_VDD=3.6V | | 85 | | dB |

- (1) With Common Mode voltage of 0.9V, the MICBIAS_VDD voltage must be at minimum 3.05V to utilize Micbias Mode 4, and minimum of 3.2V to utilize Micbias Mode 5.
- (2) An explicit external capacitor should not be placed on MICBIAS or MICBIAS_EXT lines.

Electrical Characteristics, Audio DAC Outputs

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{\text{ext}} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------------------------|------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT | | | | | | |
| Device Setup | | Load = 10 k Ω (single-ended), 56pF Input and Output CM=0.9V DOSR = 128, MCLK=256* f_S , Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P4 | | | | |
| | Full scale output voltage (0dB) | | | 0.5 | | V _{RMS} |
| SNR | Signal-to-noise ratio A-weighted ^{(1) (2)} | All zeros fed to DAC input | 85 | 101 | | dB |
| DR | Dynamic range, A-weighted ^{(1) (2)} | –60dB 1kHz input full-scale signal, Word length=20 bits | | 102 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | –3dB full-scale, 1-kHz input signal | | –92 | –70 | dB |
| | DAC Gain Error | –3dB full-scale, 1-kHz input signal | | 0.1 | | dB |
| | DAC Mute Attenuation | Mute | | 125 | | dB |
| | DAC channel separation | –1 dB, 1kHz signal, between left and right Line out | | 108 | | dB |
| DAC PSRR | | 100mVpp, 1kHz signal applied to AVDD_18, AVDDx_18 | | 81 | | dB |
| | | 100mVpp, 217Hz signal applied to AVDD_18, AVDDx_18 | | 79 | | dB |
| AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT | | | | | | |
| Device Setup | | Load = 10 k Ω (single-ended), 56pF Input and Output CM=0.75V; AVDD_18, AVDDx_18, HVDD_18=1.5V DOSR = 128 MCLK=256* f_S Channel Gain = 0dB Processing Block = PRB_P1 Power Tune = PTM_P4 | | | | |
| | Full scale output voltage (0dB) | | | 0.375 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | All zeros fed to DAC input | | 100 | | dB |
| DR | Dynamic range, A-weighted ^{(1) (2)} | –60dB 1 kHz input full-scale signal, Word length=20 bits | | 99 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | –3 dB full-scale, 1-kHz input signal | | –90 | | dB |

- (1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (2) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Audio DAC Outputs (continued)

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{ext} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| AUDIO DAC – MONO DIFFERENTIAL LINE OUTPUT | | | | | |
| Device Setup | Load = 10 k Ω (differential), 56pF Input and Output CM=0.9V, LOL signal routed to LOR amplifier DOSR = 128, MCLK=256* f_S , Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P4 | | | | |
| Full scale output voltage (0dB) | | | 1 | | V _{RMS} |
| SNR | Signal-to-noise ratio A-weighted ⁽³⁾ ⁽⁴⁾ All zeros fed to DAC input | | 101 | | dB |
| DR | Dynamic range, A-weighted ⁽³⁾ ⁽⁴⁾ –60dB 1kHz input full-scale signal, | | 101 | | dB |
| THD+N | Total Harmonic Distortion plus Noise –3dB full-scale, 1-kHz input signal | | -91 | | dB |
| DAC Gain Error | –3dB full-scale, 1-kHz input signal | | -0.03 | | dB |
| DAC Mute Attenuation | Mute | | 124 | | dB |
| DAC PSRR | 100mVpp, 1kHz signal applied to AVDD_18, AVDDx_18 | | 63 | | dB |
| | 100mVpp, 217Hz signal applied to AVDD_18, AVDDx_18 | | 63 | | dB |

- (3) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (4) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Audio DAC Outputs (continued)

T_A = 25°C; AVDD₁₈, AVDDx₁₈, HVDD₁₈, CPVDD₁₈, DVDD, IOVDDx = 1.8V; RECVDD₃₃ = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------------------|
| AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (GROUND-CENTERED CIRCUIT CONFIGURATION) | | | | | | |
| Device Setup | | Load = 16Ω (single-ended), 56pF, Input CM=0.9V; DOSR = 128, MCLK=256* f _S , Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P3, Headphone Output Strength=100% | | | | |
| Output 1 | Output voltage | | | 0.5 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ⁽⁵⁾ ₍₆₎ | All zeros fed to DAC input | 83 | 94 | | dB |
| DR | Dynamic range, A-weighted ⁽⁵⁾ ₍₆₎ | -60dB 1 kHz input full-scale signal | | 94 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | -3dB full-scale, 1-kHz input signal | | -75 | -60 | dB |
| | DAC Gain Error | -3dB, 1kHz input full scale signal | | 0.03 | | dB |
| | DAC Mute Attenuation | Mute | | 130 | | dB |
| | DAC channel separation | -3dB, 1kHz signal, between left and right HP out | | 80 | | dB |
| DAC PSRR | | 100mVpp, 1kHz signal applied to AVDD ₁₈ , AVDD1x ₁₈ | | 59 | | dB |
| | | 100mVpp, 217Hz signal applied to AVDD ₁₈ , AVDD1x ₁₈ | | 63 | | dB |
| | Power Delivered | THDN ≤ -40dB, Load = 16Ω | | 22 | | mW |
| Output 2 | Output voltage | Load = 16Ω (single-ended), Channel Gain = 5dB | | 0.8 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ⁽⁵⁾ ₍₆₎ | All zeros fed to DAC input, Load = 16Ω | | 95 | | dB |
| | Power Delivered | THDN ≤ -40dB, Load = 16Ω | | 25 | | mW |
| Output 3 | Output voltage | Load = 32Ω (single-ended), Channel Gain = 5dB | | 0.9 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ⁽⁵⁾ ₍₆₎ | All zeros fed to DAC input, Load = 32Ω | | 97 | | dB |
| | Power Delivered | THDN ≤ -40dB, Load = 32Ω | | 22 | | mW |

(5) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.

(6) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Audio DAC Outputs (continued)

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{\text{ext}} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (UNIPOLAR CIRCUIT CONFIGURATION) | | | | | |
| Device Setup | Load = 16Ω (single-ended), 56pF Input and Output CM=0.9V, DOSR = 128, MCLK=256* f_S , Channel Gain=0dB Processing Block = PRB_P1 Power Tune = PTM_P4 Headphone Output Control = 100% | | | | |
| Full scale output voltage (0dB) | | | 0.5 | | V_{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ^{(7) (8)} All zeros fed to DAC input | | 99 | | dB |
| DR | Dynamic range, A-weighted ^{(7) (8)} –60dB 1kHz input full-scale signal, Power Tune = PTM_P4 | | 99 | | dB |
| THD+N | Total Harmonic Distortion plus Noise –3dB full-scale, 1-kHz input signal | | –89 | –65 | dB |
| DAC Gain Error | –3dB, 1kHz input full scale signal | | –0.16 | | dB |
| DAC Mute Attenuation | Mute | | 126 | | dB |
| DAC channel separation | –1dB, 1kHz signal, between left and right HP out | | 119 | | dB |
| DAC PSRR | 100mVpp, 1kHz signal applied to AVDD_18, AVDD1x_18 | | 65 | | dB |
| | 100mVpp, 217Hz signal applied to AVDD_18, AVDD1x_18 | | 78 | | dB |
| Power Delivered | $R_L=16\Omega$ THDN ≤ –40dB, Input CM=0.9V, Output CM=0.9V | | 16 | | mW |

- (7) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (8) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Audio DAC Outputs (continued)

T_A = 25°C; AVDD₁₈, AVDDx₁₈, HVDD₁₈, CPVDD₁₈, DVDD, IOVDDx = 1.8V; RECVDD₃₃ = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------------------------|------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-----|------------------|
| AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT (UNIPOLAR CIRCUIT CONFIGURATION) | | | | | | |
| Device Setup | | Load = 16Ω (single-ended), 56pF, Input and Output CM=0.75V; AVDD ₁₈ , AVDDx ₁₈ , HVDD ₁₈ =1.5V, DOSR = 128, MCLK=256* f _S , Channel Gain = 0dB, Processing Block = PRB_P1, Power Tune = PTM_P4 Headphone Output Control = 100% | | | | |
| Full scale output voltage (0dB) | | | | 0.375 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ⁽⁹⁾ ₍₁₀₎ | All zeros fed to DAC input | | 99 | | dB |
| DR | Dynamic range, A-weighted ⁽⁹⁾ ₍₁₀₎ | -60dB 1 kHz input full-scale signal | | 99 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | -3dB full-scale, 1-kHz input signal | | -90 | | dB |
| AUDIO DAC – MONO DIFFERENTIAL RECEIVER OUTPUT | | | | | | |
| Device Setup | | Load = 32 Ω (differential), 56pF, Output CM=1.65V, AVDDx ₁₈ =1.8V, DOSR = 128 MCLK=256* f _S , Left DAC routed to RECP, RECM, Channel (Receiver Driver) Gain = 6dB for full scale output signal, Processing Block = PRB_P4, Power Tune = PTM_P4 | | | | |
| Full scale output voltage (0dB) | | | | 2 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ⁽⁹⁾ ₍₁₀₎ | All zeros fed to DAC input | 87 | 102 | | dB |
| DR | Dynamic range, A-weighted ⁽⁹⁾ ₍₁₀₎ | -60dB 1kHz input full-scale signal | | 102 | | dB |
| THD+N | Total Harmonic Distortion plus Noise | -3dB full-scale, 1-kHz input signal | | -91 | -70 | dB |
| DAC PSRR | | 100mVpp, 1kHz signal applied to AVDD ₁₈ , AVDD1x ₁₈ | | 64 | | dB |
| | | 100mVpp, 217Hz signal applied to AVDD ₁₈ , AVDD1x ₁₈ | | 64 | | dB |
| Power Delivered | | R _L =32Ω THDN ≤ -40dB, Input CM=0.9V, Output CM=1.65V | | 123 | | mW |

- (9) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (10) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Class-D Outputs

$T_A = 25^\circ\text{C}$; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; $C_{\text{ext}} = 1\mu\text{F}$ on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|-----|------------------|
| DAC OUTPUT to CLASS-D SPEAKER OUTPUT; Load = 8Ω (Differential), 56pF+33μH | | | | | | |
| Output voltage | SVDD=3.6, BTL measurement, DAC input = 0dBFS, class-D gain = 12dB, THD+N ≤ -20dB, CM=0.9V | | | 2.64 | | V _{RMS} |
| SNR | Signal-to-noise ratio | SVDD=3.6V, BTL measurement, class-D gain = 6dB, measured as idle-channel noise, A-weighted (with respect to full-scale output value of 2 V _{rms}) ⁽¹⁾ ⁽²⁾ , CM=0.9V | | 91 | | dB |
| THD | Total harmonic distortion | SVDD=3.6V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V | | -70 | | dB |
| THD+N | Total harmonic distortion + noise | SVDD=3.6V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V | | -70 | | dB |
| PSRR | Power-supply rejection ratio | SVDD=3.6V, BTL measurement, ripple on SVDD = 200 mVp-p at 1 kHz, CM=0.9V | | 64 | | dB |
| | | SVDD=3.6V, BTL measurement, ripple on SVDD = 200 mVp-p at 217 Hz, CM=0.9V | | 64 | | dB |
| | Mute attenuation | Analog Mute Only | | 92 | | dB |
| P _O | Maximum output power | THD+N = 10%, f = 1 kHz, Class-D Gain = 12 dB, CM = 0.9 V, R _L = 8 Ω | SVDD = 3.6 V | 0.72 | | W |
| | | | SVDD = 4.2 V | 0.99 | | |
| | | | SVDD = 5.5 V | 1.68 | | |
| | | THD+N = 1%, f = 1 kHz, Class-D Gain = 12 dB, CM = 0.9 V, R _L = 8 Ω | SVDD = 3.6 V | 0.58 | | |
| | | | SVDD = 4.2 V | 0.79 | | |
| | | | SVDD = 5.5 V | 1.36 | | |
| DAC OUTPUT to CLASS-D SPEAKER OUTPUT; Load = 8Ω (Differential), 56pF+33μH | | | | | | |
| Output voltage | SVDD=5.0V, BTL measurement, DAC input = 0dBFS, class-D gain = 12dB, THD+N ≤ -20dB, CM=0.9V | | | 3.40 | | V _{RMS} |
| SNR | Signal-to-noise ratio | SVDD=5.0V, BTL measurement, class-D gain = 6dB, measured as idle-channel noise, A-weighted (with respect to full-scale output value of 2 V _{rms}) ⁽¹⁾ ⁽²⁾ , CM=0.9V | | 92 | | |
| THD | Total harmonic distortion | SVDD=5.0V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V | | -72 | | |
| THD+N | Total harmonic distortion + noise | SVDD=5.0V, BTL measurement, DAC input = 0dBFS, class-D gain = 6dB, CM=0.9V | | -72 | | |
| PSRR | Power-supply rejection ratio | SVDD=5.0V, BTL measurement, ripple on SVDD = 200mVp-p at 1kHz, CM=0.9V | | 60 | | |
| | | SVDD=5.0V, BTL measurement, ripple on SVDD = 200 mVp-p at 217 Hz, CM=0.9V | | 60 | | |
| | Mute attenuation | Analog Mute Only | | 93 | | dB |
| P _O | Maximum output power | THD+N = 10%, f = 1 kHz, Class-D Gain = 12 dB, CM = 0.9 V, R _L = 8 Ω | SVDD = 5.0 V | 1.40 | | W |

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, Misc.

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|------|-------------------|
| REFERENCE - VREF_AUDIO | | | | | |
| Reference Voltage Settings | CMMode = 0 (0.9V) | | 0.9 | | V |
| | CMMode = 1 (0.75V) | | 0.75 | | |
| Reference Noise | CM=0.9V, A-weighted, 20Hz to 20kHz bandwidth, C _{ref} = 1µF | | 1.62 | | µV _{RMS} |
| Decoupling Capacitor | | | 1 | | µF |
| miniDSP⁽¹⁾ | | | | | |
| miniDSP clock frequency - ADC | DVDD = 1.26V | | | 37.5 | MHz |
| miniDSP clock frequency - DAC | DVDD = 1.26V | | | 35.0 | MHz |
| miniDSP clock frequency - ADC | DVDD = 1.65V | | | 63 | MHz |
| miniDSP clock frequency - DAC | DVDD = 1.65V | | | 59.0 | MHz |
| miniDSP clock frequency - ADC | DVDD = 1.71V | | | 69 | MHz |
| miniDSP clock frequency - DAC | DVDD = 1.71V | | | 62.5 | MHz |
| Shutdown Power | | | | | |
| Device Setup | Coarse AVdd supply turned off, All External analog supplies powered and set available, No external digital input is toggled, register values are retained. | | | | |
| P(total) ⁽²⁾ | Sum of all supply currents, all supplies at 1.8 V except for SVDD = SPK_V = MICBIAS_VDD = 3.6 V and RECVDD_33 = 3.3 V | | 9.8 | | µW |
| I(DVDD) | | | 2.6 | | µA |
| I(IOVDD1, IOVDD2, IOVDD3) | | | 0.15 | | µA |
| I(AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18, HVDD_18, CPVDD_18) | | | 1.15 | | µA |
| I(RECVDD_33) | | | 0.15 | | µA |
| I(SVDD, SPK_V, MICBIAS_VDD) | | | 0.5 | | µA |

- (1) miniDSP clock speed is specified by design and not tested in production.
- (2) For further details on playback and recording power consumption, refer to PowerTune section in SLAU475.

Electrical Characteristics, Logic Levels, IOVDDx

T_A = 25°C; AVDD_18, AVDDx_18, HVDD_18, CPVDD_18, DVDD, IOVDDx = 1.8V; RECVDD_33 = 3.3V; SVDD, SPK_V, MICBIAS_VDD = 3.6V; f_S (Audio) = 48kHz; Audio Word Length = 20 bits; C_{ext} = 1µF on VREF_SAR and VREF_AUDIO pins; PLL disabled unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|----------------------------------------------|--------------|--------------|-----|------|
| LOGIC FAMILY | | | | | |
| CMOS | | | | | |
| V _{IH} Logic Level | I _{IH} = 5 µA, IOVDDx > 1.65V | 0.7 × IOVDDx | | | V |
| | I _{IH} = 5µA, 1.2V ≤ IOVDDx < 1.65V | 0.9 × IOVDDx | | | V |
| | I _{IH} = 5µA, IOVDDx < 1.2V | IOVDDx | | | V |
| V _{IL} | I _{IL} = 5 µA, IOVDDx > 1.65V | -0.3 | 0.3 × IOVDDx | | V |
| | I _{IL} = 5µA, 1.2V ≤ IOVDDx < 1.65V | | 0.1 × IOVDDx | | V |
| | I _{IL} = 5µA, IOVDDx < 1.2V | | | 0 | V |
| V _{OH} | I _{OH} = 3mA load, IOVDDx > 1.65V | 0.8 × IOVDDx | | | V |
| | I _{OH} = 1mA load, IOVDDx < 1.65V | 0.8 × IOVDDx | | | V |
| V _{OL} | I _{OL} = 3mA load, IOVDDx > 1.65V | | 0.1 × IOVDDx | | V |
| | I _{OL} = 1mA load, IOVDDx < 1.65V | | 0.1 × IOVDDx | | V |
| Capacitive Load | | | 10 | | pF |

Interface Timing

Note: All timing specifications are measured at characterization but not tested at final test. The audio serial interface timing specifications are applied to Audio Serial Interface 1, Audio Serial Interface 2 and Audio Serial Interface 3.

Typical Timing Characteristics — Audio Data Serial Interface Timing (I²S)

WCLK represents WCLK1 pin for Audio Serial Interface 1 BCLK represents BCLK1 pin for Audio Serial Interface 1 DOUT represents DOUT1 pin for Audio Serial Interface 1 DIN represents DIN1 pin for Audio Serial Interface 1 Specifications are at 25° C with DVDD = 1.8V and IOVDDx = 1.8 V.

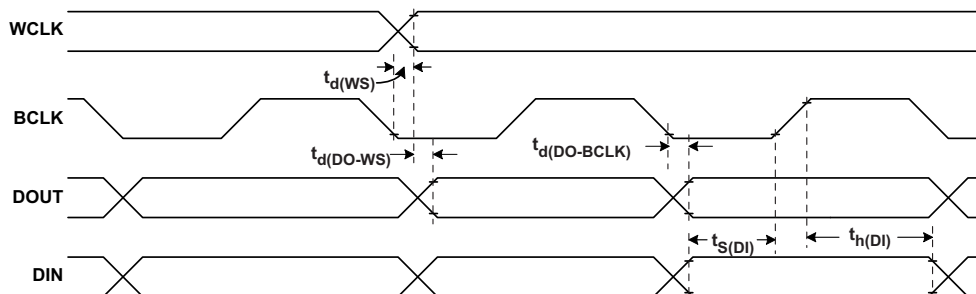


Figure 3. I²S/LJF/RJF Timing in Master Mode

Table 2. I²S/LJF/RJF Timing in Master Mode (see Figure 3)

| PARAMETER | | IOVDDx=1.8V | | IOVDDx=3.3V | | UNITS |
|----------------|----------------------------------------|-------------|-----|-------------|-----|-------|
| | | MIN | MAX | MIN | MAX | |
| $t_d(WS)$ | WCLK delay | | 22 | | 20 | ns |
| $t_d(DO-WS)$ | WCLK to DOUT delay (For LJF Mode only) | | 22 | | 20 | ns |
| $t_d(DO-BCLK)$ | BCLK to DOUT delay | | 22 | | 20 | ns |
| $t_s(DI)$ | DIN setup | 4 | | 4 | | ns |
| $t_h(DI)$ | DIN hold | 4 | | 4 | | ns |
| t_r | BCLK Rise time | | 10 | | 8 | ns |
| t_f | BCLK Fall time | | 10 | | 8 | ns |

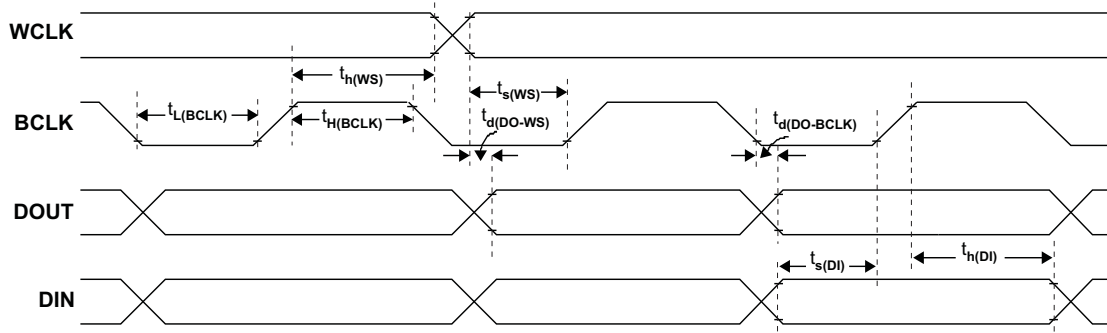


Figure 4. I²S/LJF/RJF Timing in Slave Mode

Table 3. I²S/LJF/RJF Timing in Slave Mode (see Figure 4)

| PARAMETER | | IOVDDx=1.8V | | IOVDDx=3.3V | | UNITS |
|--------------------------|----------------------------------------|-------------|-----|-------------|-----|-------|
| | | MIN | MAX | MIN | MAX | |
| t _H (BCLK) | BCLK high period | 30 | | 30 | | ns |
| t _L (BCLK) | BCLK low period | 30 | | 30 | | |
| t _s (WS) | WCLK setup | 4 | | 4 | | |
| t _h (WS) | WCLK hold | 4 | | 4 | | |
| t _d (DO-WS) | WCLK to DOUT delay (For LJF mode only) | | 22 | | 20 | |
| t _d (DO-BCLK) | BCLK to DOUT delay | | 22 | | 20 | |
| t _s (DI) | DIN setup | 4 | | 4 | | |
| t _h (DI) | DIN hold | 4 | | 4 | | |
| t _r | BCLK Rise time | | 5 | | 4 | |
| t _f | BCLK Fall time | | 5 | | 4 | |

Typical DSP Timing Characteristics

Specifications are at 25° C with DVDD = 1.8 V.

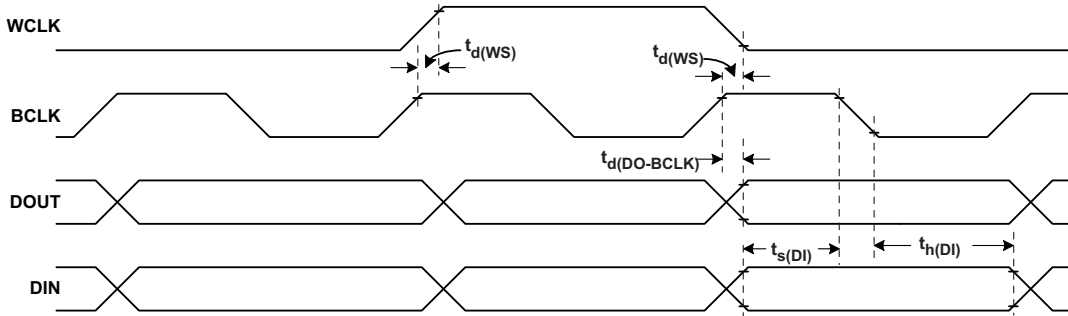


Figure 5. DSP/Mono PCM Timing in Master Mode

Table 4. DSP/Mono PCM Timing in Master Mode (see Figure 5)

| PARAMETER | | IOVDDx=1.8V | | IOVDDx=3.3V | | UNITS |
|----------------|--------------------|-------------|-----|-------------|-----|-------|
| | | MIN | MAX | MIN | MAX | |
| $t_d(WS)$ | WCLK delay | | 22 | | 20 | ns |
| $t_d(DO-BCLK)$ | BCLK to DOUT delay | | 22 | | 20 | ns |
| $t_s(DI)$ | DIN setup | 4 | | 4 | | ns |
| $t_h(DI)$ | DIN hold | 4 | | 4 | | ns |
| t_r | BCLK Rise time | | 10 | | 8 | ns |
| t_f | BCLK Fall time | | 10 | | 8 | ns |

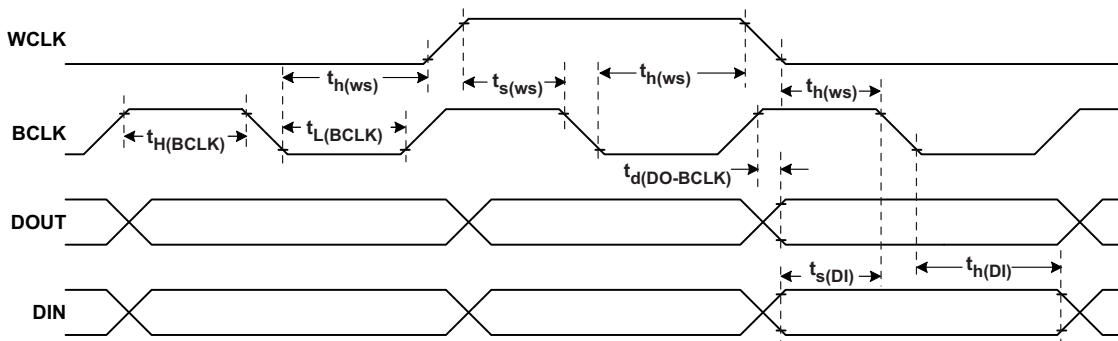


Figure 6. DSP/Mono PCM Timing in Slave Mode

Table 5. DSP/Mono PCM Timing in Slave Mode (see Figure 6)

| PARAMETER | | IOVDDx=1.8V | | IOVDDx=3.3V | | UNITS |
|----------------|--------------------|-------------|-----|-------------|-----|-------|
| | | MIN | MAX | MIN | MAX | |
| $t_H(BCLK)$ | BCLK high period | 30 | | 30 | | ns |
| $t_L(BCLK)$ | BCLK low period | 30 | | 30 | | ns |
| $t_s(WS)$ | WCLK setup | 4 | | 4 | | ns |
| $t_h(WS)$ | WCLK hold | 4 | | 4 | | ns |
| $t_d(DO-BCLK)$ | BCLK to DOUT delay | | 22 | | 20 | ns |
| $t_s(DI)$ | DIN setup | 5 | | 5 | | ns |
| $t_h(DI)$ | DIN hold | 5 | | 5 | | ns |
| t_r | BCLK Rise time | | 5 | | 4 | ns |
| t_f | BCLK Fall time | | 5 | | 4 | ns |

I²C Interface Timing

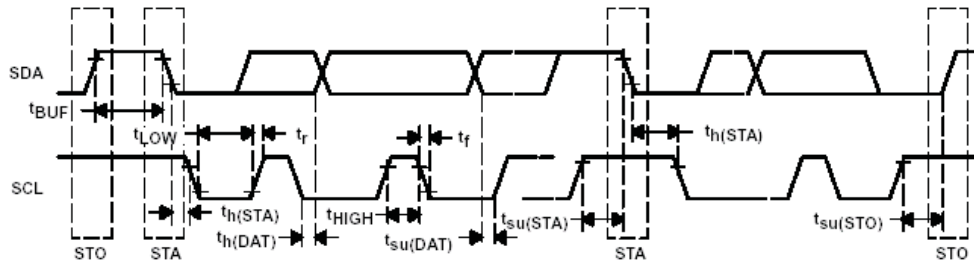


Figure 7. I²C Interface Timing Diagram

Table 6. I²C Interface Timing (see Figure 7)

| PARAMETER | TEST CONDITION | Standard-Mode | | | Fast-Mode | | | UNITS | | | |
|---------------------|----------------------------------------------------------------------------------------------|---------------|-----|-----|-----------|------|-----|------------------------|--|-----|-----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | | | | |
| f _{SCL} | SCL clock frequency | | | 0 | | 100 | | 0 | | 400 | kHz |
| t _{HD;STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | | | 4.0 | | | | 0.8 | | | μs |
| t _{LOW} | LOW period of the SCL clock | | | 4.7 | | | | 1.3 | | | μs |
| t _{HIGH} | HIGH period of the SCL clock | | | 4.0 | | | | 0.6 | | | μs |
| t _{SU;STA} | Setup time for a repeated START condition | | | 4.7 | | | | 0.8 | | | μs |
| t _{HD;DAT} | Data hold time: For I2C bus devices | | | 0 | | 3.45 | | 0 | | 0.9 | μs |
| t _{SU;DAT} | Data set-up time | | | 250 | | | | 100 | | | ns |
| t _r | SDA and SCL Rise Time | | | | | 1000 | | 20 + 0.1C _b | | 300 | ns |
| t _f | SDA and SCL Fall Time | | | | | 300 | | 20 + 0.1C _b | | 300 | ns |
| t _{SU;STO} | Set-up time for STOP condition | | | 4.0 | | | | 0.8 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | | | 4.7 | | | | 1.3 | | | μs |
| C _b | Capacitive load for each bus line | | | | | 400 | | | | 400 | pF |

SPI Interface Timing

SS = SCL pin, **SCLK** = I2C_ADDR_SCLK pin, **MISO** = GPO1 pin, and **MOSI** = SDA pin. Specifications are at 25° C with DVDD = 1.8V.

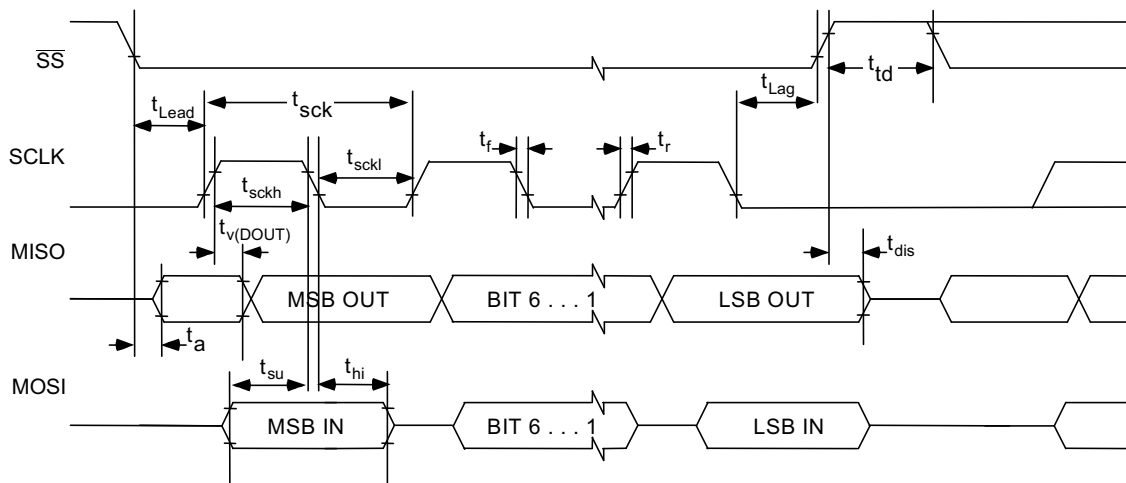


Figure 8. SPI Interface Timing Diagram

Timing Requirements (See Figure 8)

Specifications are at 25° C with DVDD = 1.8 V.

Table 7. SPI Interface Timing

| PARAMETER | TEST CONDITION | IOVDD1=1.8V | | | IOVDD1=3.3V | | | UNITS |
|-----------------------|--------------------------------|-------------|-----|-----|-------------|-----|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t _{sck} | SCLK Period ⁽¹⁾ | 50 | | | 40 | | | ns |
| t _{sckh} | SCLK Pulse width High | 25 | | | 20 | | | ns |
| t _{sckl} | SCLK Pulse width Low | 25 | | | 20 | | | ns |
| t _{lead} | Enable Lead Time | 25 | | | 20 | | | ns |
| t _{trail} | Enable Trail Time | 25 | | | 20 | | | ns |
| t _{d,seqxfr} | Sequential Transfer Delay | 25 | | | 20 | | | ns |
| t _a | Slave DOUT (MISO) access time | | | 25 | | | 20 | ns |
| t _{dis} | Slave DOUT (MISO) disable time | | | 25 | | | 20 | ns |
| t _{su} | DIN (MOSI) data setup time | 8 | | | 8 | | | ns |
| t _{h,DIN} | DIN (MOSI) data hold time | 8 | | | 8 | | | ns |
| t _{v,DOUT} | DOUT (MISO) data valid time | | | 20 | | | 14 | ns |
| t _r | SCLK Rise Time | | | 4 | | | 4 | ns |
| t _f | SCLK Fall Time | | | 4 | | | 4 | ns |

(1) These parameters are based on characterization and are not tested in production.

Typical Characteristics

Device Power Consumption

Device power consumption largely depends on PowerTune configuration. For information on device power consumption, see the *TLV320AIC3263 Application Reference Guide*, literature number SLAU475.

Typical Performance

Audio ADC Performance

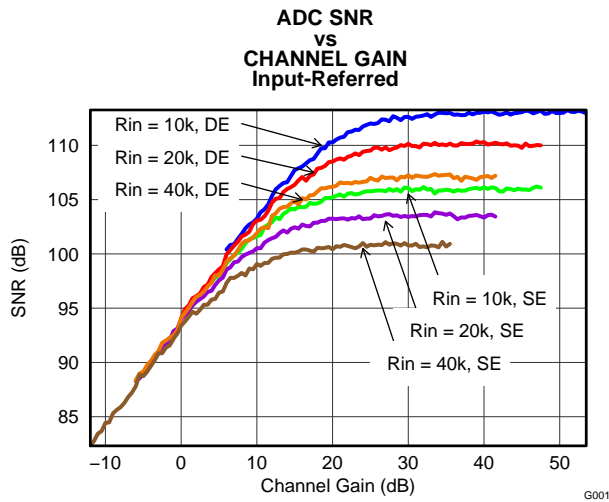


Figure 9.

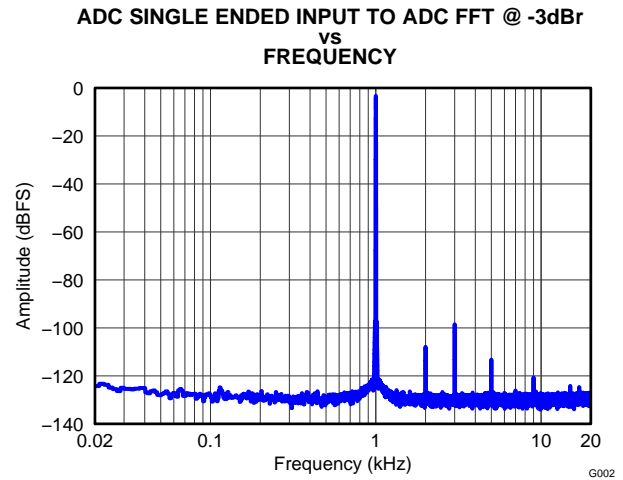


Figure 10.

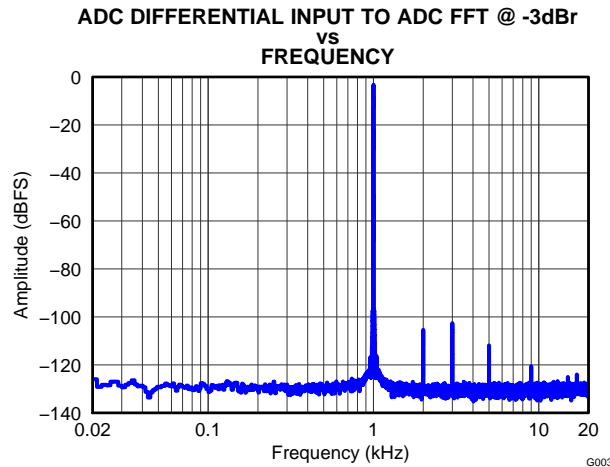


Figure 11.

Audio DAC Performance

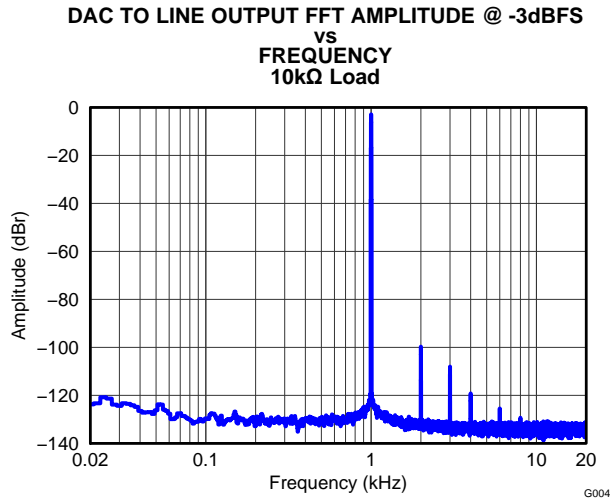


Figure 12.

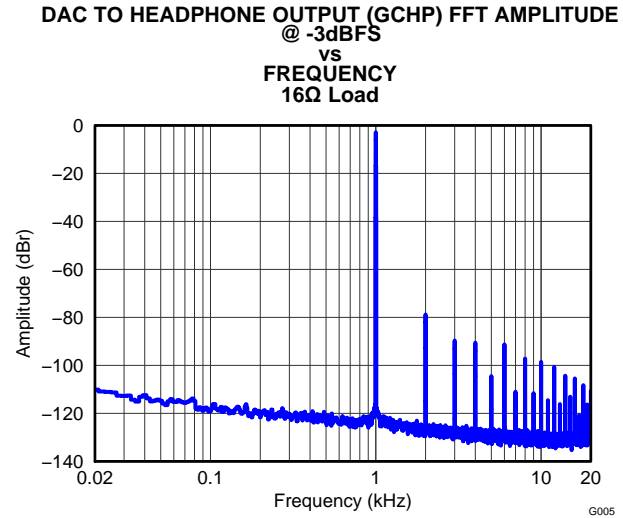


Figure 13.

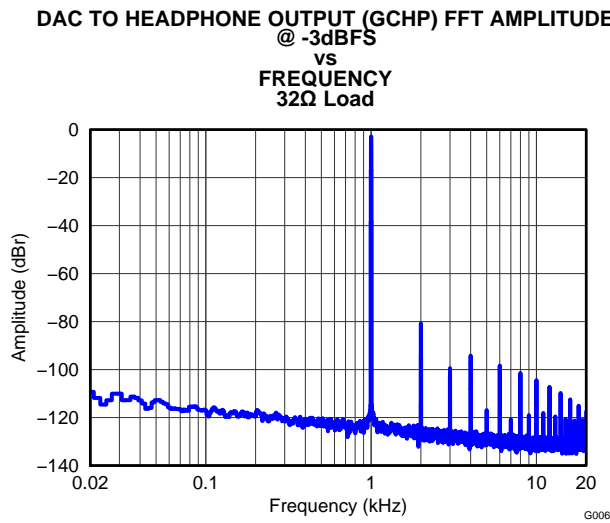


Figure 14.

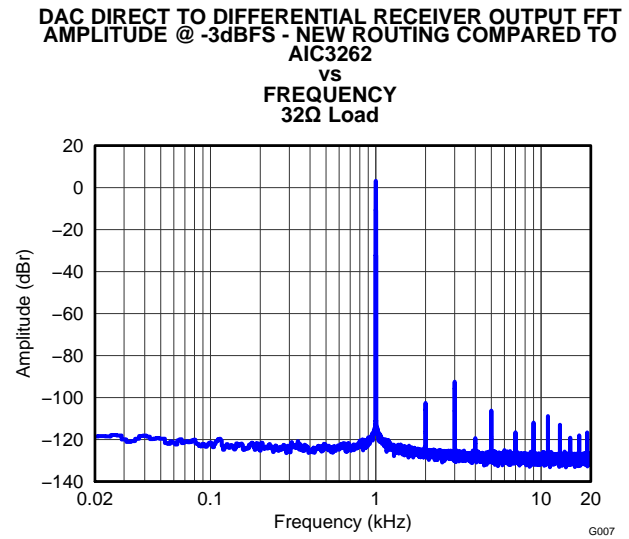


Figure 15.

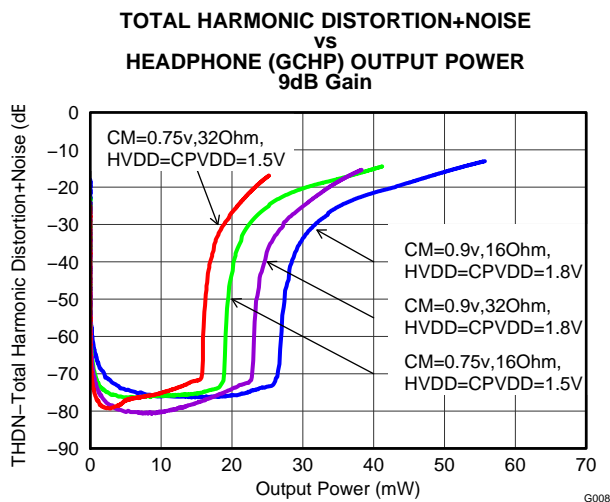


Figure 16.

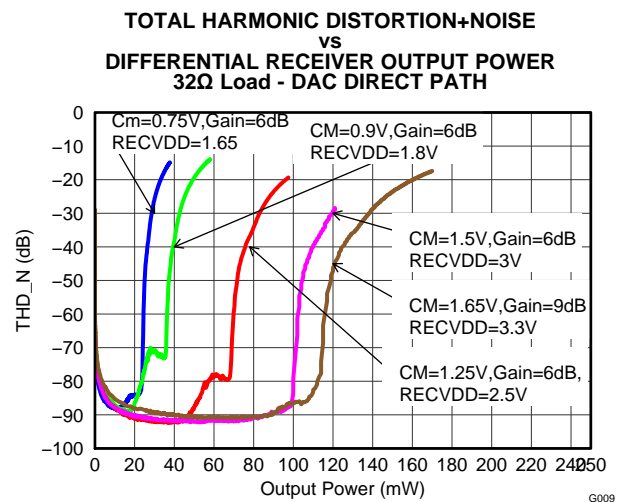


Figure 17.

**DIFFERENTIAL RECEIVER SNR AND OUTPUT POWER (DAC DIRECT PATH)
vs
OUTPUT COMMON MODE SETTING
32Ω Load**

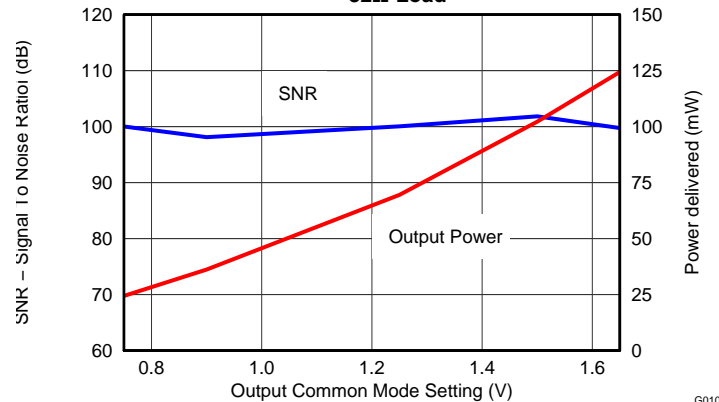


Figure 18.

Class-D Driver Performance

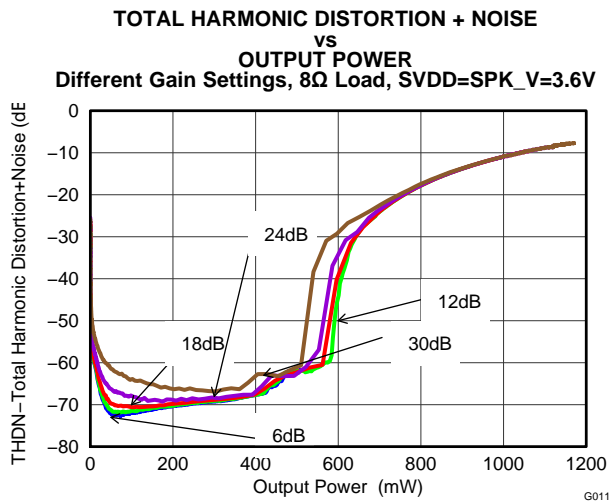


Figure 19.

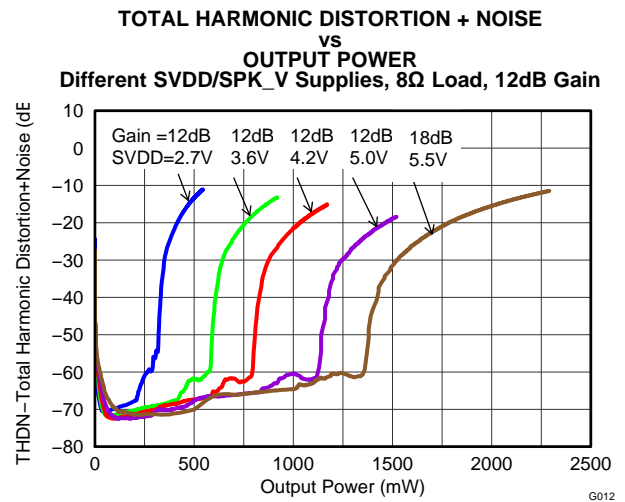


Figure 20.

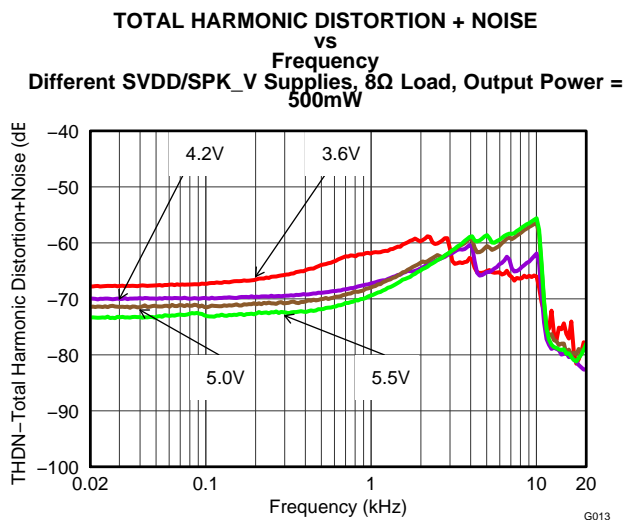


Figure 21.

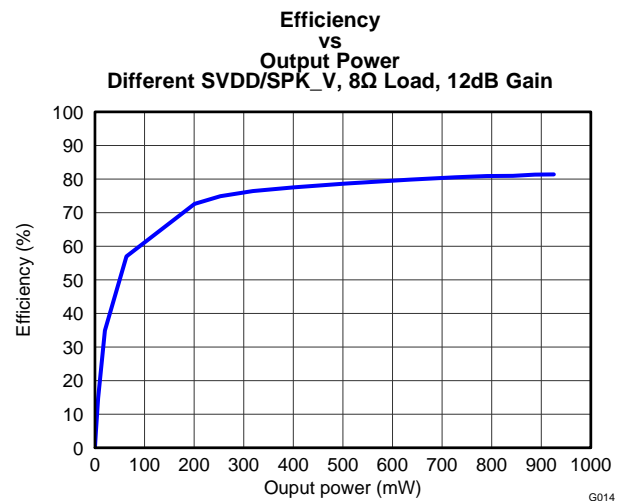


Figure 22.

MICBIAS Performance

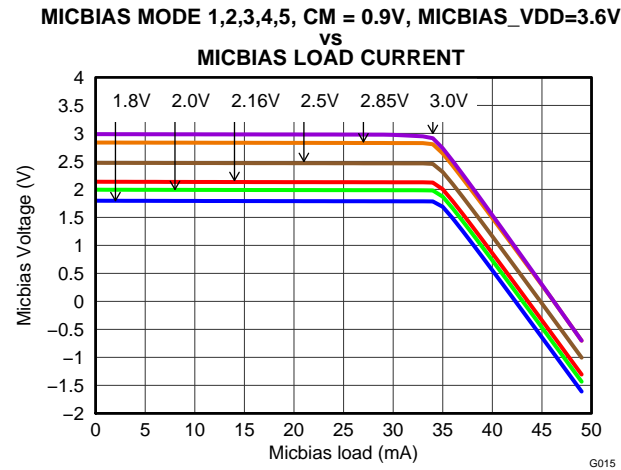


Figure 23.

Application Overview

Typical Circuit Configuration

Figure 24 shows a typical circuit configuration for a system utilizing TLV320AIC3263. Note that while this circuit configuration shows all three Audio Serial Interfaces connected to a single Host Processor, it is also quite common for these Audio Serial Interfaces to connect to separate devices (such as Host Processor on Audio Serial Interface 1, and modems and/or Bluetooth devices on the other audio serial interfaces).

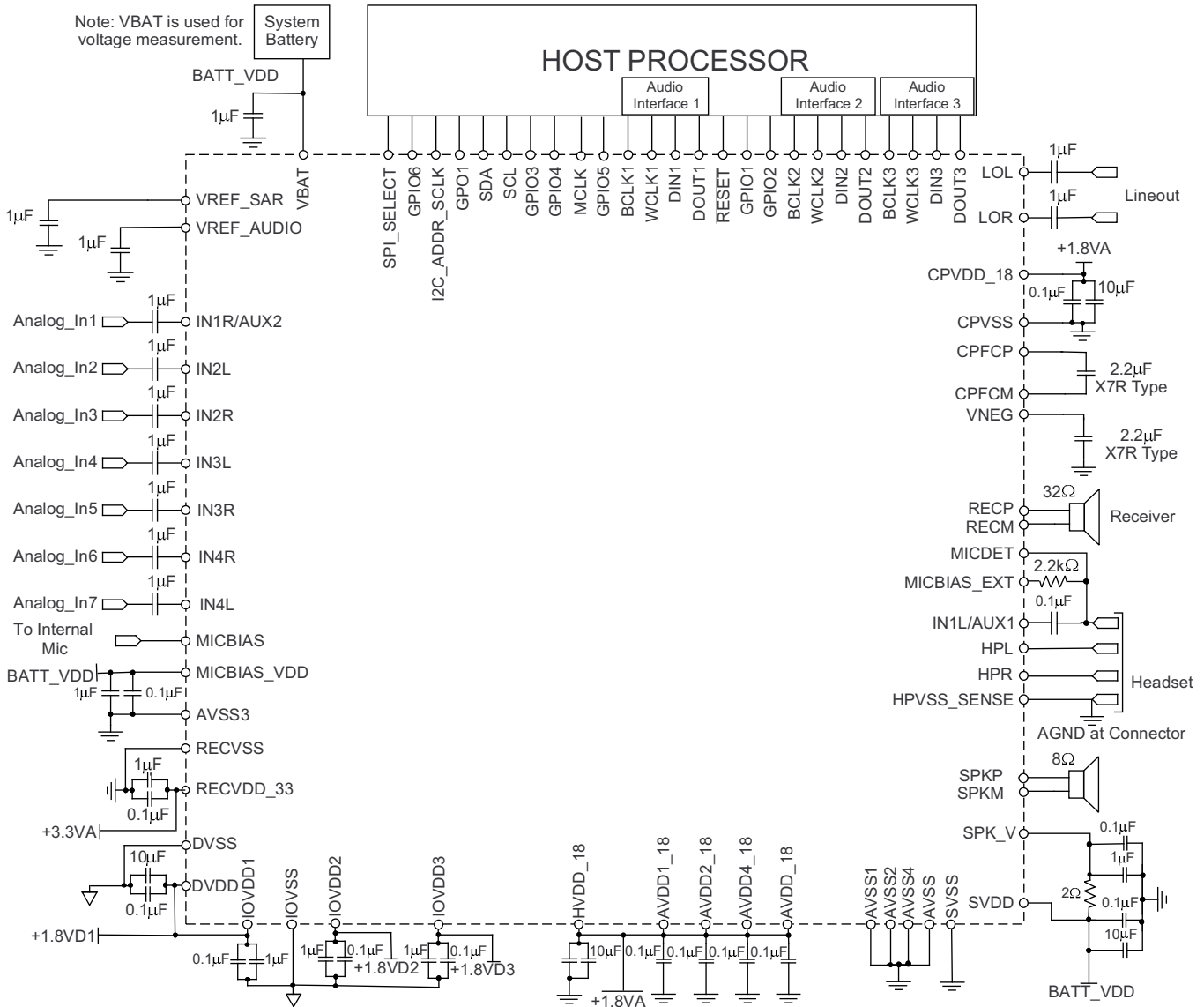


Figure 24. Typical Circuit Configuration

Device Connections

Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are hardware-control pins $\overline{\text{RESET}}$ and SPI_SELECT pin. Depending on the state of SPI_SELECT, four pins SCL, SDA, GPO1, and I2C_ADDR_SCLK are configured for either I²C or SPI protocol. Only in I²C mode, I2C_ADDR_SCLK provide two possible I²C addresses for the TLV320AIC3263, while this pin receives the SPI SCLK when the device is set to SPI mode.

Other digital IO pins can be configured for various functions via register control.

Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

The possible analog routings of analog input pins to ADCs and output amplifiers as well as the routing from DACs to output amplifiers can be seen in the Analog Routing Diagram.

Multifunction Pins

Table 8 show the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 9 pins (MCLK, BCLK1, DIN1, BCLK2, BCLK3, GPIO1, GPIO2, GPIO3, GPIO6).

Table 8. Multifunction Pin Assignments for Pins MCLK, GPIO5, WCLK1, BCLK1, DIN1, DOUT1, WCLK2, BCLK2, DIN2, and DOUT2

| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|-------------------------------------|------|-------|-------|-------|---------------------|------------------|-------|-------|------|-------|
| | Pin Function | MCLK | GPIO5 | WCLK1 | BCLK1 | DIN1 | DOUT1 | WCLK2 | BCLK2 | DIN2 | DOUT2 |
| A | INT1 Output | | | | | | E | E | E | | E |
| B | INT2 Output | | | | | | E | E | E | | E |
| D | CLOCKOUT Output | | | E | | | E | E | E | | |
| E | ADC_MOD_CLOCK Output | | E | | | | | E | E | | E |
| F | Single DOUT for ASI1 (All Channels) | | E | | | | E, D | | | | |
| F | Single DOUT for ASI2 | | E | | | | | | | | E, D |
| F | Single DOUT for ASI3 | | E | | | | | | | | |
| G | Multiple DOUTs for ASI1 (L1, R1) | | | | | | E | | | | |
| G | Multiple DOUTs for ASI1 (L2, R2) | | | | | | | | | | E |
| G | Multiple DOUTs for ASI1 (L3, R3) | | | | | | | | E | | |
| G | Multiple DOUTs for ASI1 (L4, R4) | | | | | | | E | | | |
| I | General Purpose Output (via Reg) | | | | | | E ⁽¹⁾ | E | E | | E |
| F | Single DIN for ASI1 (All Channels) | | | | | E, D ⁽²⁾ | | | | | |
| F | Single DIN for ASI2 | | | | | | | | | E, D | |
| F | Single DIN for ASI3 | | | | | | | | | | |
| H | Multiple DINs for ASI1 (L1, R1) | | | | | E | | | | | |
| H | Multiple DINs for ASI1 (L2, R2) | | | | | | | | | E | |
| H | Multiple DINs for ASI1 (L3, R3) | | E | | | | | | E | | |
| H | Multiple DINs for ASI1 (L4, R4) | | E | | | | | E | | | |
| J | Digital Mic Data | | E | | | E | | | | E | |

(1) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (such as if DOUT1 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

(2) D: Default Function

Table 8. Multifunction Pin Assignments for Pins MCLK, GPIO5, WCLK1, BCLK1, DIN1, DOUT1, WCLK2, BCLK2, DIN2, and DOUT2 (continued)

| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|-----------|-------------------------------------|----------------------|-------|-------|----------------------|------|-------|-------|----------------------|------|-------|
| | Pin Function | MCLK | GPIO5 | WCLK1 | BCLK1 | DIN1 | DOUT1 | WCLK2 | BCLK2 | DIN2 | DOUT2 |
| K | Input to PLL_CLKIN | S ⁽³⁾ , D | | | S ⁽⁴⁾ | S | | | S ⁽⁴⁾ | | |
| L | Input to ADC_CLKIN | S ⁽³⁾ , D | S | | S ⁽⁴⁾ | | | | S ⁽⁴⁾ | | |
| M | Input to DAC_CLKIN | S ⁽³⁾ , D | S | | S ⁽⁴⁾ | | | | S ⁽⁴⁾ | | |
| N | Input to CDIV_CLKIN | S ⁽³⁾ , D | S | | S | S | | | S | | |
| O | Input to LFR_CLKIN | S ⁽³⁾ , D | S | S | | | | S | S | S | |
| P | Input to HF_CLK | S ⁽³⁾ | | | | | | | | | |
| Q | Input to REF_1MHz_CLK | S ⁽³⁾ | | | | | | | | | |
| R | General Purpose Input (via Reg) | | E | | | E | | E | E | E | |
| S | ISR Interrupt for miniDSP (via Reg) | | | | | | | | | E | |
| T | WCLK Output for ASI1 | | | E | | | | | | | |
| U | WCLK Input for ASI1 | | | S, D | | | | | | | |
| V | BCLK Output for ASI1 | | | | E | | | | | | |
| W | BCLK Input for ASI1 | | | | S ⁽⁴⁾ , D | | | | | | |
| X | WCLK Output for ASI2 | | | | | | | E | | | |
| Y | WCLK Input for ASI2 | | | | | | | S, D | | | |
| Z | BCLK Output for ASI2 | | | | | | | | E | | |
| AA | BCLK Input for ASI2 | | | | | | | | S ⁽⁴⁾ , D | | |
| BB | WCLK Output for ASI3 | | | | | | | | | | |
| CC | WCLK Input for ASI3 | | | | | | | | | | |
| DD | BCLK Output for ASI3 | | | | | | | | | | |
| EE | BCLK Input for ASI3 | | | | | | | | | | |

- (3) S⁽³⁾: The MCLK pin could be chosen to drive the PLL, ADC Clock, DAC Clock, CDIV Clock, LFR Clock, HF Clock, and REF_1MHz_CLK inputs **simultaneously**
- (4) S⁽⁴⁾: The BCLK1 or BCLK2 pins could be chosen to drive the PLL, ADC Clock, DAC Clock, and audio interface bit clock inputs **simultaneously**

Table 9. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, I2C_ADDR_SCL, GPIO6, GPIO3, and GPIO4

| | | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
|----------|-------------------------------------|-------|-------|------|-------|-------|-------|------------------------------|--------------|-------|-------|-------|
| | Pin Function | WCLK3 | BCLK3 | DIN3 | DOUT3 | GPIO1 | GPIO2 | GPO1/ MISO ⁽¹⁾ | I2C_ADDR_SCL | GPIO6 | GPIO3 | GPIO4 |
| A | INT1 Output | | | | | E | E | E | | | | |
| B | INT2 Output | | | | | E | E | E | | | | |
| D | CLOCKOUT Output | | | | | E | E | E | | | | |
| E | ADC_MOD_CLOCK Output | | | | E | E | E | E | | E | E | E |
| F | Single DOUT for ASI1 (All Channels) | | | | | | | E | | E | | |
| F | Single DOUT for ASI2 | | | | | | | | | | | |
| F | Single DOUT for ASI3 | | | | E, D | | | | | | | |
| G | Multiple DOUTs for ASI1 (L1, R1) | | | | | | | | | | | |
| G | Multiple DOUTs for ASI1 (L2, R2) | | | | E | | E | E | | | | |
| G | Multiple DOUTs for ASI1 (L3, R3) | | E | | E | E | E | E | | | | |

(1) GPO1 can only be utilized for functions defined in this table when part utilizes I²C for control. In SPI mode, this pin serves as MISO.

Table 9. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPIO3, I2C_ADDR_SCL, GPIO6, GPIO3, and GPIO4 (continued)

| | | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
|-----------|-------------------------------------|---------------------|------------------|------|-------|------------------|------------------|------------------------------|--------------|------------------|------------------|-------|
| | Pin Function | WCLK3 | BCLK3 | DIN3 | DOUT3 | GPIO1 | GPIO2 | GPO1/ MISO ⁽¹⁾ | I2C_ADDR_SCL | GPIO6 | GPIO3 | GPIO4 |
| G | Multiple DOUTs for ASI1 (L4, R4) | E | | | | E | E | E | | | | |
| I | General Purpose Output (via Reg) | E ⁽²⁾ | E | | E | E | E | E | | | | |
| F | Single DIN for ASI1 (All Channels) | | | | | | | | | E | | |
| F | Single DIN for ASI2 | | | | | | | | | E | | |
| F | Single DIN for ASI3 | | | E, D | | | | | | E | | |
| H | Multiple DINs for ASI1 (L1, R1) | | | | | | | | | | | |
| H | Multiple DINs for ASI1 (L2, R2) | | | | | | E | | | E | E | |
| H | Multiple DINs for ASI1 (L3, R3) | | | E | | E | E | | | E | E | |
| H | Multiple DINs for ASI1 (L4, R4) | | | | | E | E | | | E | E | |
| J | Digital Mic Data | E | E | E | | E | E | | | E | E | E |
| K | Input to PLL_CLKIN | | S ⁽³⁾ | | | S ⁽³⁾ | S ⁽³⁾ | | | S ⁽³⁾ | S ⁽³⁾ | |
| L | Input to ADC_CLKIN | | S ⁽³⁾ | | | S ⁽³⁾ | S ⁽³⁾ | | | S ⁽³⁾ | S ⁽³⁾ | |
| M | Input to DAC_CLKIN | | S ⁽³⁾ | | | S ⁽³⁾ | S ⁽³⁾ | | | S ⁽³⁾ | S ⁽³⁾ | |
| N | Input to CDIV_CLKIN | | | | | | | | | S | S | |
| O | Input to LFR_CLKIN | S | S | | | S | S | | | S | S | |
| P | Input to HF_CLK | | | | | | | | | | | |
| Q | Input to REF_1MHz_CLK | | | | | | | | | | | |
| R | General Purpose Input (via Reg) | E | E | E | | E | E | | | E | | E |
| S | ISR Interrupt for miniDSP (via Reg) | | | | | E | E | | | | E | |
| T | WCLK Output for ASI1 | | | | E | E | | | | | | |
| U | WCLK Input for ASI1 | | | | | E | | | | | | |
| V | BCLK Output for ASI1 | | | | | | E | | | | | |
| W | BCLK Input for ASI1 | | | | | | E | | | | | |
| X | WCLK Output for ASI2 | | | | | E | | | | | | |
| Y | WCLK Input for ASI2 | | | | | E | | | | | | |
| Z | BCLK Output for ASI2 | | | | | | E | | | | | |
| AA | BCLK Input for ASI2 | | | | | | E | | | | | |
| BB | WCLK Output for ASI3 | E | | | | E | | | | | | |
| CC | WCLK Input for ASI3 | S, D ⁽⁴⁾ | | | | E | | | | | | |
| DD | BCLK Output for ASI3 | | E | | | | E | | | | | |
| EE | BCLK Input for ASI3 | | S, D | | | | E | | | | | |
| FF | ADC BCLK Input for ASI1 | | | | | E | E | | | E | E | E |

(2) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (such as if WCLK3 has been allocated for General Purpose Output, it cannot be used as the ASI3 WCLK output at the same time)

(3) S⁽⁴⁾: The GPIO1, GPIO2, GPIO3, or GPIO6 pins could be chosen to drive the PLL, ADC Clock, and DAC Clock inputs **simultaneously**

(4) D: Default Function

Table 9. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, I2C_ADDR_SCL, GPIO6, GPIO3, and GPIO4 (continued)

| | | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
|-----------|--------------------------|-------|-------|------|-------|-------|-------|------------------------------|--------------|-------|-------|-------|
| | Pin Function | WCLK3 | BCLK3 | DIN3 | DOUT3 | GPIO1 | GPIO2 | GPO1/ MISO ⁽¹⁾ | I2C_ADDR_SCL | GPIO6 | GPIO3 | GPIO4 |
| GG | ADC WCLK Input for ASI1 | | | | | E | E | | | E | E | E |
| HH | ADC BCLK Output for ASI1 | | | | | E | E | | | | | |
| II | ADC WCLK Output for ASI1 | | | | | E | E | | | | | |
| JJ | ADC BCLK Input for ASI2 | | | | | E | E | | | E | E | E |
| KK | ADC WCLK Input for ASI2 | | | | | E | E | | | E | E | E |
| LL | ADC BCLK Output for ASI2 | | | | | E | E | | | | | |
| MM | ADC WCLK Output for ASI2 | | | | | E | E | | | | | |
| NN | ADC BCLK Input for ASI3 | | | | | E | E | | | E | E | E |
| OO | ADC WCLK Input for ASI3 | | | | | E | E | | | E | E | E |
| PP | ADC BCLK Output for ASI3 | | | | | E | E | | | | | |
| QQ | ADC WCLK Output for ASI3 | | | | | E | E | | | | | |
| RR | Bit Bang Input | | | | | E | E | | | E | E | E |
| SS | Bit Bang Output | | | | | E | E | | | E | E | E |

Analog Audio I/O

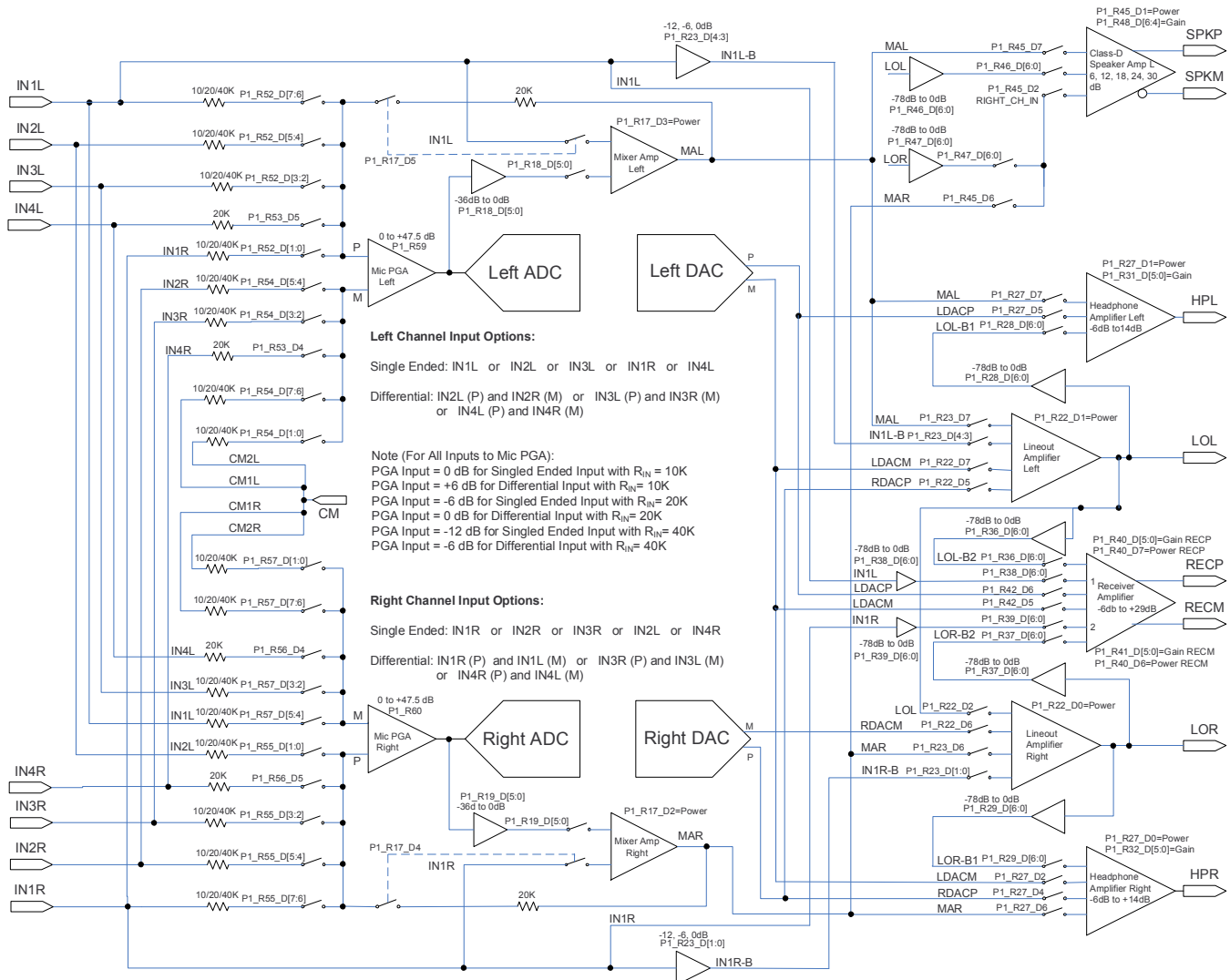


Figure 25. Analog Routing Diagram

For more detailed information see the TLV320AIC3263 Application Reference Guide [SLAU475](#).

Analog Low Power Bypass

The TLV320AIC3263 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode. In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1L to the left lineout amplifier (LOL) and IN1R to LOR. Additionally, line-level signals can be routed directly from these analog inputs to the amplifier, which outputs on RECP and RECM.

ADC Bypass Using Mixer Amplifiers

In addition to the low-power bypass mode, there is a bypass mode that uses the programmable gain amplifiers of the input stage in conjunction with a mixer amplifier. With this mode, microphone-level signals can be amplified and routed to the line, speaker, or headphone outputs, fully bypassing the ADC and DAC. To enable this mode, the mixer amplifiers are powered on via software command.

Headphone Outputs

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended DC-coupled headphone configurations. An integral charge pump generates the negative supply required to operate the headphone drivers in dc-coupled mode, where the common mode of the output signal is made equal to the ground of the headphone load using a ground-sense circuit. Operation of headphone drivers in dc-coupled (ground centered mode) eliminates the need for large dc-blocking capacitors.

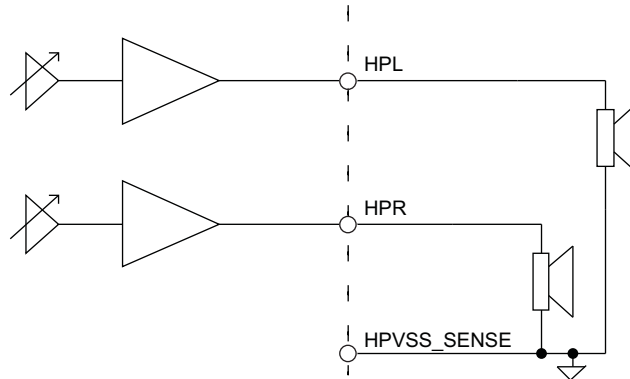


Figure 26. TLV320AIC3263 Ground-Centered Headphone Output

Alternatively the headphone amplifier can also be operated in a unipolar circuit configuration using DC blocking capacitors.

Stereo Line Outputs

The stereo line level drivers on LOL and LOR pins can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common mode of line level drivers can be configured to equal the analog input common-mode setting, either 0.75V or 0.9V. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal, and signal mixing is register-programmable.

Differential Receiver Output

The differential receiver amplifier output spans the RECP and RECM pins and can drive a 32Ω receiver driver. With output common-mode setting of 1.65V and RECVDD_33 supply at 3.3V, the receiver driver can drive up to a 1Vrms output signal. With the RECVDD_33 supply at 3.3V, the receiver driver can deliver greater than 128mW into a 32Ω BTL load. If desired, the RECVDD_33 supply can be set to 1.8V, at which the driver can deliver about 40mW into the 32Ω BTL load.

Class-D Speaker Output

The integrated Class-D speaker driver (SPKP/SPKN) is capable of driving an 8Ω differential load. The speaker driver can be powered directly from the power supply (2.7V to 5.5V) on the SVDD pin, however the voltage (including spike voltage) must be limited below the Absolute Maximum Voltage of 6.0V.

The speaker driver is capable of supplying 720 mW at 10% THD+N with a 3.6-V power supply and 1.40W at 10% THD+N with a 5.0V power supply. Separate left and right channels can be sent to the Class-D driver through the Lineout signal path, or from the mixer amplifiers in the ADC bypass. Additionally, the analog mixer before the Speaker amplifier can sum the left and right audio signals for monophonic playback.

ADC / Digital Microphone Interface

The TLV320AIC3263 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter and a programmable miniDSP. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3263 features a large set of options for signal conditioning as well as signal routing:

- 2 ADCs
- 8 analog inputs which can be mixed and/or multiplexed in single-ended and/or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Fine gain adjust of digital channels with 0.1 dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function
- Automatic gain control (AGC)

In addition to the standard set of ADC features the TLV320AIC3263 also offers the following special functions:

- Built in microphone biases
- Four-channel digital microphone interface
 - Allows 4 total microphones
 - Up to 4 digital microphones
 - Up to 2 analog microphones
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive filter mode

ADC Processing Blocks — Overview

The TLV320AIC3263 ADC channel includes a built-in digital decimation filter to process the oversampled data from the to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

ADC Processing Blocks

The TLV320AIC3263 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Decreasing the use of signal-processing capabilities reduces the power consumed by the device. [Table 10](#) gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user programmable coefficients.

Table 10. ADC Processing Blocks

| Processing Blocks | Channel | Decimation Filter | 1st Order IIR Available | Number BiQuads | FIR | Required AOSR Value | Resource Class |
|-----------------------|---------|-------------------|-------------------------|----------------|--------|---------------------|----------------|
| PRB_R1 ⁽¹⁾ | Stereo | A | Yes | 0 | No | 128,64,32,16,8,4 | 7 |
| PRB_R2 | Stereo | A | Yes | 2 | No | 128,64,32,16,8,4 | 8 |
| PRB_R3 | Stereo | A | Yes | 0 | 17-Tap | 128,64,32,16,8,4 | 8 |
| PRB_R4 | Left | A | Yes | 0 | No | 128,64,32,16,8,4 | 4 |
| PRB_R5 | Left | A | Yes | 5 | No | 128,64,32,16,8,4 | 5 |
| PRB_R6 | Left | A | Yes | 0 | 25-Tap | 128,64,32,16,8,4 | 5 |
| PRB_R7 | Stereo | B | Yes | 0 | No | 64,32,16,8,4,2 | 4 |
| PRB_R8 | Stereo | B | Yes | 3 | No | 64,32,16,8,4,2 | 5 |
| PRB_R9 | Stereo | B | Yes | 0 | 17-Tap | 64,32,16,8,4,2 | 5 |
| PRB_R10 | Left | B | Yes | 0 | No | 64,32,16,8,4,2 | 2 |
| PRB_R11 | Left | B | Yes | 3 | No | 64,32,16,8,4,2 | 3 |
| PRB_R12 | Left | B | Yes | 0 | 17-Tap | 64,32,16,8,4,2 | 3 |
| PRB_R13 | Stereo | C | Yes | 0 | No | 32,16,8,4,2,1 | 4 |
| PRB_R14 | Stereo | C | Yes | 5 | No | 32,16,8,4,2,1 | 5 |
| PRB_R15 | Stereo | C | Yes | 0 | 25-Tap | 32,16,8,4,2,1 | 5 |
| PRB_R16 | Left | C | Yes | 0 | No | 32,16,8,4,2,1 | 2 |
| PRB_R17 | Left | C | Yes | 5 | No | 32,16,8,4,2,1 | 3 |
| PRB_R18 | Left | C | Yes | 0 | 25-Tap | 32,16,8,4,2,1 | 3 |
| PRB_R19 | Stereo | A | Yes | 5 | No | 128,64,32,16,8,4 | 9 |
| PRB_R20 | Stereo | A | Yes | 0 | 25-Tap | 128,64,32,16,8,4 | 9 |

(1) Default

For more detailed information see the TLV320AIC3263 Application Reference Guide.

DAC

The TLV320AIC3263 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3263 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3263 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3263 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
 - Usable in single-ended stereo or differential mono mode
 - Analog volume setting with a range of -6 to +14 dB
- 2 line-out amplifiers
 - Usable in single-ended stereo or differential mono mode
- Class-D speaker amplifier
 - Usable with left, right, or monophonic mix modes
 - Analog volume control with a settings of +6, +12, +18, +24, and +30 dB
- 1 Receiver amplifier
 - Usable in mono differential mode
 - Analog volume setting with a range of -6 to +29 dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320AIC3263 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode
- Asynchronous Sample Rate Conversion

DAC Processing Blocks — Overview

The TLV320AIC3263 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. The [Table 11](#) gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 11. Overview – DAC Predefined Processing Blocks

| Processing Block No. | Interpolation Filter | Channel | 1st Order IIR Available | Num. of Biquads | DRC | 3D | Beep Generator | RC Class |
|------------------------------|----------------------|---------|-------------------------|-----------------|-----|-----|----------------|----------|
| <i>PRB_P1</i> ⁽¹⁾ | A | Stereo | No | 2 | No | No | No | 8 |
| PRB_P2 | A | Stereo | Yes | 6 | Yes | No | No | 12 |
| PRB_P3 | A | Stereo | Yes | 6 | No | No | No | 10 |
| PRB_P4 | A | Left | No | 2 | No | No | No | 4 |
| PRB_P5 | A | Left | Yes | 6 | Yes | No | No | 6 |
| PRB_P6 | A | Left | Yes | 6 | No | No | No | 5 |
| PRB_P7 | B | Stereo | Yes | 0 | No | No | No | 6 |
| PRB_P8 | B | Stereo | No | 4 | Yes | No | No | 8 |
| PRB_P9 | B | Stereo | No | 4 | No | No | No | 7 |
| PRB_P10 | B | Stereo | Yes | 6 | Yes | No | No | 10 |
| PRB_P11 | B | Stereo | Yes | 6 | No | No | No | 8 |
| PRB_P12 | B | Left | Yes | 0 | No | No | No | 3 |
| PRB_P13 | B | Left | No | 4 | Yes | No | No | 5 |
| PRB_P14 | B | Left | No | 4 | No | No | No | 4 |
| PRB_P15 | B | Left | Yes | 6 | Yes | No | No | 5 |
| PRB_P16 | B | Left | Yes | 6 | No | No | No | 4 |
| PRB_P17 | C | Stereo | Yes | 0 | No | No | No | 3 |
| PRB_P18 | C | Stereo | Yes | 4 | Yes | No | No | 7 |
| PRB_P19 | C | Stereo | Yes | 4 | No | No | No | 5 |
| PRB_P20 | C | Left | Yes | 0 | No | No | No | 2 |
| PRB_P21 | C | Left | Yes | 4 | Yes | No | No | 4 |
| PRB_P22 | C | Left | Yes | 4 | No | No | No | 3 |
| PRB_P23 | A | Stereo | No | 1 | No | Yes | No | 8 |
| PRB_P24 | A | Stereo | Yes | 3 | Yes | Yes | No | 12 |
| PRB_P25 | A | Stereo | Yes | 1 | Yes | Yes | Yes | 12 |
| PRB_P26 | D | Stereo | No | 0 | No | No | No | 1 |
| PRB_P27 | A | Stereo | Yes | 3 | Yes | Yes | Yes | 13 |

(1) Default

For more detailed information see the TLV320AIC3263 Application Reference Guide.

PowerTune

The TLV320AIC3263 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application.

For more detailed information see the TLV320AIC3263 Application Reference Guide.

Clock Generation and PLL

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output pin and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3263.

The TLV320AIC3263 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks. The clocks for ADC and DAC require source reference clocks, and these clocks can be from a single source or from two separate sources. They can be provided on a variety of device pins such as MCLK, BCLK1, BCLK2, BCLK3, or GPIOx pins. The clocks, ADC_CLKIN and DAC_CLKIN, can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the miniDSP sections. In the event that the desired audio or miniDSP clocks cannot be generated from the reference clocks on MCLK, BCLK1, BCLK2, BCLK3, or GPIOx, the codec also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. The ADC_CLKIN and DAC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the miniDSP sections.

For more detailed information see the TLV320AIC3263 Application Reference Guide.

Interfaces

Control Interfaces

The TLV320AIC3263 control interface supports SPI or I²C communication protocols. For SPI, the SPI_SELECT pin should be tied high; for I²C, SPI_SELECT should be tied low. It is not recommended to change the state of SPI_SELECT during device operation.

I²C Control

The TLV320AIC3263 supports the I²C control protocol, and will respond by default (I2C_ADDR_SCLK grounded) to the 7-bit I²C address of 0011000. With the one I²C address pin, I2C_ADDR_SCLK, the device can be configured to respond to one of two 7-bit I²C addresses, 0011000 or 0011001. The full 8-bit I²C address can be calculated as:

8-Bit I²C Address = "001100" + I2C_ADDR_SCLK + R/W

Example: to write to the TLV320AIC3263 with I2C_ADDR_SCLK = 1 the 8-Bit I²C Address is "001100" + I2C_ADDR_SCLK + R/W = "00110010" = 0x32

I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

SPI Control

In the SPI control mode, the TLV320AIC3263 uses the pins SCL as \overline{SS} , I2C_ADDR_SCLK as SCLK, GPO1 as MISO, SDA as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0) and clock phase setting of 1 (typical microprocessor SPI control bit CPHA = 1). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3263) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the TLV320AIC3263 Application Reference Guide.

Digital Audio Interfaces

The TLV320AIC3263 features three digital audio data serial interfaces, or audio buses. These three interfaces can be run simultaneously, thereby enabling reception and transmission of digital audio from/to three separate devices. A common example of this scenario would be individual connections to an application processor, a communication baseband processor, and a Bluetooth chipset. By utilizing the TLV320AIC3263 as the center of the audio processing in a portable audio system, mixing of voice and music audio is greatly simplified. In addition, the miniDSP can be utilized to greatly enhance the portable device experience by providing advanced audio processing to both communication and media audio streams simultaneously. In addition to the three simultaneous digital audio interfaces, a fourth set of digital audio pins can be muxed into Audio Serial Interface 1. In other words, four separate 4-wire digital audio buses can be connected to the TLV320AIC3263, with up to three of these 4-wire buses receiving and sending digital audio data.

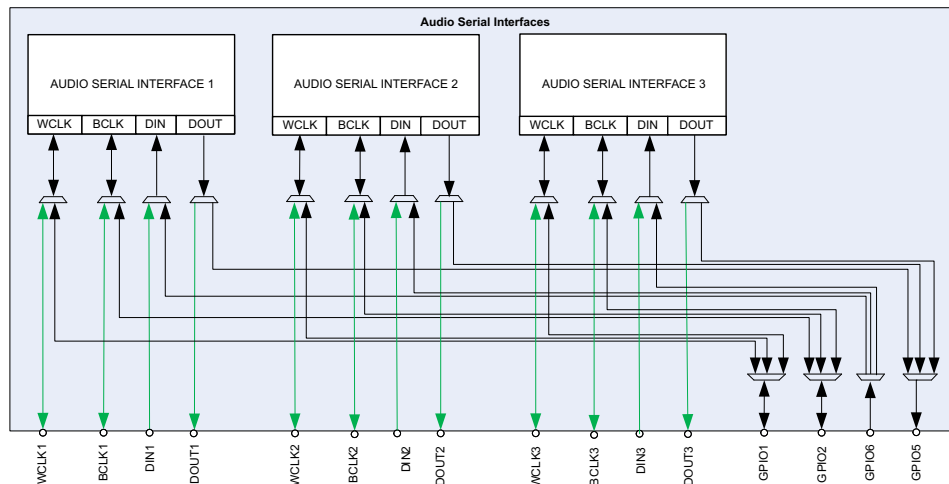


Figure 27. Typical Multiple Connections to Three Audio Serial Interfaces

Each audio bus on the TLV320AIC3263 is very flexible, including left or right-justified data options, support for I²S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

Each of the three audio buses of the TLV320AIC3263 can be configured for left or right-justified, I²S, DSP, or TDM modes of operation, where communication with PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate word clocks.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC3263s may share the same audio bus. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate bit clocks.

The TLV320AIC3263 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clacks.

The TLV320AIC3263 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen.

The TLV320AIC3263 further includes programmability to 3-state the DOUT line during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a 3-state output condition.

By default, when the word-clacks and bit-clacks are generated by the TLV320AIC3263, these clacks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clacks and bit-clacks can be active even when the codec is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clacks are used in the system as general-purpose clacks.

For more detailed information see the TLV320AIC3263 Application Reference Guide.

miniDSP

The TLV320AIC3263 features two fully programmable miniDSP cores. The first miniDSP core is tightly coupled to the ADC, the second miniDSP core is tightly coupled to the DAC. The algorithms for the miniDSP must be loaded into the device after power up. The miniDSPs have direct access to the digital stereo audio stream on the ADC and on the DAC side, offering the possibility for advanced, very-low group delay DSP algorithms. Each miniDSP can run up to 1145 instructions on every audio sample at a 48kHz sample rate. The two cores can run fully synchronized and can exchange data. The TLV320AIC3263 features the ability to process a multitude of algorithms simultaneously. For example, the miniDSPs enable simultaneous noise cancellation, acoustic echo cancellation, sidetone, equalization filtering, dynamic range compression, conversation recording, user-interface sound mixing, and other voice enhancement processing at voice-band sampling rates (such as 8kHz) and high-definition voice sampling rates (such as 16kHz). The TLV320AIC3263 miniDSPs also enable advanced DSP sound enhancement algorithms for an enhanced media experience on a portable audio device.

Software

Software development for the TLV320AIC3263 is supported through TI's comprehensive PurePath Studio Development Environment. A powerful, easy-to-use tool designed specifically to simplify software development on the TLV320AIC3xxx miniDSP audio platform. The Graphical Development Environment consists of a library of common audio functions that can be dragged-and-dropped into an audio signal flow and graphically connected together. The DSP code can then be assembled from the graphical signal flow with the click of a mouse.

For more detailed information see the TLV320AIC3263 Application Reference Guide.

Asynchronous Sample Rate Conversion (ASRC)

For playing back audio/speech signals at various sampling rates, AIC3263 provides an efficient asynchronous sampling rate conversion with the combination of a dedicated ASRC coefficient calculator and the DAC miniDSP engine. The coefficient calculator estimates the audio/speech data input rate versus the DAC playback rate and feeds the calculated coefficients to the miniDSP, with which it converts the audio/speech data to the DAC playback rate. The whole process can be configured automatically without the need of any input sampling rate related information. The input sampling rates as well as the DAC playback rate are not limited to the typical audio/speech sampling rates. A reliable and efficient handshaking is involved between the .

For more detailed information see the TLV320AIC3263 Application Reference Guide.

Power Supply

The TLV320AIC3263 integrates a large amount of digital and analog functionality, and each of these blocks can be powered separately to enable the system to select appropriate power supplies for desired performance and power consumption. The device has separate power domains for digital IO (including three separate digital IO supplies for three separate IOVDD domains), digital core, analog core, analog input, receiver driver, charge-pump input, headphone driver, and speaker driver. If desired, all of the supplies (except for the battery-direct supply for speaker driver and microphone bias) can be connected together and be supplied from one source in the range of 1.65 to 1.95V. Individually, each of the three IOVDD voltages can be supplied in the range of 1.1V to 3.6V. For improved power efficiency, the digital core power supply can range from 1.26V to 1.95V. The analog core voltages (AVDD1_18, AVDD2_18, AVDD4_18, and AVDD_18) can range from 1.5V to 1.95V. The receiver driver supply (RECVDD_33) voltages can range from 1.65V to 3.6V. The charge-pump input voltage (CPVDD_18) can range from 1.26V to 1.95V, and the headphone driver supply (HVDD_18) voltage can range from 1.5V to 1.95V. The speaker driver voltage (SVDD and SPK_V) and microphone bias voltage (MICBIAS_VDD, which is then internally filtered for optimal performance) can range from 2.7V to 5.5V.

For more detailed information see the TLV320AIC3263 Application Reference Guide.

Device Special Functions

The following special functions are available to support advanced system requirements:

- SAR ADC
- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the TLV320AIC3263 Application Reference Guide.

Register Map Summary

Table 12. Summary of Register Map

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|----------|-----------|----------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 0 | 0 | 0x00 | 0x00 | 0x00 | Page Select Register |
| 0 | 0 | 1 | 0x00 | 0x00 | 0x01 | Software Reset Register |
| 0 | 0 | 2-3 | 0x00 | 0x00 | 0x02-0x03 | Reserved Registers |
| 0 | 0 | 4 | 0x00 | 0x00 | 0x04 | Clock Control Register 1, Clock Input Multiplexers |
| 0 | 0 | 5 | 0x00 | 0x00 | 0x05 | Clock Control Register 2, PLL Input Multiplexer |
| 0 | 0 | 6 | 0x00 | 0x00 | 0x06 | Clock Control Register 3, PLL P and R Values |
| 0 | 0 | 7 | 0x00 | 0x00 | 0x07 | Clock Control Register 4, PLL J Value |
| 0 | 0 | 8 | 0x00 | 0x00 | 0x08 | Clock Control Register 5, PLL D Values (MSB) |
| 0 | 0 | 9 | 0x00 | 0x00 | 0x09 | Clock Control Register 6, PLL D Values (LSB) |
| 0 | 0 | 10 | 0x00 | 0x00 | 0x0A | Clock Control Register 7, PLL_CLKIN Divider |
| 0 | 0 | 11 | 0x00 | 0x00 | 0x0B | Clock Control Register 8, NDAC Divider Values |
| 0 | 0 | 12 | 0x00 | 0x00 | 0x0C | Clock Control Register 9, MDAC Divider Values |
| 0 | 0 | 13 | 0x00 | 0x00 | 0x0D | DAC OSR Control Register 1, MSB Value |
| 0 | 0 | 14 | 0x00 | 0x00 | 0x0E | DAC OSR Control Register 2, LSB Value |
| 0 | 0 | 15-17 | 0x00 | 0x00 | 0x0F-0x11 | Reserved Registers |
| 0 | 0 | 18 | 0x00 | 0x00 | 0x12 | Clock Control Register 10, NADC Values |
| 0 | 0 | 19 | 0x00 | 0x00 | 0x13 | Clock Control Register 11, MADC Values |
| 0 | 0 | 20 | 0x00 | 0x00 | 0x14 | ADC Oversampling (AOSR) Register |
| 0 | 0 | 21 | 0x00 | 0x00 | 0x15 | CLKOUT MUX |
| 0 | 0 | 22 | 0x00 | 0x00 | 0x16 | Clock Control Register 12, CLKOUT M Divider Value |
| 0 | 0 | 23 | 0x00 | 0x00 | 0x17 | Timer clock |
| 0 | 0 | 24 | 0x00 | 0x00 | 0x18 | Low Frequency Clock Generation Control |
| 0 | 0 | 25 | 0x00 | 0x00 | 0x19 | High Frequency Clock Generation Control 1 |
| 0 | 0 | 26 | 0x00 | 0x00 | 0x1A | High Frequency Clock Generation Control 2 |
| 0 | 0 | 27 | 0x00 | 0x00 | 0x1B | High Frequency Clock Generation Control 3 |
| 0 | 0 | 28 | 0x00 | 0x00 | 0x1C | High Frequency Clock Generation Control 4 |
| 0 | 0 | 29 | 0x00 | 0x00 | 0x1D | High Frequency Clock Trim Control 1 |
| 0 | 0 | 30 | 0x00 | 0x00 | 0x1E | High Frequency Clock Trim Control 2 |
| 0 | 0 | 31 | 0x00 | 0x00 | 0x1F | High Frequency Clock Trim Control 3 |
| 0 | 0 | 32 | 0x00 | 0x00 | 0x20 | High Frequency Clock Trim Control 4 |
| 0 | 0 | 33-35 | 0x00 | 0x00 | 0x21-0x23 | Reserved Registers |
| 0 | 0 | 36 | 0x00 | 0x00 | 0x24 | ADC Flag Register |
| 0 | 0 | 37 | 0x00 | 0x00 | 0x25 | DAC Flag Register |
| 0 | 0 | 38 | 0x00 | 0x00 | 0x26 | DAC Flag Register |
| 0 | 0 | 39-41 | 0x00 | 0x00 | 0x27-0x29 | Reserved Registers |
| 0 | 0 | 42 | 0x00 | 0x00 | 0x2A | Sticky Flag Register 1 |
| 0 | 0 | 43 | 0x00 | 0x00 | 0x2B | Interrupt Flag Register 1 |
| 0 | 0 | 44 | 0x00 | 0x00 | 0x2C | Sticky Flag Register 2 |
| 0 | 0 | 45 | 0x00 | 0x00 | 0x2D | Sticky Flag Register 3 |
| 0 | 0 | 46 | 0x00 | 0x00 | 0x2E | Interrupt Flag Register 2 |
| 0 | 0 | 47 | 0x00 | 0x00 | 0x2F | Interrupt Flag Register 3 |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|----------|-----------|------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 0 | 48 | 0x00 | 0x00 | 0x30 | INT1 Interrupt Control |
| 0 | 0 | 49 | 0x00 | 0x00 | 0x31 | INT2 Interrupt Control |
| 0 | 0 | 50 | 0x00 | 0x00 | 0x32 | SAR Control 1 |
| 0 | 0 | 51 | 0x00 | 0x00 | 0x33 | Interrupt Format Control Register |
| 0 | 0 | 52-59 | 0x00 | 0x00 | 0x34-0x3B | Reserved Registers |
| 0 | 0 | 60 | 0x00 | 0x00 | 0x3C | DAC Processing Block and miniDSP Power Control |
| 0 | 0 | 61 | 0x00 | 0x00 | 0x3D | ADC Processing Block Control |
| 0 | 0 | 62 | 0x00 | 0x00 | 0x3E | Reserved Register |
| 0 | 0 | 63 | 0x00 | 0x00 | 0x3F | Primary DAC Power and Soft-Stepping Control |
| 0 | 0 | 64 | 0x00 | 0x00 | 0x40 | Primary DAC Master Volume Configuration |
| 0 | 0 | 65 | 0x00 | 0x00 | 0x41 | Primary DAC Left Volume Control Setting |
| 0 | 0 | 66 | 0x00 | 0x00 | 0x42 | Primary DAC Right Volume Control Setting |
| 0 | 0 | 67 | 0x00 | 0x00 | 0x43 | Headset Detection |
| 0 | 0 | 68 | 0x00 | 0x00 | 0x44 | DRC Control Register 1 |
| 0 | 0 | 69 | 0x00 | 0x00 | 0x45 | DRC Control Register 2 |
| 0 | 0 | 70 | 0x00 | 0x00 | 0x46 | DRC Control Register 3 |
| 0 | 0 | 71 | 0x00 | 0x00 | 0x47 | Beep Generator Register 1 |
| 0 | 0 | 72 | 0x00 | 0x00 | 0x48 | Beep Generator Register 2 |
| 0 | 0 | 73 | 0x00 | 0x00 | 0x49 | Beep Generator Register 3 |
| 0 | 0 | 74 | 0x00 | 0x00 | 0x4A | Beep Generator Register 4 |
| 0 | 0 | 75 | 0x00 | 0x00 | 0x4B | Beep Generator Register 5 |
| 0 | 0 | 76 | 0x00 | 0x00 | 0x4C | Beep Sin(x) MSB |
| 0 | 0 | 77 | 0x00 | 0x00 | 0x4D | Beep Sin(x) LSB |
| 0 | 0 | 78 | 0x00 | 0x00 | 0x4E | Beep Cos(x) MSB |
| 0 | 0 | 79 | 0x00 | 0x00 | 0x4F | Beep Cos(x) LSB |
| 0 | 0 | 80 | 0x00 | 0x00 | 0x50 | Reserved Register |
| 0 | 0 | 81 | 0x00 | 0x00 | 0x51 | ADC Channel Power Control |
| 0 | 0 | 82 | 0x00 | 0x00 | 0x52 | ADC Fine Gain Volume Control |
| 0 | 0 | 83 | 0x00 | 0x00 | 0x53 | Left ADC Volume Control |
| 0 | 0 | 84 | 0x00 | 0x00 | 0x54 | Right ADC Volume Control |
| 0 | 0 | 85 | 0x00 | 0x00 | 0x55 | ADC Phase Control |
| 0 | 0 | 86 | 0x00 | 0x00 | 0x56 | Left AGC Control 1 |
| 0 | 0 | 87 | 0x00 | 0x00 | 0x57 | Left AGC Control 2 |
| 0 | 0 | 88 | 0x00 | 0x00 | 0x58 | Left AGC Control 3 |
| 0 | 0 | 89 | 0x00 | 0x00 | 0x59 | Left AGC Attack Time |
| 0 | 0 | 90 | 0x00 | 0x00 | 0x5A | Left AGC Decay Time |
| 0 | 0 | 91 | 0x00 | 0x00 | 0x5B | Left AGC Noise Debounce |
| 0 | 0 | 92 | 0x00 | 0x00 | 0x5C | Left AGC Signal Debounce |
| 0 | 0 | 93 | 0x00 | 0x00 | 0x5D | Left AGC Gain |
| 0 | 0 | 94 | 0x00 | 0x00 | 0x5E | Right AGC Control 1 |
| 0 | 0 | 95 | 0x00 | 0x00 | 0x5F | Right AGC Control 2 |
| 0 | 0 | 96 | 0x00 | 0x00 | 0x60 | Right AGC Control 3 |
| 0 | 0 | 97 | 0x00 | 0x00 | 0x61 | Right AGC Attack Time |
| 0 | 0 | 98 | 0x00 | 0x00 | 0x62 | Right AGC Decay Time |
| 0 | 0 | 99 | 0x00 | 0x00 | 0x63 | Right AGC Noise Debounce |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|----------|-----------|--------------------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 0 | 100 | 0x00 | 0x00 | 0x64 | Right AGC Signal Debounce |
| 0 | 0 | 101 | 0x00 | 0x00 | 0x65 | Right AGC Gain |
| 0 | 0 | 102 | 0x00 | 0x00 | 0x66 | ADC DC Measurement Control Register 1 |
| 0 | 0 | 103 | 0x00 | 0x00 | 0x67 | ADC DC Measurement Control Register 2 |
| 0 | 0 | 104 | 0x00 | 0x00 | 0x68 | Left Channel DC Measurement Output Register 1 (MSB Byte) |
| 0 | 0 | 105 | 0x00 | 0x00 | 0x69 | Left Channel DC Measurement Output Register 2 (Middle Byte) |
| 0 | 0 | 106 | 0x00 | 0x00 | 0x6A | Left Channel DC Measurement Output Register 3 (LSB Byte) |
| 0 | 0 | 107 | 0x00 | 0x00 | 0x6B | Right Channel DC Measurement Output Register 1 (MSB Byte) |
| 0 | 0 | 108 | 0x00 | 0x00 | 0x6C | Right Channel DC Measurement Output Register 2 (Middle Byte) |
| 0 | 0 | 109 | 0x00 | 0x00 | 0x6D | Right Channel DC Measurement Output Register 3 (LSB Byte) |
| 0 | 0 | 110-111 | 0x00 | 0x00 | 0x6E-0x6F | Reserved Registers |
| 0 | 0 | 112 | 0x00 | 0x00 | 0x70 | Digital Microphone 2 Control |
| 0 | 0 | 113-114 | 0x00 | 0x00 | 0x71-0x72 | Reserved Registers |
| 0 | 0 | 115 | 0x00 | 0x00 | 0x73 | I2C Interface Miscellaneous Control |
| 0 | 0 | 116-118 | 0x00 | 0x00 | 0x74-0x76 | Reserved Registers |
| 0 | 0 | 119 | 0x00 | 0x00 | 0x77 | miniDSP Control Register 1, Register Access Control |
| 0 | 0 | 120 | 0x00 | 0x00 | 0x78 | miniDSP Control Register 2, Register Access Control |
| 0 | 0 | 121 | 0x00 | 0x00 | 0x79 | miniDSP Control Register 3, Register Access Control |
| 0 | 0 | 122-126 | 0x00 | 0x00 | 0x7A-0x7E | Reserved Registers |
| 0 | 0 | 127 | 0x00 | 0x00 | 0x7F | Book Selection Register |
| 0 | 1 | 0 | 0x00 | 0x01 | 0x00 | Page Select Register |
| 0 | 1 | 1 | 0x00 | 0x01 | 0x01 | Power Configuration Register |
| 0 | 1 | 2 | 0x00 | 0x01 | 0x02 | Reserved Register |
| 0 | 1 | 3 | 0x00 | 0x01 | 0x03 | Left DAC PowerTune Configuration Register |
| 0 | 1 | 4 | 0x00 | 0x01 | 0x04 | Right DAC PowerTune Configuration Register |
| 0 | 1 | 5-7 | 0x00 | 0x01 | 0x05-0x07 | Reserved Registers |
| 0 | 1 | 8 | 0x00 | 0x01 | 0x08 | Common Mode Register |
| 0 | 1 | 9 | 0x00 | 0x01 | 0x09 | Headphone Output Driver Control |
| 0 | 1 | 10 | 0x00 | 0x01 | 0x0A | Receiver Output Driver Control |
| 0 | 1 | 11 | 0x00 | 0x01 | 0x0B | Headphone Output Driver De-pop Control |
| 0 | 1 | 12 | 0x00 | 0x01 | 0x0C | Receiver Output Driver De-Pop Control |
| 0 | 1 | 13-16 | 0x00 | 0x01 | 0x0D-0x10 | Reserved Registers |
| 0 | 1 | 17 | 0x00 | 0x01 | 0x11 | Mixer Amplifier Control |
| 0 | 1 | 18 | 0x00 | 0x01 | 0x12 | Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control |
| 0 | 1 | 19 | 0x00 | 0x01 | 0x13 | Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control |
| 0 | 1 | 20-21 | 0x00 | 0x01 | 0x14-0x15 | Reserved Registers |
| 0 | 1 | 22 | 0x00 | 0x01 | 0x16 | Lineout Amplifier Control 1 |
| 0 | 1 | 23 | 0x00 | 0x01 | 0x17 | Lineout Amplifier Control 2 |
| 0 | 1 | 24-26 | 0x00 | 0x01 | 0x18-0x1A | Reserved |
| 0 | 1 | 27 | 0x00 | 0x01 | 0x1B | Headphone Amplifier Control 1 |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|----------|-----------|----------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 1 | 28 | 0x00 | 0x01 | 0x1C | Headphone Amplifier Control 2 |
| 0 | 1 | 29 | 0x00 | 0x01 | 0x1D | Headphone Amplifier Control 3 |
| 0 | 1 | 30 | 0x00 | 0x01 | 0x1E | Reserved Register |
| 0 | 1 | 31 | 0x00 | 0x01 | 0x1F | HPL Driver Volume Control |
| 0 | 1 | 32 | 0x00 | 0x01 | 0x20 | HPR Driver Volume Control |
| 0 | 1 | 33 | 0x00 | 0x01 | 0x21 | Charge Pump Control 1 |
| 0 | 1 | 34 | 0x00 | 0x01 | 0x22 | Charge Pump Control 2 |
| 0 | 1 | 35 | 0x00 | 0x01 | 0x23 | Charge Pump Control 3 |
| 0 | 1 | 36 | 0x00 | 0x01 | 0x24 | Receiver Amplifier Control 1 |
| 0 | 1 | 37 | 0x00 | 0x01 | 0x25 | Receiver Amplifier Control 2 |
| 0 | 1 | 38 | 0x00 | 0x01 | 0x26 | Receiver Amplifier Control 3 |
| 0 | 1 | 39 | 0x00 | 0x01 | 0x27 | Receiver Amplifier Control 4 |
| 0 | 1 | 40 | 0x00 | 0x01 | 0x28 | Receiver Amplifier Control 5 |
| 0 | 1 | 41 | 0x00 | 0x01 | 0x29 | Receiver Amplifier Control 6 |
| 0 | 1 | 42 | 0x00 | 0x01 | 0x2A | Receiver Amplifier Control 7 |
| 0 | 1 | 43-44 | 0x00 | 0x01 | 0x2B-0x2C | Reserved Registers |
| 0 | 1 | 45 | 0x00 | 0x01 | 0x2D | Speaker Amplifier Control 1 |
| 0 | 1 | 46 | 0x00 | 0x01 | 0x2E | Speaker Amplifier Control 2 |
| 0 | 1 | 47 | 0x00 | 0x01 | 0x2F | Speaker Amplifier Control 3 |
| 0 | 1 | 48 | 0x00 | 0x01 | 0x30 | Speaker Amplifier Volume Controls |
| 0 | 1 | 49-50 | 0x00 | 0x01 | 0x31-0x32 | Reserved Registers |
| 0 | 1 | 51 | 0x00 | 0x01 | 0x33 | Microphone Bias Control |
| 0 | 1 | 52 | 0x00 | 0x01 | 0x34 | Input Select 1 for Left Microphone PGA P-Terminal |
| 0 | 1 | 53 | 0x00 | 0x01 | 0x35 | Input Select 2 for Left Microphone PGA P-Terminal |
| 0 | 1 | 54 | 0x00 | 0x01 | 0x36 | Input Select for Left Microphone PGA M-Terminal |
| 0 | 1 | 55 | 0x00 | 0x01 | 0x37 | Input Select 1 for Right Microphone PGA P-Terminal |
| 0 | 1 | 56 | 0x00 | 0x01 | 0x38 | Input Select 2 for Right Microphone PGA P-Terminal |
| 0 | 1 | 57 | 0x00 | 0x01 | 0x39 | Input Select for Right Microphone PGA M-Terminal |
| 0 | 1 | 58 | 0x00 | 0x01 | 0x3A | Input Common Mode Control |
| 0 | 1 | 59 | 0x00 | 0x01 | 0x3B | Left Microphone PGA Control |
| 0 | 1 | 60 | 0x00 | 0x01 | 0x3C | Right Microphone PGA Control |
| 0 | 1 | 61 | 0x00 | 0x01 | 0x3D | ADC PowerTune Configuration Register |
| 0 | 1 | 62 | 0x00 | 0x01 | 0x3E | ADC Analog PGA Gain Flag Register |
| 0 | 1 | 63 | 0x00 | 0x01 | 0x3F | DAC Analog Gain Flags Register 1 |
| 0 | 1 | 64 | 0x00 | 0x01 | 0x40 | DAC Analog Gain Flags Register 2 |
| 0 | 1 | 65 | 0x00 | 0x01 | 0x41 | Analog Bypass Gain Flags Register |
| 0 | 1 | 66 | 0x00 | 0x01 | 0x42 | Driver Power-Up Flags Register |
| 0 | 1 | 67-118 | 0x00 | 0x01 | 0x43-0x76 | Reserved Registers |
| 0 | 1 | 119 | 0x00 | 0x01 | 0x77 | Headset Detection Tuning Register 1 |
| 0 | 1 | 120 | 0x00 | 0x01 | 0x78 | Headset Detection Tuning Register 2 |
| 0 | 1 | 121 | 0x00 | 0x01 | 0x79 | Microphone PGA Power-Up Control Register |
| 0 | 1 | 122 | 0x00 | 0x01 | 0x7A | Reference Powerup Delay Register |
| 0 | 1 | 123-127 | 0x00 | 0x01 | 0x7B-0x7F | Reserved Registers |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|----------|-----------|---------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 3 | 0 | 0x00 | 0x03 | 0x00 | Page Select Register |
| 0 | 3 | 1 | 0x00 | 0x03 | 0x01 | Reserved Register |
| 0 | 3 | 2 | 0x00 | 0x03 | 0x02 | Primary SAR ADC Control |
| 0 | 3 | 3 | 0x00 | 0x03 | 0x03 | Primary SAR ADC Conversion Mode |
| 0 | 3 | 4-5 | 0x00 | 0x03 | 0x04-0x05 | Reserved Registers |
| 0 | 3 | 6 | 0x00 | 0x03 | 0x06 | SAR Reference Control |
| 0 | 3 | 7-8 | 0x00 | 0x03 | 0x07-0x08 | Reserved Registers |
| 0 | 3 | 9 | 0x00 | 0x03 | 0x09 | SAR ADC Flags Register 1 |
| 0 | 3 | 10 | 0x00 | 0x03 | 0x0A | SAR ADC Flags Register 2 |
| 0 | 3 | 11-12 | 0x00 | 0x03 | 0x0B-0x0C | Reserved Registers |
| 0 | 3 | 13 | 0x00 | 0x03 | 0x0D | SAR ADC Buffer Mode Control |
| 0 | 3 | 14 | 0x00 | 0x03 | 0x0E | Reserved Register |
| 0 | 3 | 15 | 0x00 | 0x03 | 0x0F | Scan Mode Timer Control |
| 0 | 3 | 16 | 0x00 | 0x03 | 0x10 | Reserved Register |
| 0 | 3 | 17 | 0x00 | 0x03 | 0x11 | SAR ADC Clock Control |
| 0 | 3 | 18 | 0x00 | 0x03 | 0x12 | SAR ADC Buffer Mode Data Read Control |
| 0 | 3 | 19 | 0x00 | 0x03 | 0x13 | SAR ADC Measurement Control |
| 0 | 3 | 20 | 0x00 | 0x03 | 0x14 | Reserved Register |
| 0 | 3 | 21 | 0x00 | 0x03 | 0x15 | SAR ADC Measurement Threshold Flags |
| 0 | 3 | 22 | 0x00 | 0x03 | 0x16 | IN1L Max Threshold Check Control 1 |
| 0 | 3 | 23 | 0x00 | 0x03 | 0x17 | IN1L Max Threshold Check Control 2 |
| 0 | 3 | 24 | 0x00 | 0x03 | 0x18 | IN1L Min Threshold Check Control 1 |
| 0 | 3 | 25 | 0x00 | 0x03 | 0x19 | IN1L Min Threshold Check Control 2 |
| 0 | 3 | 26 | 0x00 | 0x03 | 0x1A | IN1R Max Threshold Check Control 1 |
| 0 | 3 | 27 | 0x00 | 0x03 | 0x1B | IN1R Max Threshold Check Control 2 |
| 0 | 3 | 28 | 0x00 | 0x03 | 0x1C | IN1R Min Threshold Check Control 1 |
| 0 | 3 | 29 | 0x00 | 0x03 | 0x1D | IN1R Min Threshold Check Control 2 |
| 0 | 3 | 30 | 0x00 | 0x03 | 0x1E | TEMP Max Threshold Check Control 1 |
| 0 | 3 | 31 | 0x00 | 0x03 | 0x1F | TEMP Max Threshold Check Control 2 |
| 0 | 3 | 32 | 0x00 | 0x03 | 0x20 | TEMP Min Threshold Check Control 1 |
| 0 | 3 | 33 | 0x00 | 0x03 | 0x21 | TEMP Min Threshold Check Control 2 |
| 0 | 3 | 34-53 | 0x00 | 0x03 | 0x22-0x35 | Reserved Registers |
| 0 | 3 | 54 | 0x00 | 0x03 | 0x36 | IN1L Measurement Data (MSB) |
| 0 | 3 | 55 | 0x00 | 0x03 | 0x37 | IN1L Measurement Data (LSB) |
| 0 | 3 | 56 | 0x00 | 0x03 | 0x38 | IN1R Measurement Data (MSB) |
| 0 | 3 | 57 | 0x00 | 0x03 | 0x39 | IN1R Measurement Data (LSB) |
| 0 | 3 | 58 | 0x00 | 0x03 | 0x3A | VBAT Measurement Data (MSB) |
| 0 | 3 | 59 | 0x00 | 0x03 | 0x3B | VBAT Measurement Data (LSB) |
| 0 | 3 | 60-65 | 0x00 | 0x03 | 0x3C-0x41 | Reserved Registers |
| 0 | 3 | 66 | 0x00 | 0x03 | 0x42 | TEMP1 Measurement Data (MSB) |
| 0 | 3 | 67 | 0x00 | 0x03 | 0x43 | TEMP1 Measurement Data (LSB) |
| 0 | 3 | 68 | 0x00 | 0x03 | 0x44 | TEMP2 Measurement Data (MSB) |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|----------|-----------|-------------------------------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 3 | 69 | 0x00 | 0x03 | 0x45 | TEMP2 Measurement Data (LSB) |
| 0 | 3 | 70-127 | 0x00 | 0x03 | 0x46-0x7F | Reserved Registers |
| 0 | 4 | 0 | 0x00 | 0x04 | 0x00 | Page Select Register |
| 0 | 4 | 1 | 0x00 | 0x04 | 0x01 | Audio Serial Interface 1, Audio Bus Format Control Register |
| 0 | 4 | 2 | 0x00 | 0x04 | 0x02 | Audio Serial Interface 1, Left Ch_Offset_1 Control Register |
| 0 | 4 | 3 | 0x00 | 0x04 | 0x03 | Audio Serial Interface 1, Right Ch_Offset_2 Control Register |
| 0 | 4 | 4 | 0x00 | 0x04 | 0x04 | Audio Serial Interface 1, Channel Setup Register |
| 0 | 4 | 5 | 0x00 | 0x04 | 0x05 | Audio Serial Interface 1, ADC Audio Bus Format Control Register |
| 0 | 4 | 6 | 0x00 | 0x04 | 0x06 | Audio Serial Interface 1, Multi-Channel Setup Register 2 |
| 0 | 4 | 7 | 0x00 | 0x04 | 0x07 | Audio Serial Interface 1, ADC Input Control |
| 0 | 4 | 8 | 0x00 | 0x04 | 0x08 | Audio Serial Interface 1, DAC Output Control |
| 0 | 4 | 9 | 0x00 | 0x04 | 0x09 | Audio Serial Interface 1, Control Register 9, ADC Slot Tristate Control |
| 0 | 4 | 10 | 0x00 | 0x04 | 0x0A | Audio Serial Interface 1, WCLK and BCLK Control Register |
| 0 | 4 | 11 | 0x00 | 0x04 | 0x0B | Audio Serial Interface 1, Bit Clock N Divider Input Control |
| 0 | 4 | 12 | 0x00 | 0x04 | 0x0C | Audio Serial Interface 1, Bit Clock N Divider |
| 0 | 4 | 13 | 0x00 | 0x04 | 0x0D | Audio Serial Interface 1, Word Clock N Divider |
| 0 | 4 | 14 | 0x00 | 0x04 | 0x0E | Audio Serial Interface 1, BCLK and WCLK Output |
| 0 | 4 | 15 | 0x00 | 0x04 | 0x0F | Audio Serial Interface 1, Data Output |
| 0 | 4 | 16 | 0x00 | 0x04 | 0x10 | Audio Serial Interface 1, ADC WCLK and BCLK Control |
| 0 | 4 | 17 | 0x00 | 0x04 | 0x11 | Audio Serial Interface 2, Audio Bus Format Control Register |
| 0 | 4 | 18 | 0x00 | 0x04 | 0x12 | Audio Serial Interface 2, Data Offset Control Register |
| 0 | 4 | 19-20 | 0x00 | 0x04 | 0x13-0x14 | Reserved Registers |
| 0 | 4 | 21 | 0x00 | 0x04 | 0x15 | Audio Serial Interface 2, ADC Audio Bus Format Control Register |
| 0 | 4 | 22 | 0x00 | 0x04 | 0x16 | Reserved Register |
| 0 | 4 | 23 | 0x00 | 0x04 | 0x17 | Audio Serial Interface 2, ADC Input Control |
| 0 | 4 | 24 | 0x00 | 0x04 | 0x18 | Audio Serial Interface 2, DAC Output Control |
| 0 | 4 | 25 | 0x00 | 0x04 | 0x19 | Reserved Register |
| 0 | 4 | 26 | 0x00 | 0x04 | 0x1A | Audio Serial Interface 2, WCLK and BCLK Control Register |
| 0 | 4 | 27 | 0x00 | 0x04 | 0x1B | Audio Serial Interface 2, Bit Clock N Divider Input Control |
| 0 | 4 | 28 | 0x00 | 0x04 | 0x1C | Audio Serial Interface 2, Bit Clock N Divider |
| 0 | 4 | 29 | 0x00 | 0x04 | 0x1D | Audio Serial Interface 2, Word Clock N Divider |
| 0 | 4 | 30 | 0x00 | 0x04 | 0x1E | Audio Serial Interface 2, BCLK and WCLK Output |
| 0 | 4 | 31 | 0x00 | 0x04 | 0x1F | Audio Serial Interface 2, Data Output |
| 0 | 4 | 32 | 0x00 | 0x04 | 0x20 | Audio Serial Interface 2, ADC WCLK and BCLK Control |
| 0 | 4 | 33 | 0x00 | 0x04 | 0x21 | Audio Serial Interface 3, Audio Bus Format Control Register |
| 0 | 4 | 34 | 0x00 | 0x04 | 0x22 | Audio Serial Interface 3, Data Offset Control Register |
| 0 | 4 | 35-36 | 0x00 | 0x04 | 0x23-0x24 | Reserved Registers |
| 0 | 4 | 37 | 0x00 | 0x04 | 0x25 | Audio Serial Interface 3, ADC Audio Bus Format Control Register |
| 0 | 4 | 38 | 0x00 | 0x04 | 0x26 | Reserved Register |
| 0 | 4 | 39 | 0x00 | 0x04 | 0x27 | Audio Serial Interface 3, ADC Input Control |
| 0 | 4 | 40 | 0x00 | 0x04 | 0x28 | Audio Serial Interface 3, DAC Output Control |
| 0 | 4 | 41 | 0x00 | 0x04 | 0x29 | Reserved Register |
| 0 | 4 | 42 | 0x00 | 0x04 | 0x2A | Audio Serial Interface 3, WCLK and BCLK Control Register |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|----------|-----------|--------------------------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 4 | 43 | 0x00 | 0x04 | 0x2B | Audio Serial Interface 3, Bit Clock N Divider Input Control |
| 0 | 4 | 44 | 0x00 | 0x04 | 0x2C | Audio Serial Interface 3, Bit Clock N Divider |
| 0 | 4 | 45 | 0x00 | 0x04 | 0x2D | Audio Serial Interface 3, Word Clock N Divider |
| 0 | 4 | 46 | 0x00 | 0x04 | 0x2E | Audio Serial Interface 3, BCLK and WCLK Output |
| 0 | 4 | 47 | 0x00 | 0x04 | 0x2F | Audio Serial Interface 3, Data Output |
| 0 | 4 | 48 | 0x00 | 0x04 | 0x30 | Audio Serial Interface 3, ADC WCLK and BCLK Control |
| 0 | 4 | 49 | 0x00 | 0x04 | 0x31 | Audio Serial Interface 1, L1/R1 Input Control |
| 0 | 4 | 50 | 0x00 | 0x04 | 0x32 | Audio Serial Interface 1, L2/R2 Input Control |
| 0 | 4 | 51 | 0x00 | 0x04 | 0x33 | Audio Serial Interface 1, L3/R3 Input Control |
| 0 | 4 | 52 | 0x00 | 0x04 | 0x34 | Audio Serial Interface 1, L4/R4 Input Control |
| 0 | 4 | 53 | 0x00 | 0x04 | 0x35 | Audio Serial Interface 2, WCLK and BCLK Input Multiplexers Control |
| 0 | 4 | 54 | 0x00 | 0x04 | 0x36 | Audio Serial Interface 2, DIN Input Multiplexer Control |
| 0 | 4 | 55 | 0x00 | 0x04 | 0x37 | Audio Serial Interface 3, WCLK and BCLK Input Multiplexers Control |
| 0 | 4 | 56 | 0x00 | 0x04 | 0x38 | Audio Serial Interface 3, DIN Input Multiplexer Control |
| 0 | 4 | 57-64 | 0x00 | 0x04 | 0x39-0x40 | Reserved Registers |
| 0 | 4 | 65 | 0x00 | 0x04 | 0x41 | WCLK1 (Input/Output) Pin Control |
| 0 | 4 | 66 | 0x00 | 0x04 | 0x42 | Reserved Register |
| 0 | 4 | 67 | 0x00 | 0x04 | 0x43 | DOUT1 (Output) Pin Control |
| 0 | 4 | 68 | 0x00 | 0x04 | 0x44 | DIN1 (Input) Pin Control |
| 0 | 4 | 69 | 0x00 | 0x04 | 0x45 | WCLK2 (Input/Output) Pin Control |
| 0 | 4 | 70 | 0x00 | 0x04 | 0x46 | BCLK2 (Input/Output) Pin Control |
| 0 | 4 | 71 | 0x00 | 0x04 | 0x47 | DOUT2 (Output) Pin Control |
| 0 | 4 | 72 | 0x00 | 0x04 | 0x48 | DIN2 (Input) Pin Control |
| 0 | 4 | 73 | 0x00 | 0x04 | 0x49 | WCLK3 (Input/Output) Pin Control |
| 0 | 4 | 74 | 0x00 | 0x04 | 0x4A | BCLK3 (Input/Output) Pin Control |
| 0 | 4 | 75 | 0x00 | 0x04 | 0x4B | DOUT3 (Output) Pin Control |
| 0 | 4 | 76 | 0x00 | 0x04 | 0x4C | DIN3 (Input) Pin Control |
| 0 | 4 | 77-85 | 0x00 | 0x04 | 0x4D-0x55 | Reserved Registers |
| 0 | 4 | 86 | 0x00 | 0x04 | 0x56 | GPIO1 (Input/Output) Pin Control |
| 0 | 4 | 87 | 0x00 | 0x04 | 0x57 | GPIO2 (Input/Output) Pin Control |
| 0 | 4 | 88 | 0x00 | 0x04 | 0x58 | GPIO3 (Input/Output) Pin Control |
| 0 | 4 | 89 | 0x00 | 0x04 | 0x59 | GPIO4 (Input/Output) Pin Control |
| 0 | 4 | 90 | 0x00 | 0x04 | 0x5A | GPIO5 (Input/Output) Pin Control |
| 0 | 4 | 91 | 0x00 | 0x04 | 0x5B | GPIO6 (Input/Output) Pin Control |
| 0 | 4 | 92-95 | 0x00 | 0x04 | 0x5C-0x5F | Reserved Registers |
| 0 | 4 | 96 | 0x00 | 0x04 | 0x60 | GPO1 (Output) Pin Control |
| 0 | 4 | 97-99 | 0x00 | 0x04 | 0x61-0x63 | Reserved Registers |
| 0 | 4 | 100 | 0x00 | 0x04 | 0x64 | Digital Microphone Clock Control |
| 0 | 4 | 101 | 0x00 | 0x04 | 0x65 | Digital Microphone 1 Input Pin Control |
| 0 | 4 | 102 | 0x00 | 0x04 | 0x66 | Digital Microphone 2 Input Pin Control |
| 0 | 4 | 103 | 0x00 | 0x04 | 0x67 | Reserved Register |
| 0 | 4 | 104 | 0x00 | 0x04 | 0x68 | Bit-Bang Output |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|-----------|-----------|--------------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 0 | 4 | 105-106 | 0x00 | 0x04 | 0x69-0x6A | Reserved Registers |
| 0 | 4 | 107 | 0x00 | 0x04 | 0x6B | Bit-Bang Input |
| 0 | 4 | 108-112 | 0x00 | 0x04 | 0x6C-0x70 | Reserved Registers |
| 0 | 4 | 113 | 0x00 | 0x04 | 0x71 | Bit-Bang miniDSP Output Control |
| 0 | 4 | 114 | 0x00 | 0x04 | 0x72 | Reserved Register |
| 0 | 4 | 115 | 0x00 | 0x04 | 0x73 | Audio Serial Interface 1, ADC BCLK and ADC WCLK Output |
| 0 | 4 | 116 | 0x00 | 0x04 | 0x74 | Audio Serial Interface 2, ADC BCLK and ADC WCLK Output |
| 0 | 4 | 117 | 0x00 | 0x04 | 0x75 | Audio Serial Interface 3, ADC BCLK and ADC WCLK Output |
| 0 | 4 | 118 | 0x00 | 0x04 | 0x76 | miniDSP Data Port Control |
| 0 | 4 | 119 | 0x00 | 0x04 | 0x77 | Digital Audio Engine Synchronization Control |
| 0 | 4 | 120-127 | 0x00 | 0x04 | 0x78-0x7F | Reserved Registers |
| 0 | 252 | 0 | 0x00 | 0xFC | 0x00 | Page Select Register |
| 0 | 252 | 1 | 0x00 | 0xFC | 0x01 | SAR Buffer Mode Data (MSB) and Buffer Flags |
| 0 | 252 | 2 | 0x00 | 0xFC | 0x02 | SAR Buffer Mode Data (LSB) |
| 0 | 252 | 3-127 | 0x00 | 0xFC | 0x03-0x7F | Reserved Registers |
| 20 | 0 | 0 | 0x14 | 0x00 | 0x00 | Page Select Register |
| 20 | 0 | 1-126 | 0x14 | 0x00 | 0x01-0x7E | Reserved Registers |
| 20 | 0 | 127 | 0x14 | 0x00 | 0x7F | Book Selection Register |
| 20 | 1-26 | 0 | 0x14 | 0x01-0x1A | 0x00 | Page Select Register |
| 20 | 1-26 | 1-7 | 0x14 | 0x01-0x1A | 0x01-0x07 | Reserved Registers |
| 20 | 1-26 | 8-127 | 0x14 | 0x01-0x1A | 0x08-0x7F | ADC Fixed Coefficients C(0:767) |
| 40 | 0 | 0 | 0x28 | 0x00 | 0x00 | Page Select Register |
| 40 | 0 | 1 | 0x28 | 0x00 | 0x01 | ADC Adaptive CRAM Configuration Register |
| 40 | 0 | 2-126 | 0x28 | 0x00 | 0x02-0x7E | Reserved Registers |
| 40 | 0 | 127 | 0x28 | 0x00 | 0x7F | Book Selection Register |
| 40 | 1-17 | 0 | 0x28 | 0x01-0x11 | 0x00 | Page Select Register |
| 40 | 1-17 | 1-7 | 0x28 | 0x01-0x11 | 0x01-0x07 | Reserved Registers |
| 40 | 1-17 | 8-127 | 0x28 | 0x01-0x11 | 0x08-0x7F | ADC Adaptive Coefficients C(0:509) |
| 40 | 18 | 0 | 0x28 | 0x12 | 0x00 | Page Select Register |
| 40 | 18 | 1-7 | 0x28 | 0x12 | 0x01-0x07 | Reserved Registers |
| 40 | 18 | 8-15 | 0x28 | 0x12 | 0x08-0x0F | ADC Adaptive Coefficients C(510:511) |
| 40 | 18 | 16-127 | 0x28 | 0x12 | 0x10-0x7F | Reserved Registers |
| 60 | 0 | 0 | 0x3C | 0x00 | 0x00 | Page Select Register |
| 60 | 0 | 1-126 | 0x3C | 0x00 | 0x01-0x7E | Reserved Registers |
| 60 | 0 | 127 | 0x3C | 0x00 | 0x7F | Book Selection Register |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|-----------|-----------|---------------------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 60 | 1-35 | 0 | 0x3C | 0x01-0x23 | 0x00 | Page Select Register |
| 60 | 1-35 | 1-7 | 0x3C | 0x01-0x23 | 0x01-0x07 | Reserved Registers |
| 60 | 1-35 | 8-127 | 0x3C | 0x01-0x23 | 0x08-0x7F | DAC Fixed Coefficients C(0:1023) |
| 80 | 0 | 0 | 0x50 | 0x00 | 0x00 | Page Select Register |
| 80 | 0 | 1 | 0x50 | 0x00 | 0x01 | DAC Adaptive Coefficient Bank #1 Configuration Register |
| 80 | 0 | 2-126 | 0x50 | 0x00 | 0x02-0x7E | Reserved Registers |
| 80 | 0 | 127 | 0x50 | 0x00 | 0x7F | Book Selection Register |
| 80 | 1-17 | 0 | 0x50 | 0x01-0x11 | 0x00 | Page Select Register |
| 80 | 1-17 | 1-7 | 0x50 | 0x01-0x11 | 0x01-0x07 | Reserved Registers |
| 80 | 1-17 | 8-127 | 0x50 | 0x01-0x11 | 0x08-0x7F | DAC Adaptive Coefficient Bank #1 C(0:509) |
| 80 | 18 | 0 | 0x50 | 0x12 | 0x00 | Page Select Register |
| 80 | 18 | 1-7 | 0x50 | 0x12 | 0x01-0x07 | Reserved Registers |
| 80 | 18 | 8-15 | 0x50 | 0x12 | 0x08-0x0F | DAC Adaptive Coefficient Bank #1 C(510:511) |
| 80 | 18 | 16-127 | 0x50 | 0x12 | 0x10-0x7F | Reserved Registers |
| 82 | 0 | 0 | 0x52 | 0x00 | 0x00 | Page Select Register |
| 82 | 0 | 1 | 0x52 | 0x00 | 0x01 | DAC Adaptive Coefficient Bank #2 Configuration Register |
| 82 | 0 | 2-126 | 0x52 | 0x00 | 0x02-0x7E | Reserved Registers |
| 82 | 0 | 127 | 0x52 | 0x00 | 0x7F | Book Selection Register |
| 82 | 1-17 | 0 | 0x52 | 0x01-0x11 | 0x00 | Page Select Register |
| 82 | 1-17 | 1-7 | 0x52 | 0x01-0x11 | 0x01-0x07 | Reserved Registers |
| 82 | 1-17 | 8-127 | 0x52 | 0x01-0x11 | 0x08-0x7F | DAC Adaptive Coefficient Bank #2 C(0:509) |
| 82 | 18 | 0 | 0x52 | 0x12 | 0x00 | Page Select Register |
| 82 | 18 | 1-7 | 0x52 | 0x12 | 0x01-0x07 | Reserved Registers |
| 82 | 18 | 8-15 | 0x52 | 0x12 | 0x08-0x0F | DAC Adaptive Coefficient Bank #2 C(510:511) |
| 82 | 18 | 16-127 | 0x52 | 0x12 | 0x10-0x7F | Reserved Registers |
| 100 | 0 | 0 | 0x64 | 0x00 | 0x00 | Page Select Register |
| 100 | 0 | 1-46 | 0x64 | 0x00 | 0x01-0x2E | Reserved Registers |
| 100 | 0 | 47 | 0x64 | 0x00 | 0x2F | Non-Programmable Override Options |
| 100 | 0 | 48 | 0x64 | 0x00 | 0x30 | ADC miniDSP_A Instruction Control Register 1 |
| 100 | 0 | 49 | 0x64 | 0x00 | 0x31 | ADC miniDSP_A Instruction Control Register 2 |
| 100 | 0 | 50 | 0x64 | 0x00 | 0x32 | ADC miniDSP_A CIC Input and Decimation Ratio Control Register |
| 100 | 0 | 51-56 | 0x64 | 0x00 | 0x33-0x38 | Reserved Registers |
| 100 | 0 | 57 | 0x64 | 0x00 | 0x39 | ADC miniDSP_A Instruction Control Register 3 |

Table 12. Summary of Register Map (continued)

| Decimal | | | Hex | | | DESCRIPTION |
|----------|----------|----------|----------|-----------|-----------|-----------------------------------------------------|
| BOOK NO. | PAGE NO. | REG. NO. | BOOK NO. | PAGE NO. | REG. NO. | |
| 100 | 0 | 58 | 0x64 | 0x00 | 0x3A | ADC miniDSP_A ISR Interrupt Control |
| 100 | 0 | 59 | 0x64 | 0x00 | 0x3B | Reserved Registers |
| 100 | 0 | 60 | 0x64 | 0x00 | 0x3C | ADC miniDSP_A Secondary CIC Input Control |
| 100 | 0 | 61 | 0x64 | 0x00 | 0x3D | miniDSP_A to Audio Serial Interface Handoff Control |
| 100 | 0 | 62-126 | 0x64 | 0x00 | 0x3E-0x7E | Reserved Registers |
| 100 | 0 | 127 | 0x64 | 0x00 | 0x7F | Book Selection Register |
| 100 | 1-52 | 0 | 0x64 | 0x01-0x34 | 0x00 | Page Select Register |
| 100 | 1-52 | 1-7 | 0x64 | 0x01-0x34 | 0x01-0x07 | Reserved Registers |
| 100 | 1-52 | 8-127 | 0x64 | 0x01-0x34 | 0x08-0x7F | miniDSP_A Instructions |
| 120 | 0 | 0 | 0x78 | 0x00 | 0x00 | Page Select Register |
| 120 | 0 | 1-46 | 0x78 | 0x00 | 0x01-0x2E | Reserved Registers |
| 120 | 0 | 47 | 0x78 | 0x00 | 0x2F | Non-Programmable Override Options |
| 120 | 0 | 48 | 0x78 | 0x00 | 0x30 | DAC miniDSP_D Instruction Control Register 1 |
| 120 | 0 | 49 | 0x78 | 0x00 | 0x31 | DAC miniDSP_D Instruction Control Register 2 |
| 120 | 0 | 50 | 0x78 | 0x00 | 0x32 | DAC miniDSP_D Interpolation Factor Control Register |
| 120 | 0 | 51-56 | 0x78 | 0x00 | 0x33-0x38 | Reserved Registers |
| 120 | 0 | 57 | 0x78 | 0x00 | 0x39 | DAC miniDSP_D Instruction Control Register 3 |
| 120 | 0 | 58 | 0x78 | 0x00 | 0x3A | DAC miniDSP_D ISR Interrupt Control |
| 120 | 0 | 59-126 | 0x78 | 0x00 | 0x3B-0x7E | Reserved Registers |
| 120 | 0 | 127 | 0x78 | 0x00 | 0x7F | Book Selection Register |
| 120 | 1-103 | 0 | 0x78 | 0x01-0x67 | 0x00 | Page Select Register |
| 120 | 1-103 | 1-7 | 0x78 | 0x01-0x67 | 0x01-0x07 | Reserved Registers |
| 120 | 1-103 | 8-127 | 0x78 | 0x01-0x67 | 0x08-0x7F | miniDSP_D Instructions |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|----------------|
| TLV320AIC3263IYZFR | ACTIVE | DSBGA | YZF | 81 | 2500 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | AIC32AA | Samples |
| TLV320AIC3263IYZFT | ACTIVE | DSBGA | YZF | 81 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | AIC32AA | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV320AIC3263IYZFR | DSBGA | YZF | 81 | 2500 | 330.0 | 12.4 | 5.04 | 5.07 | 0.75 | 8.0 | 12.0 | Q1 |
| TLV320AIC3263IYZFT | DSBGA | YZF | 81 | 250 | 330.0 | 12.4 | 5.04 | 5.07 | 0.75 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

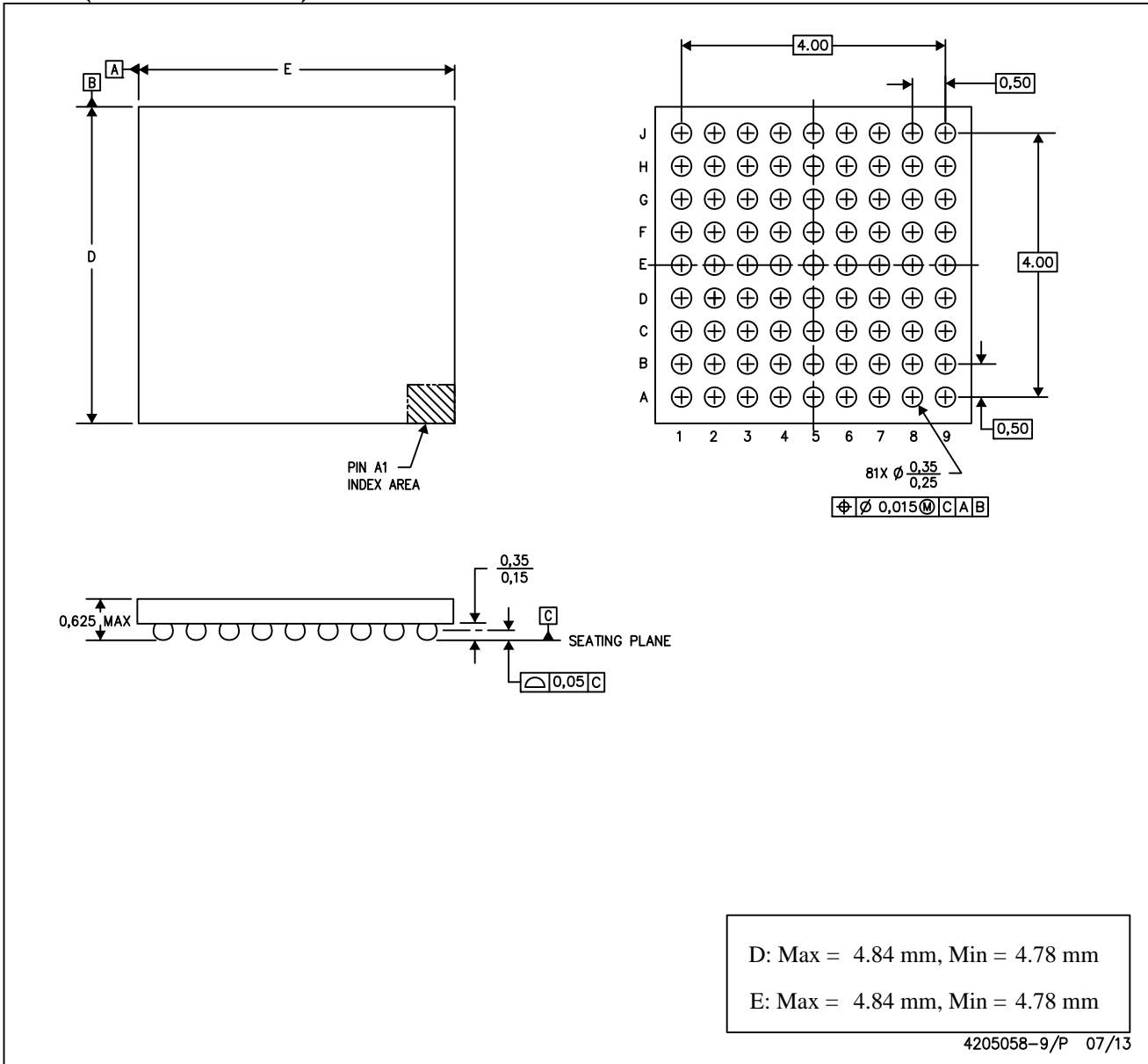


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV320AIC3263IYZFR | DSBGA | YZF | 81 | 2500 | 335.0 | 335.0 | 25.0 |
| TLV320AIC3263IYZFT | DSBGA | YZF | 81 | 250 | 335.0 | 335.0 | 25.0 |

YZF (R-XBGA-N81)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

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