Application Note

TAS2x63QFN Schematic and Layout Guidelines

ABSTRACT

Updated PCB captures display improved GND connection on Pin 28

In audio applications, it is always important to minimize the noise effects that may be induced by external conditions or even by the same components of the PCB. All the audio amplifiers require a clean and stable power supply to get the best performance. Any noise issue at the power supplies may be the cause of a high THD+N and SNR levels. In addition, the analog inputs and outputs require good noise immunity against the digital activity from nearby devices.

This document describes an optimized layout for the TAS2x63 device in mono configuration. The goal of utilizing these layout guidelines is to minimize the noise issues and ensure the best device performance.

The TAS2x63EVM was taken as reference for the suggested guidelines.

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1 Layout Guidelines

1.1 Typical Application Circuit

Figure 1-1 shows the typical application block diagram for TAS2563 device.

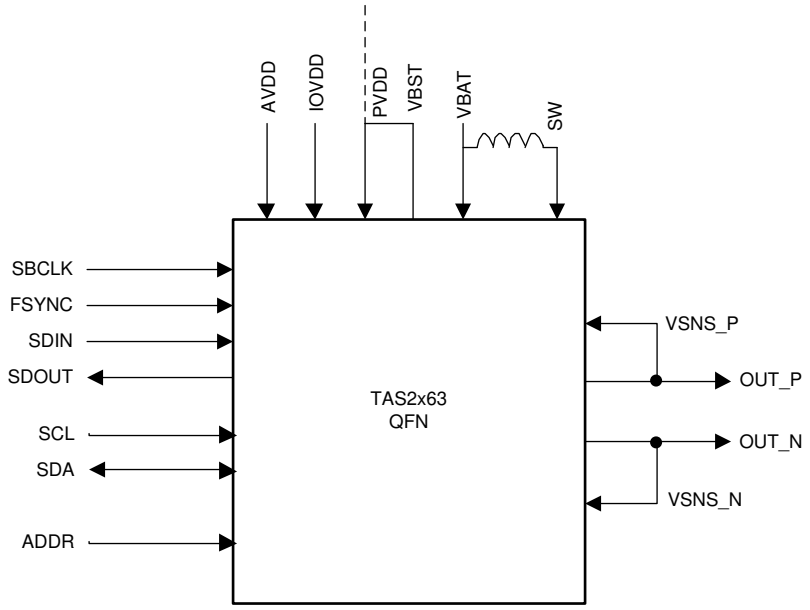

Figure 1-1. TAS2x63 Block Diagram

Figure 1-2 and Figure 1-3 show the components location of the PCBA reference layout.

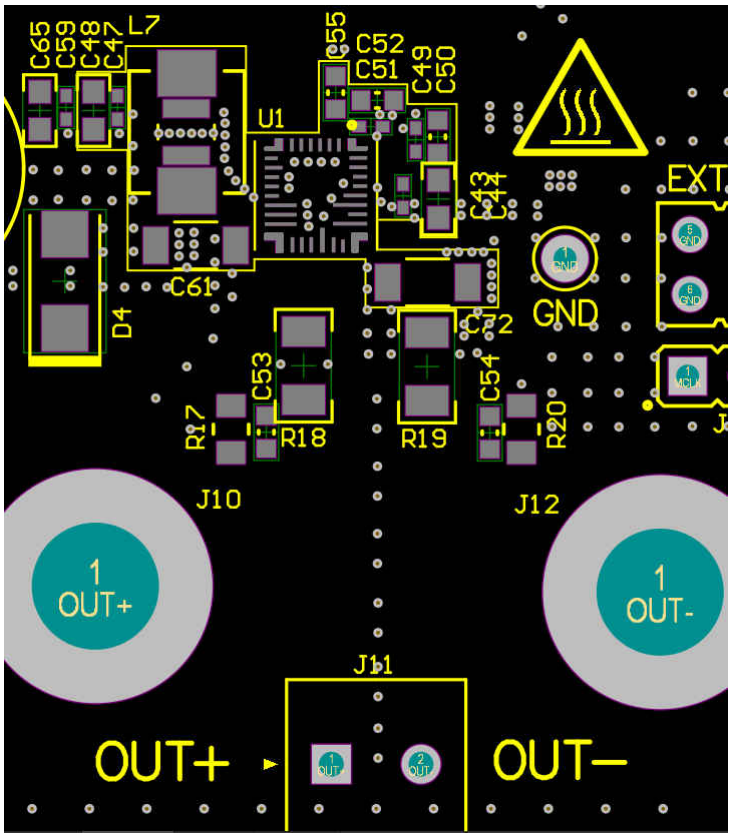

Figure 1-2. TAS2x63EVM Component Locations

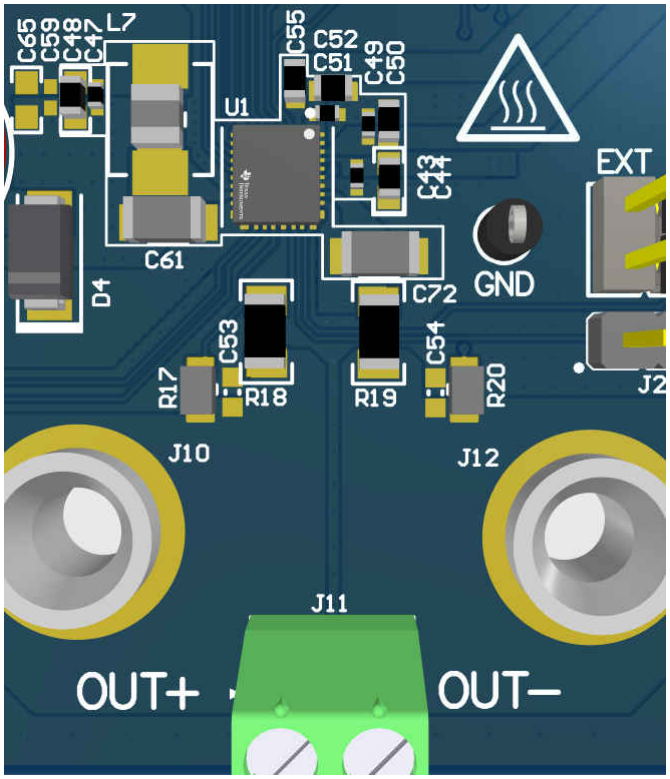

Figure 1-3. TAS2x63EVM Component Locations (3D View)

1.2 VBAT

VBAT is the battery power supply input. It carries a considerable amount of current when the internal boost is used. VBAT trace can be separated in two, one trace that supplies the boost inductor (high current) and another trace that supplies the VBAT pin from the device (low current). Each termination of the VBAT supply must be decoupled thus decoupling capcaitors must be placed next to both the boost inductor and the VBAT pin from the IC.

At least a 0.1uF and 10uF must be used to bypass VBAT to GND close to the boost inductor, and at leat a 1uF must be used to bypass VBAT to GND close to the VBAT pin from the IC.

It is important to consider the following recommendations for VBAT:

- Include additional bulk capacitors to reduce overall THD+N at high power, most important hen using low VBAT voltage levels.
- Use wide traces for VBAT to handle the total output power.
- Do not use vias between the devie pin, inductor terminal and related capacitors.

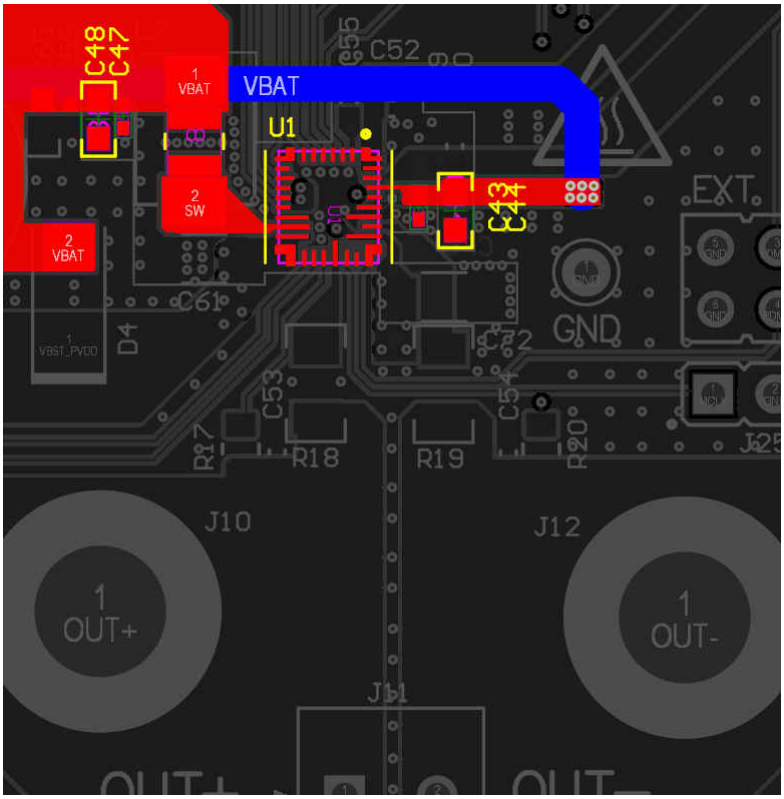

Figure 1-4. VBAT Connection

1.3 DREG

DREG is the digital core voltage regulator output. This pin must be bypassed to GND with a 1-µF capacitor and it must not be connected to an external load. TI recommends ensuring that both decoupling capacitor ends see as low inductance as possible between this DREG pin and GND. Multiple vias are suggested to reduce the inductance. See the Decoupling Capacitors section for details.

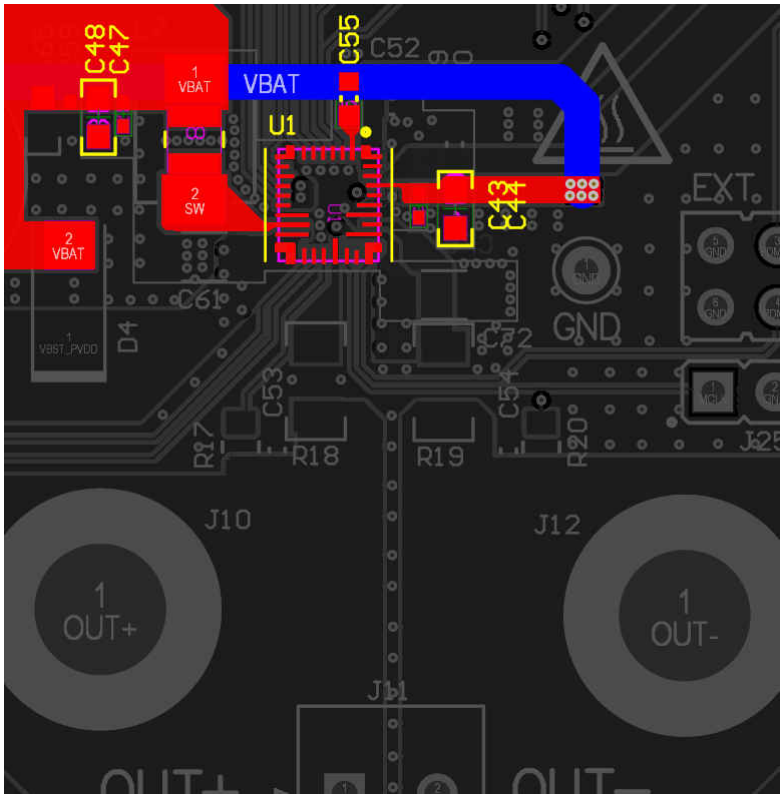

Figure 1-5. DREG Connection

1.4 GREG

The GREG pin is the output of the high-side gate charge-pump regulator. This pin must not be connected to an external load. A minimum of a 0.1-µF capacitor must be connected from the GREG pin to the PVDD pin (see Figure 1-6, for details).

TI recommends verifying that the PCB design does not generate a parasitic inductance higher than 200 pH. In addition, it is important to connect the GREG pin capacitor to PVDD with a star connection and not to the boost plane. This practice reduces the possibility of EMI radiation.

Similar to the ground pin connections, the layer changes should use multiple vias to minimize the parasitic inductance.

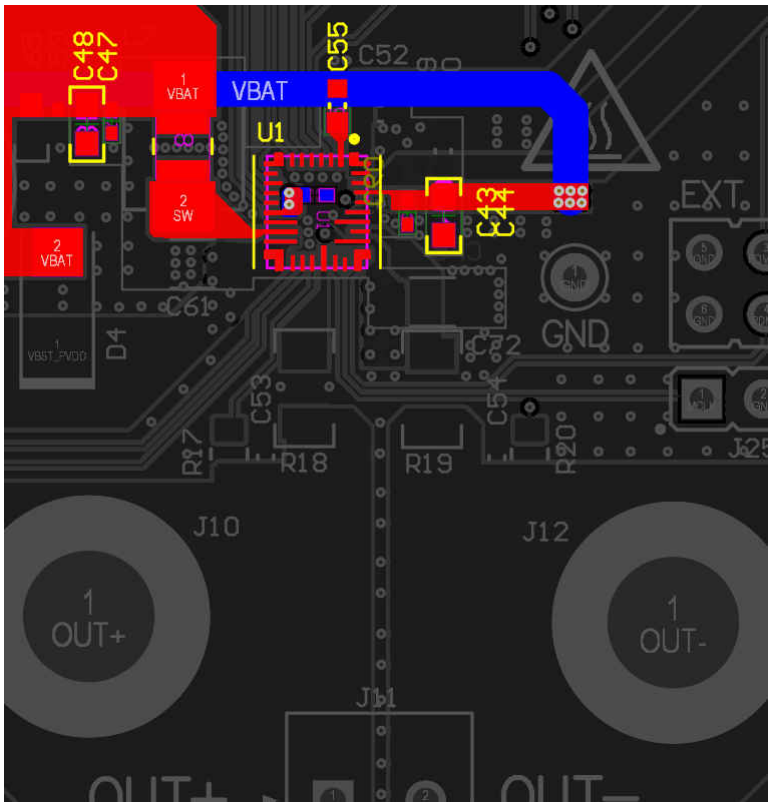

Figure 1-6. GREG Connection

1.5 PVDD and VBST

VBST is the internal boost converter output. This is the pin that will supply the power stage supply pin (PVDD). PVDD must be shorted to the VBST pin using a strong connection.

There are a few considerations that must be taken into account for the PVDD to VBST connection:

- VBST must not be connected to an external load. This pin should be bypassed to GND with decoupling capacitors. The decoupling capacitor ends should see as low an inductance as possible between the VBST pin and the BGND pin. See the LINK for details.
- There should be a maximum parasitic inductance of 100 pH from the device pin to decoupling.
- VBST should be connected to PVDD through a thick plane (use multiple vias to reduce parasitic inductance).
- PVDD should be connected with a star connection to the GREG capacitor.
- VBST and PVDD traces carry a high amount of current. The traces should support currents up to the device overcurrent limit.
- Boost capacitor derating should satisfy the ratio with boost inductor: L/C < 1/3 • Ceramic capacitors derate with the applied DC voltage. Often, a 10-µF capacitor loses 80% of the nominal value at the 10-V to 12-V range (for example, a 10-µF capacitance value would result in 2 µF). Typically, TI recommends using a 20-µF capacitor (or a pair of two 10-µF capacitors) as decoupling capacitor.

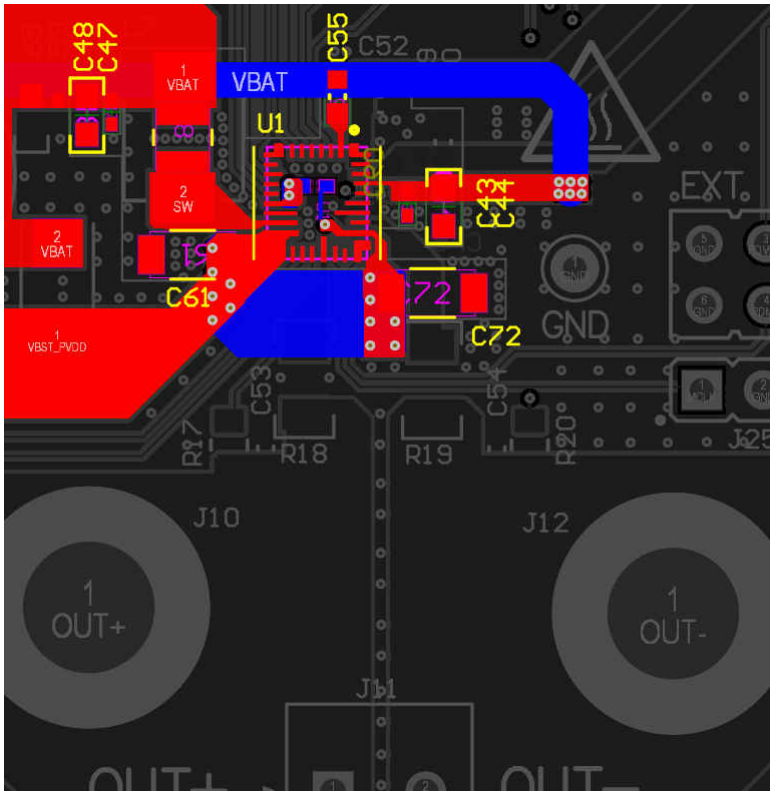

Figure 1-7. PVDD and VBST Connection

1.6 VDD

VDD is the analog and digital power supply input. Similar to the VBAT pin, this power pin requires a decoupling capacitor. A minimum of 4.7-µF capacitor is suggested to bypass VDD to GND. See the Decoupling Capacitors section for details.

This pin requires having a maximum parasitic inductance of 200 pH.

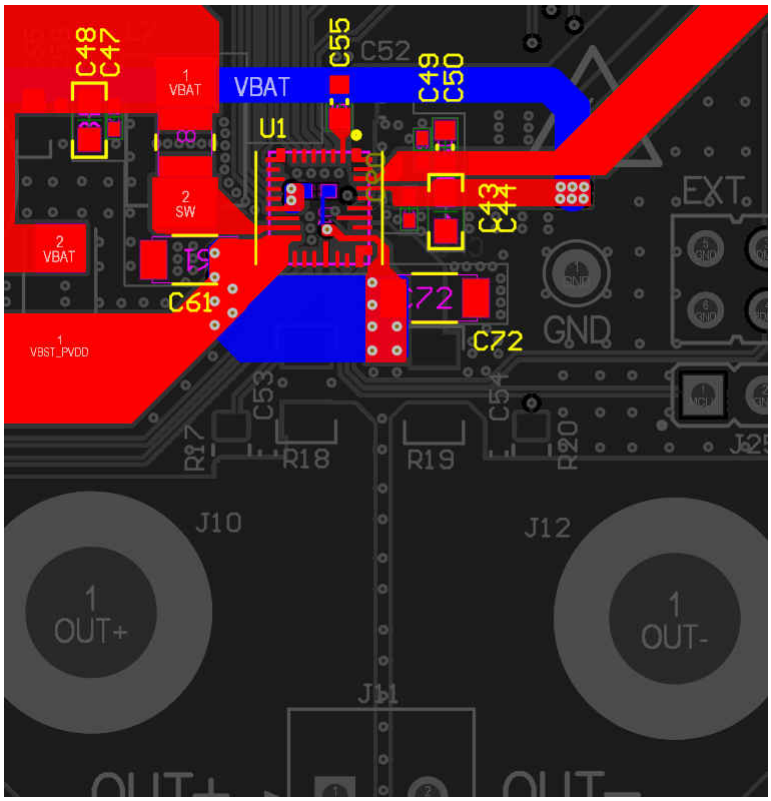

Figure 1-8. VDD Connection

1.7 IOVDD

Similar to VDD, IOVDD is the I/O power supplyinput. It requires decoupling capacitor. A minimum of 1-µF capacitor is suggested to bypass VDD to GND. See the Decoupling Capacitors section for details.

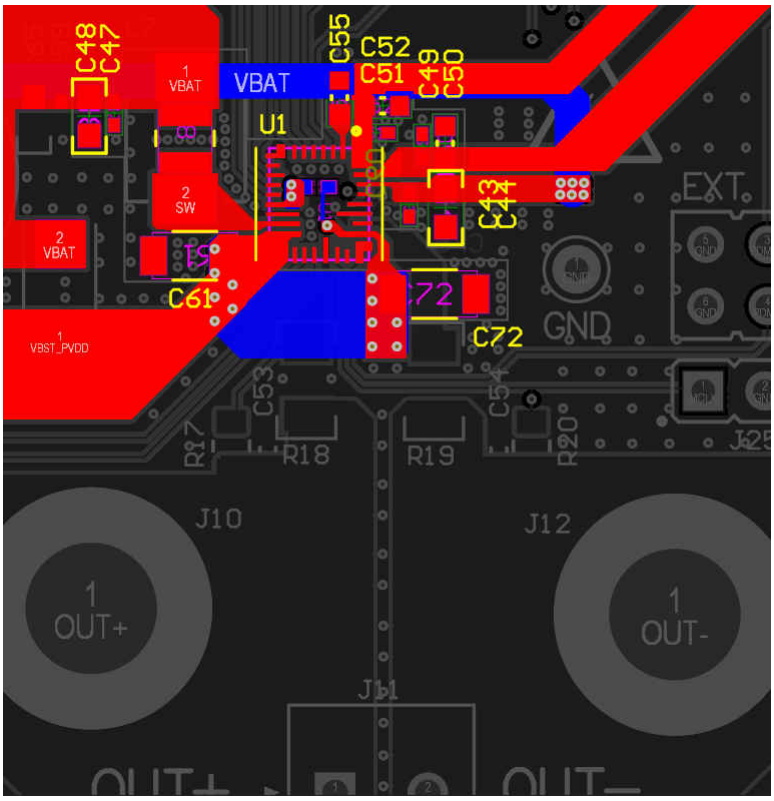

Figure 1-9. IOVDD Connection

1.8 Output Pins

OUT_N and OUT_P are the Class-D channel negative and positive output, respectively. Due to its switching nature, TI recommends keeping the routing short to limit the emissions.

For optimal current flow, the PCB traces must be widened near to the output pins. In addition, the outputs need to be routed on two layers using several vias to minimize parasitic impedance.

It is important to consider a few things when using an EMI filter (LC array):

- Inductance should be the first element in the filter.
- Capacitance to GND or other output will pull high-current spikes capable of triggering overcurrent protection.
- TI recommends fixing 1.5 MHz as the lower limit of the corner frequency to simplify the filter debug and noise issues.
- Place 1kΩ resistors in series to VSNS pins to prevent higher current spikes damaging the sense pins internal structure.

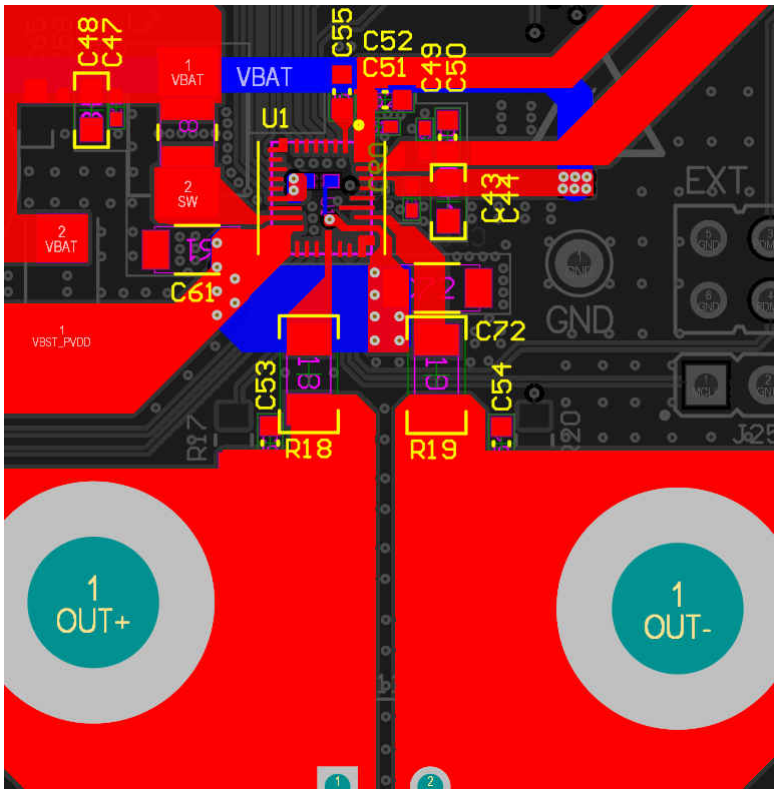

Figure 1-10. OUT_P and OUT_N Connections

1.9 Sense Pins

VSNS_N and VSNS_P are the voltage sense negative and positive inputs, respectively. These inputs are connected to the Class-D outputs (VSNS_N to OUT_N and VSNS_P to OUT_P) after the ferrite bead filter.

When routing these pins to the ferrite bead filter, it is necessary to the make the connection to its respective output at the speaker terminal, not to a pin or trace. In addition, TI recommends adding a 1-kΩ resistor for each voltage sense path. This practice helps to reduce emissions and reduce ICN increments that result from the EMI filter.

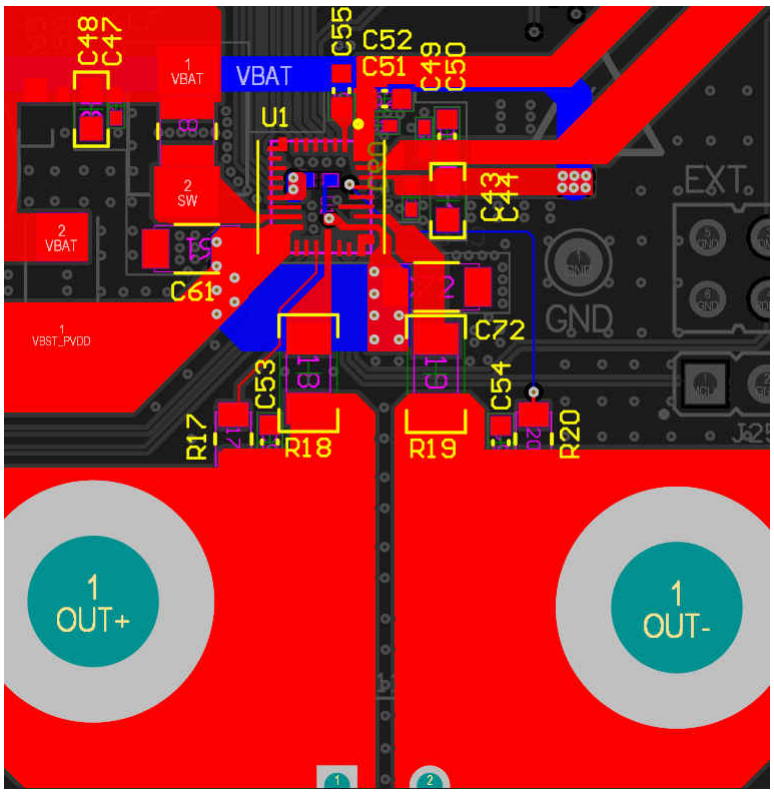

Figure 1-11. VSNS_P and VSNS_N Connections

1.10 Digital Portion

The TAS2563 device involves digital and analog activity. Care must be taken when routing the different signals since it may result in noise issues, especially from the digital lines to the analog portion.

The digital lines can reach frequencies up to 1 MHz for the I^2C lines in Fast-Mode Plus and up to 50 MHz for the I^2S lines. This high-frequency content can affect the performance of the analog signals. For measurement purposes, the digital noise level may affect the scope captures or a THD+N measurement.

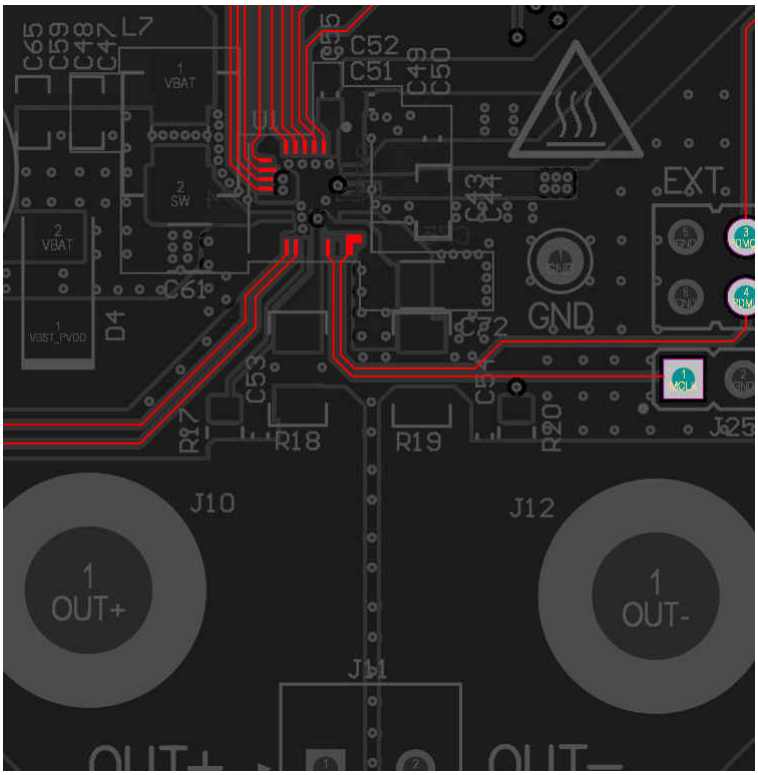

Figure 1-12. Digital Conections

1.11 Ground Planes

The ground plane routing is important when designing the PCB layout. These planes must be designed to have a proper thermal dissipation and minimize the parasitic impedance as much as possible. Design tips for the different ground pins are listed here:

- GND pin 28 must be treated like a signal, and connected to GND separately through a via. Do not pour GND plane over pins 27 and 28 together.
- All other ground pins must be shorted below the package and connected to the PCB ground plane through multiple vias.
- The vias are the best way to carry heat from the different sections in the board. Since the GND plane will need to quickly dissipate all the elevated temperatures, it is necessary to add multiple vias close to the ground pins.
- A maximum 150 pH of parasitic inductance is recommended. Having many vias reduces the additional impedance and provides good conduction in both electrical and thermal perspective.
- An entire layer immediately below the top layer must be dedicated to GND, as best practice.

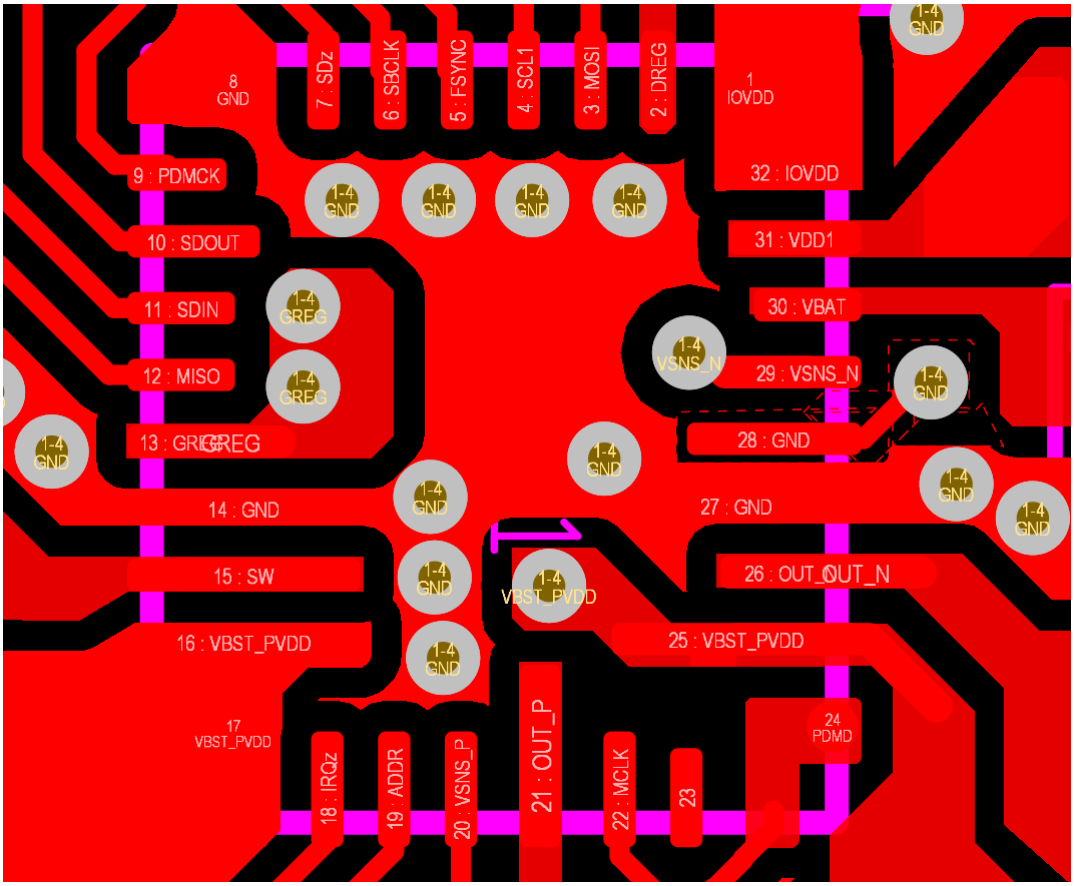

Figure 1-13. GND Pin 28

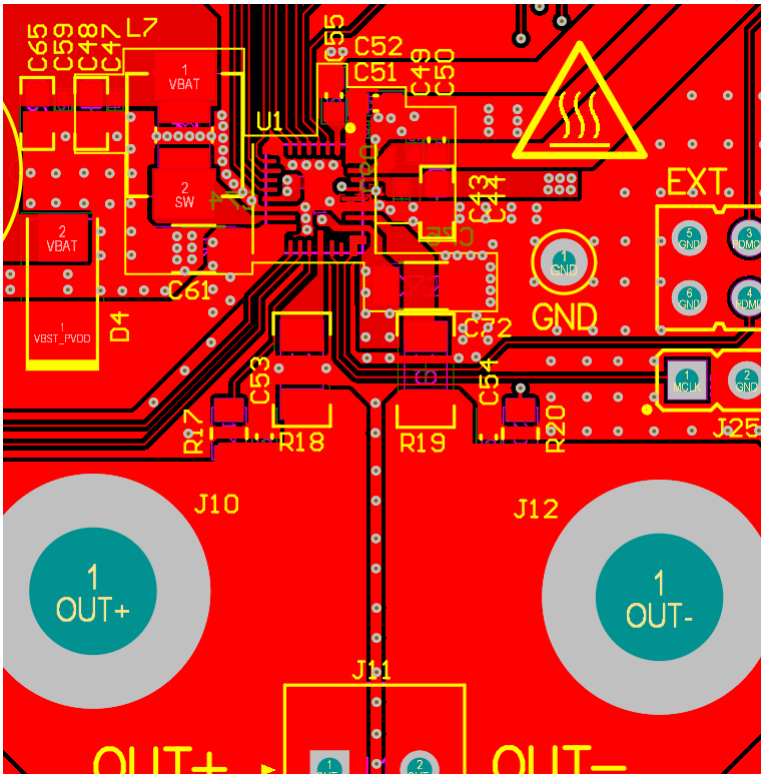

Figure 1-14. TAS2x63 Top Layer

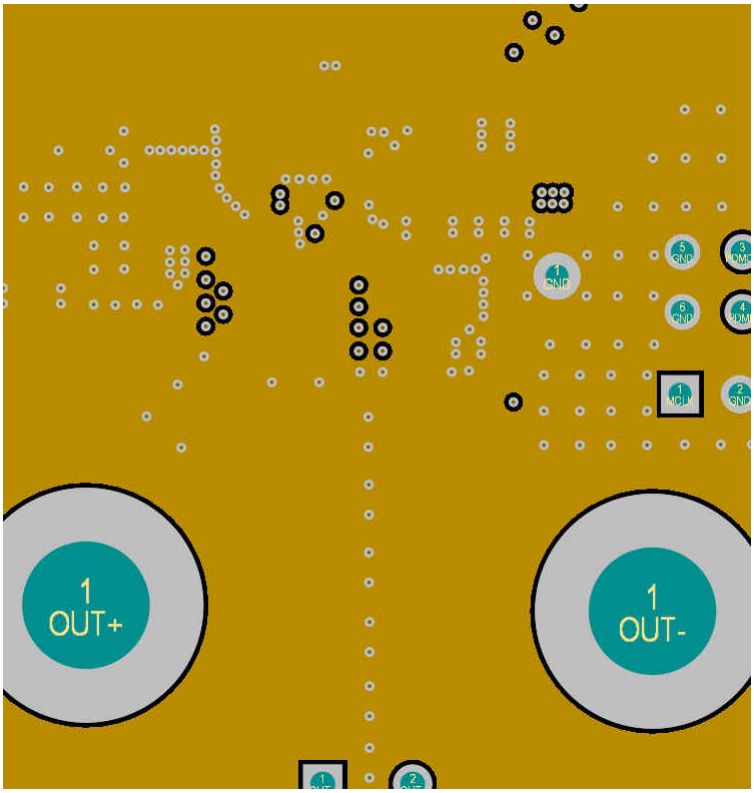

Figure 1-15. TAS2x63 Layer 2

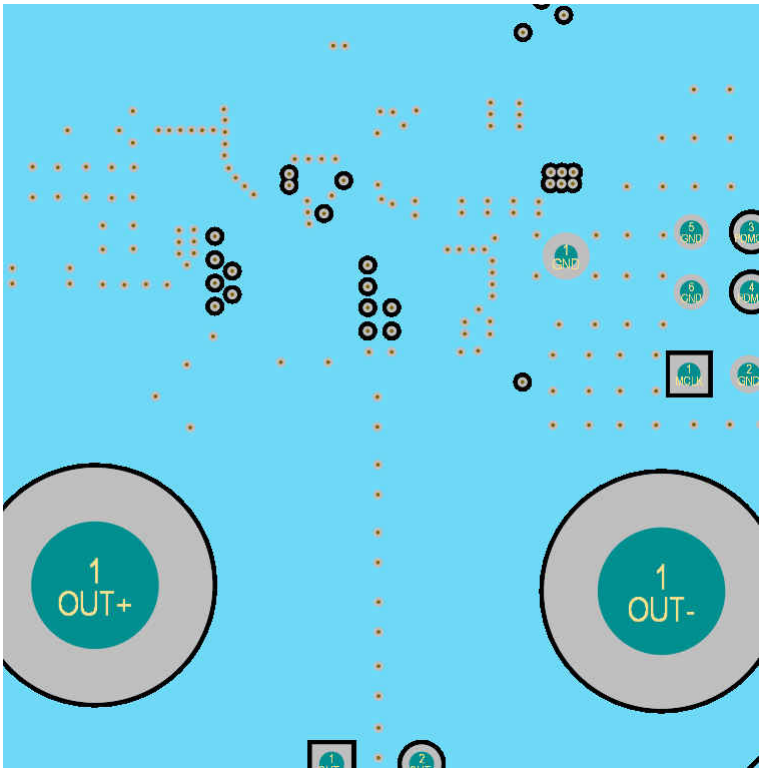

Figure 1-16. TAS2x63 Layer 3

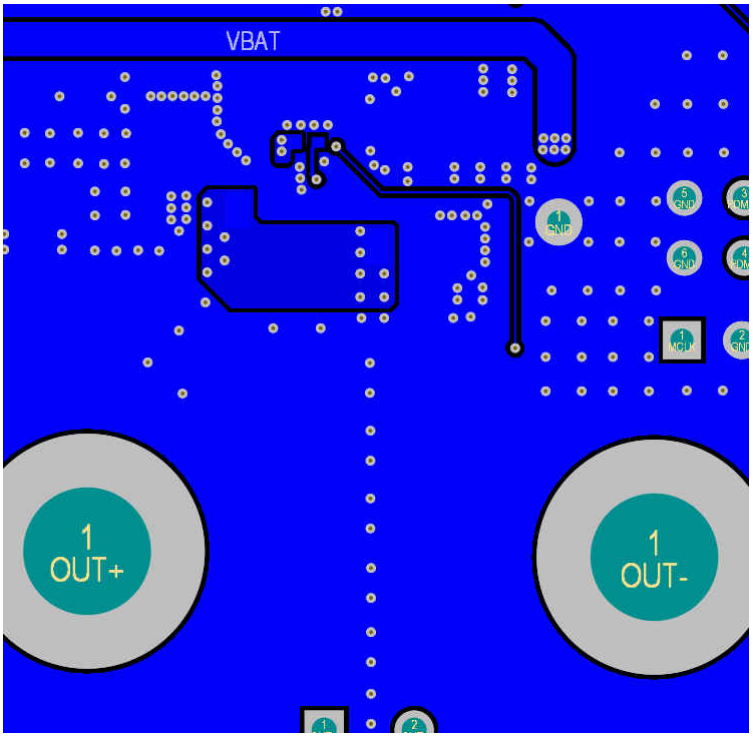

Figure 1-17. TAS2x63 Bottom Layer

2 Schematic

Figure 2-1 shows the typical application circuit for the TAS2563 with the components names used in this document.

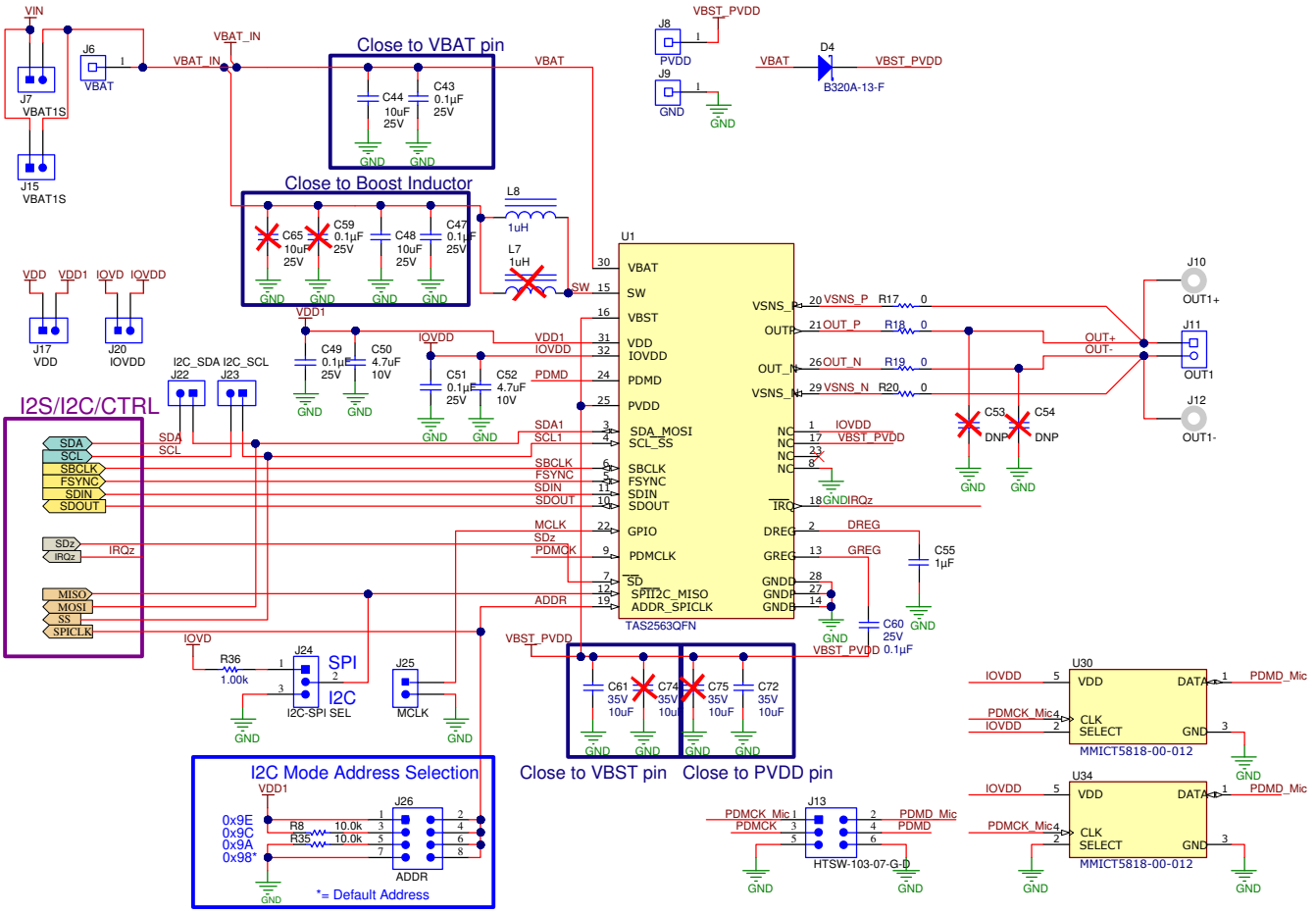

Figure 2-1. TAS2x63 Schematic

2.1 Recommended External Components

Component	Description	Specification	MIN	TYP	MAX	Unit
C43, C44	VBAT Decoupling Capacitor - VBAT pin	Type	X7R			
		Capacitance, 20% Tolerance	10, 0.1			µF
		Rated Voltage	10			V
C47, C48	VBAT Decoupling Capacitor - Boost inductor	Type	X7R			
		Capacitance, 20% Tolerance	10, 0.1			µF
		Rated Voltage	10			V
C61, C72	PVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20%	10			µF
		Rated Voltage	35			V
C49, C50	VDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	4.7			µF
		Rated Voltage	6			V
C55	DREG Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	0.68	1	1.5	µF
		Rated Voltage	6			V
C51, C52	IOVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	1			µF
		Rated Voltage	6			V
C60	GREG Decoupling Capacito	Type	X7R			
		Capacitance, 20% Tolerance	0.1			uF
		Rated Voltage	10			V
Replace R18 and R19 by these inductors in case the EMI Filter is required	EMI Filter Inductors (optional). These are not recommended as it degrades THD+N performance. The device is a filter-less Class-D and does not require these bead inductors.	Impedance at 100 MHz		120		Ω
		DC Resistance			0.095	Ω
		DC Current	5			A
C53, C54	EMI Filter Capacitors (optional, must use EMI inductors if C37, C49, C106, C115 used)	Capacitance		1		nF

3 Decoupling Capacitors

All the PCB routes have defined impedance that must be considered during all design stages. These signal paths will act as additional components in the board. In addition, the PCB lines have a parasitic inductance and capacitance that result in a different power distribution.

To reduce the negative effects of all these parasitic impedances, TI recommends that the VBAT and VDD decoupling capacitor connections respect the following rules:

- **Place the decoupling capacitor close to the device pin in the same layer.** The decoupling capacitor stores local charge and supplies the large transient currents when it is required. The TAS2563 device has many switching activity and voltage fluctuations that demand large current transients in a short period of time. In addition, the parasitic effects caused by the vias, traces, and pads generate a voltage drop in the power supply. The proximity of the decoupling capacitors to the power pins compensates these effects and supplies the large transient currents when it is required. On a multi-layer board, the capacitors must be placed in the same layer where the TAS2563 device is located. Otherwise, the decoupling capacitor value may be reduced by the additional capacitance due to the vias connections.
- **Place the VDD and GND vias as close as possible to the decoupling capacitors.** If possible, place the vias directly or as close as possible to the capacitor mounting pads. The vias have defined impedance determined by its length and diameter. This impedance may cause a voltage drop (in highfrequency applications the signal integrity is greatly influenced) and a current flow that must be reduced or avoided. For that reason, TI recommends adding many vias around the mounting pads. This practice reduces the parasitic impedance.

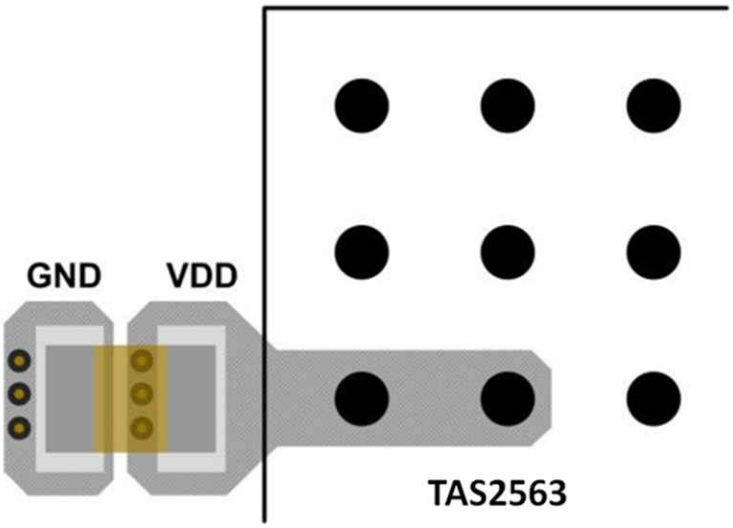

Figure 3-1. Decoupling Capacitor

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (January 2022)	Page
• Updated PCB captures display, improved GND connection on pin 28	1
• Add pin 28 description in Section 1.11	13
• Added Figure 1-13, GND Pin 28	13

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