Application Report

How to Use External PVDD Configuration

ABSTRACT

The Texas Instruments boosted smart amplifiers TAS2563, TAS2562 and TAS2110 have highly versatile operation modes. These devices can operate with the power output stage supplied by the internal boost, or from a higher external voltage rail connected directly to the PVDD pin.

This document covers the hardware and power sequence requirements to use an external PVDD source, as well as example of its operation and configuration including a comparison of using internal boost versus an external PVDD source.

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Trademarks

1 Introduction

Some systems are powered from 2S or 3S batteries, which mean there is a voltage source higher than usual 5 V for VBAT power. In these cases the overall system efficiency may be impacted by using the integrated boost as voltage source would be stepped-down to ~5 V and then internal boost raises it again to ~11.5 V.

In order to support all kind of applications, our boosted smart amplifiers are capable of using either the internal boost or an external higher voltage directly connected to PVDD; this allows customer applications to save some cost and decreases the total solution size when using external PVDD.

2 Hardware Requirements for External PVDD

The recommended power sequence, exposed in Section 4 of this document, suggests that VBAT is powered up before PVDD; this is to prevent reverse bias on the internal circuitry connecting these two potentials. However, forward biasing this internal circuitry must be considered as well. Powering up VBAT while PVDD is not present will cause the voltage from VBAT to forward bias the internal circuitry and charge up the decoupling capacitors next to PVDD pins.

Depending on the amount of capacitance on the PVDD side, the current flowing through the internal circuitry varies. The higher the capacitance, the higher the current peak will be when capacitors are initially charged. Following the EVM design with 10~20 uF capacitors would cause a peak current of ~2.5 A to flow inside the device. This current would not damage the device, however if capacitance increases the current can be as high as ~7 A for 330 uF capacitance on PVDD.

In order to prevent damage due to high current during forward bias from VBAT to PVDD, an external diode can be placed between these power connections. The anode of the diode connects to VBAT and cathode to PVDD, and its current rating is chosen based on PVDD capacitance, as mentioned above.

Additional changes from using internal boost compared to external PVDD are related to the boost passive components:

- Boost inductor is not required and can be removed.
- Decoupling capacitance close to the inductor is not required and can be removed.
- SW pin should be left floating.

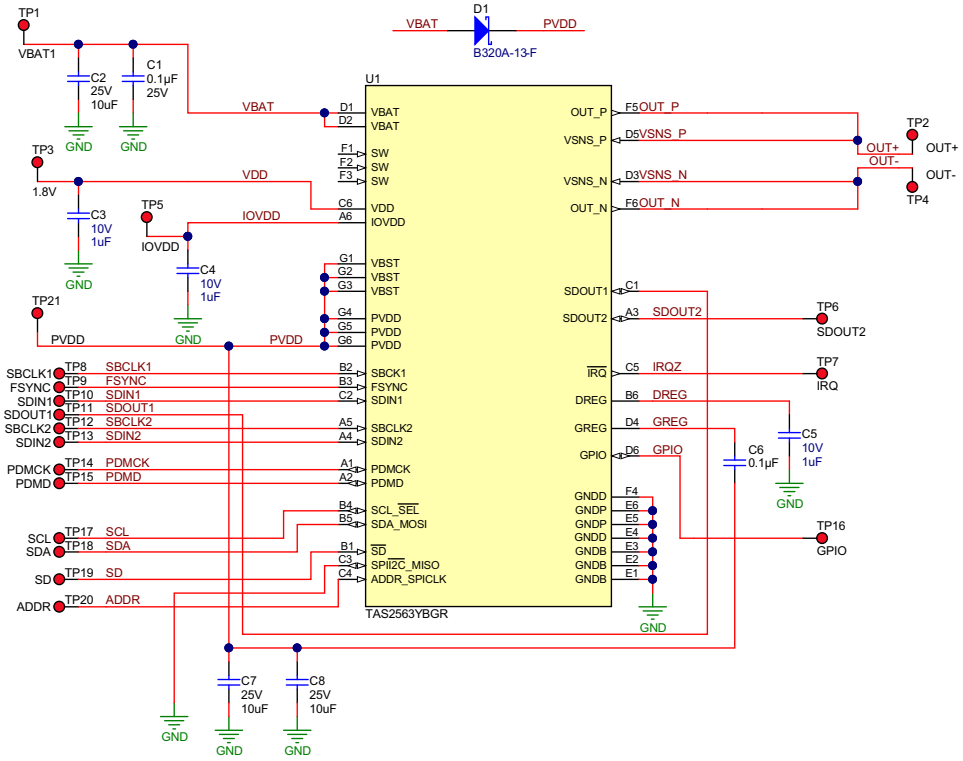

Figure 2-1. External PVDD Schematic

3 Configuration for External PVDD

Configuration for External PVDD Using PPC3 GUI

PPC3 software can be used to configure the device for external PVDD use. Simply go to Device Control panel within TAS2563 app, look for Channel Gain block and a checkbox is available to Enable/Disable the internal boost.

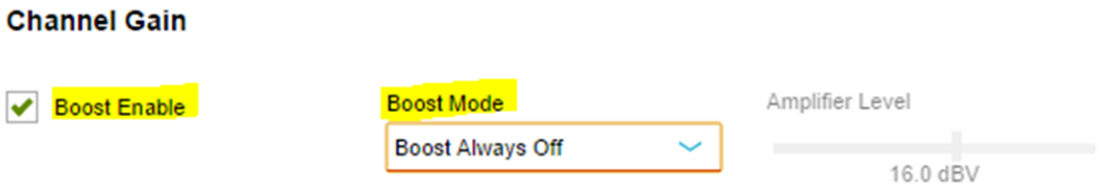

Figure 3-1. PPC3 GUI Boost Controls

Configuration for External PVDD Using I²C Commands

Using external PVDD supply voltage means the internal boost will not be used and thus it needs to be disabled. Boost configuration is set by register 0x33 from page 0, book 0; this register address location is shared across TAS2x63, TAS2562, TAS2110 and must be set to 0xD4. Further details can be consulted in the register map section of your device of interest, but with this value will set the boost to “Boost always OFF” as well as “Boost disabled”, If the boost is not disabled, it will interfere with the external supplied PVDD and can ultimately cause device malfunction.

The brief set of commands below can be used with the EVM and PPC3 I²C command tool to disable the boost from the register configuration:

w 98 00 00

w 98 7f 00

w 98 00 00

w 98 33 c4

4 Power and Configuration Sequence

Figure 4-1 shows the required power sequence for external PVDD. PVDD voltage should not be powered if VBAT is not present as this would cause reverse bias of the internal circuitry.

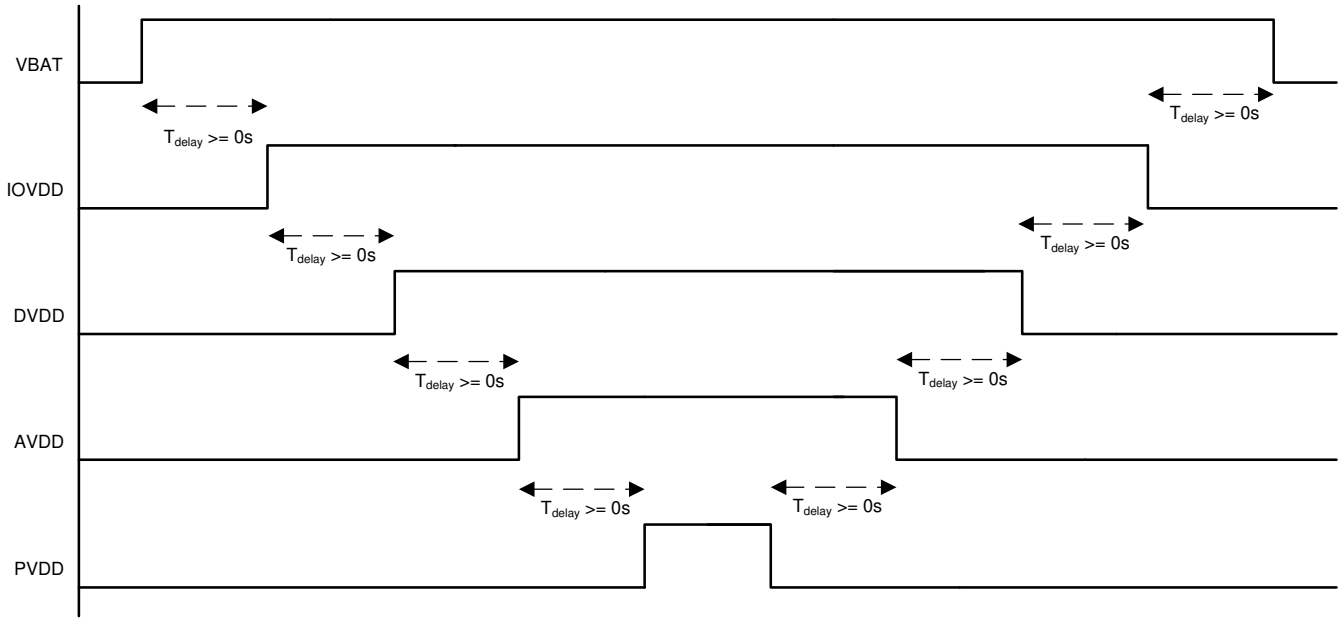

Figure 4-1. Power Sequence for External PVDD

Regarding device configuration, any other configuration file can be used but it is important to use the commands mentioned in Section 3 after the configuration and before taking the device out of software shutdown.

5 Internal vs External PVDD Comparison

This section provides an efficiency comparison of three different solutions:

- Black plot shows the efficiency when using an external PVDD source, this test was taken with external 11 V voltage source.
- Green plot shows the efficiency when using the Class-G multilevel boost.
- Red plot shows the efficiency when the boost is always enabled, regardless of the input signal amplitude.

As it can be observed from the comparison, when there is a higher voltage source available in the system, it is most efficient to use it as the internal boost will not cause any drop in efficiency.

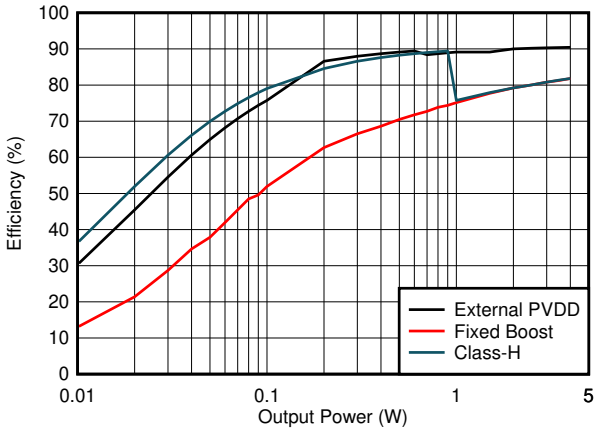

Figure 5-1. Efficiency Comparison

6 Conclusion

This document shows the versatile application of Texas Instruments boosted smart amplifiers, and provides examples and recommendations for system implementation when an external boost is used or there is a higher voltage rail available at the end application.

If further test and analysis is required on this or other device features, we encourage you to try our devices on their evaluation modules. Additionally if you have any questions do not hesitate to visit our e2e forum; there are plenty of answers and FAQs online and you can ask a new question if yours is not already there.

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