Application Report
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System Design Guidelines for SimpleLink™ MSP432E4 Microcontrollers

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ABSTRACT

The SimpleLink™ MSP432E4 microcontrollers are highly-integrated system-on-chip (SOC) devices with extensive interface and processing capabilities. Consequently, there are many factors to consider when creating a schematic and designing a circuit board. By following the recommendations in this design guide, you will increase your confidence that the board will work successfully the first time it is powered it up.

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Trademarks

1 Introduction

The General Design Information section of this guide contains design information that applies to most designs (Section 3). Topics include important factors in the schematic design and layout of power supplies, oscillators, and debug accessibility. The Feature-Specific Design Information section describes specific peripherals and their unique considerations that are relevant to your design (Section 4).

To further assist you with the design process, Texas Instruments provides a wide range of additional design resources, including application reports and reference designs. See the System Design Examples (Section 5) for links to these resources.

2 Using This Guide

The information in this design guide is intended to be general enough to cover a wide range of designs by describing solutions for typical situations. However, because every system is different, it is inevitable that there will be conflicting requirements and potential trade-offs, particularly in designs that include high-performance analog circuits, radio frequencies, high voltages, or high currents. If your design includes these features, then special considerations beyond the scope of this application report may be necessary.

Where possible, the distinction is made between *preferred practice* and *acceptable practice*. This distinction addresses the reality that constraints such as size, cost, and layout restrictions might not always allow for best-practice design.

When considering which practices to apply to a design, one of the most important factors is the pin switching rate and current. If only low-speed, low-current switching on the MSP432E4 peripheral pins, then acceptable-practice rules are likely sufficient. If high-speed switching is present, particularly with simultaneous transitions, then best-practice rules are recommended.

NOTE: Some of the information in this guide comes directly from the individual MSP432E4 microcontroller data sheets. The microcontroller data sheets are the defining documents for device usage and may contain specific requirements that are not covered in this design guide. You should always use the most current version of the data sheet and also check the most recent errata documents for the part number you have selected. Visit www.ti.com/msp432 to sign up for email alerts specific to a MSP432E4 part number. This document defines system design guidelines for MSP432E4 microcontrollers with part numbers starting with MSP432E4.

3 General Design Information

This section contains design information that applies to most MSP432E4 microcontrollers including:

- Package Footprint
- PCB Stack-Up
- General Routing Rules
- Power
- Reset
- Oscillators
- JTAG Interface
- ETM Interface
- System
- All External Signals

3.1 Package Footprint

Packages for MSP432E4 MCUs are BGA or TQFP. Package details and dimensions can be found in the data sheet for the part. PCB footprints for the part should be created using the IPC-7351 standard. For BGA parts, the nominal ball diameter is used as a reference for the landing pad size and solder mask opening for each ball pad. For TQFP parts, the package and lead dimensions maximum and minimum specifications along with standard tolerances are used to calculate the pad size and locations. Many PCB layout tools offer "package wizards" to perform these calculations.

3.1.1 212-Ball BGA Package (ZAD)

The 212-ball BGA package is 10 mm × 10 mm × 1 mm in size. The ball array consists of a 19×19 ball array with a ball pitch of 0.5 mm. Selected balls are not populated to allow 0.8-mm routing rules to be used when routing. See Figure 1. Ball H8 is not populated to provide an obvious orientation of the part for both layout and assembly. The IPC-7351 standard should be followed for NSMD (Non Solder Mask Defined) pads for a 0.3-mm nominal ball diameter, which translates to a 0.25-mm land pad with a 0.30-mm solder mask opening as shown in Figure 2.

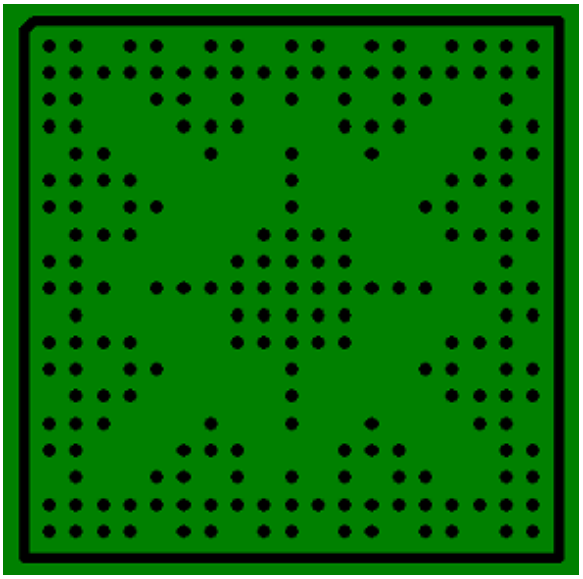


Figure 1. ZAD BGA Footprint Top View

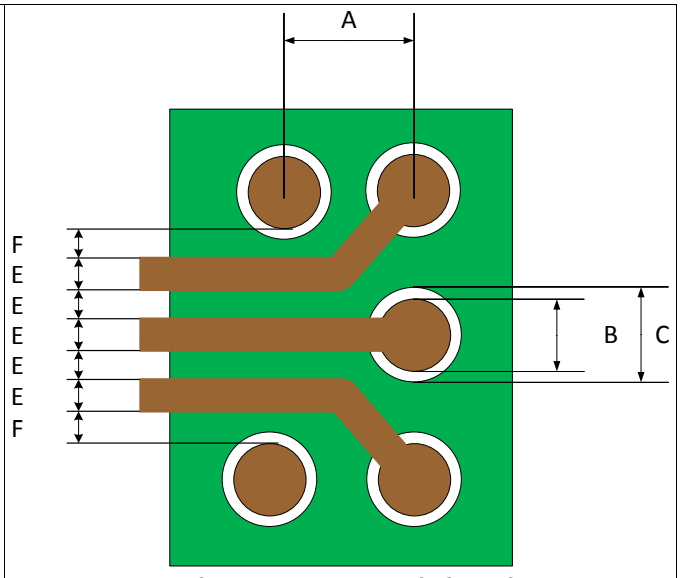


Figure 2. ZAD BGA Pad Dimensions

Table 1. Dimensions for Figure 2

Designator	Description	Size
A	Ball pitch	0.50 mm (19.68 mil)
B	Landing pad size	0.25 mm (9.84 mil)
C	Solder mask opening	0.30 mm (11.81 mil)
D	Not applicable	N/A
E	Trace width and trace spacing	0.1016 mm (4.00 mil)
F	Trace to landing pad spacing	0.1210 mm (4.76 mil)

3.1.2 128-Pin TQFP Package (PDT)

The 128-pin TQFP package is 14 mm × 14 mm × 1 mm in size. The package has 32 pins per side with a pin pitch of 0.4 mm. Figure 3 shows the results of a PCB footprint calculator that follows the IPC-7351 specification based on the package tolerances.

Solder mask oversize is dependent on the tolerances and capabilities of the PCB fabrication shop being used. Three common options for a 0.4-mm pitch TQFP are:

1. Make the solder mask the same size as the pad (0 oversize) and allow the fab shop to make any required adjustments to the Gerber files as required for their process.
2. Make the solder mask 0.05 mm (2.0 mil) larger than the pad [0.05-mm (2.0-mil) oversize] and confirm that the fab shop can handle the 0.1-mm (3.94-mil) solder mask width between pads
3. Create a gang solder mask that voids the solder mask along all pins of each side such that there are no slivers of solder mask between each individual pin. This approach may require special care during assembly to ensure there is no solder bridging between pins.

Paste mask is typically the same size as the pad (0 oversize)

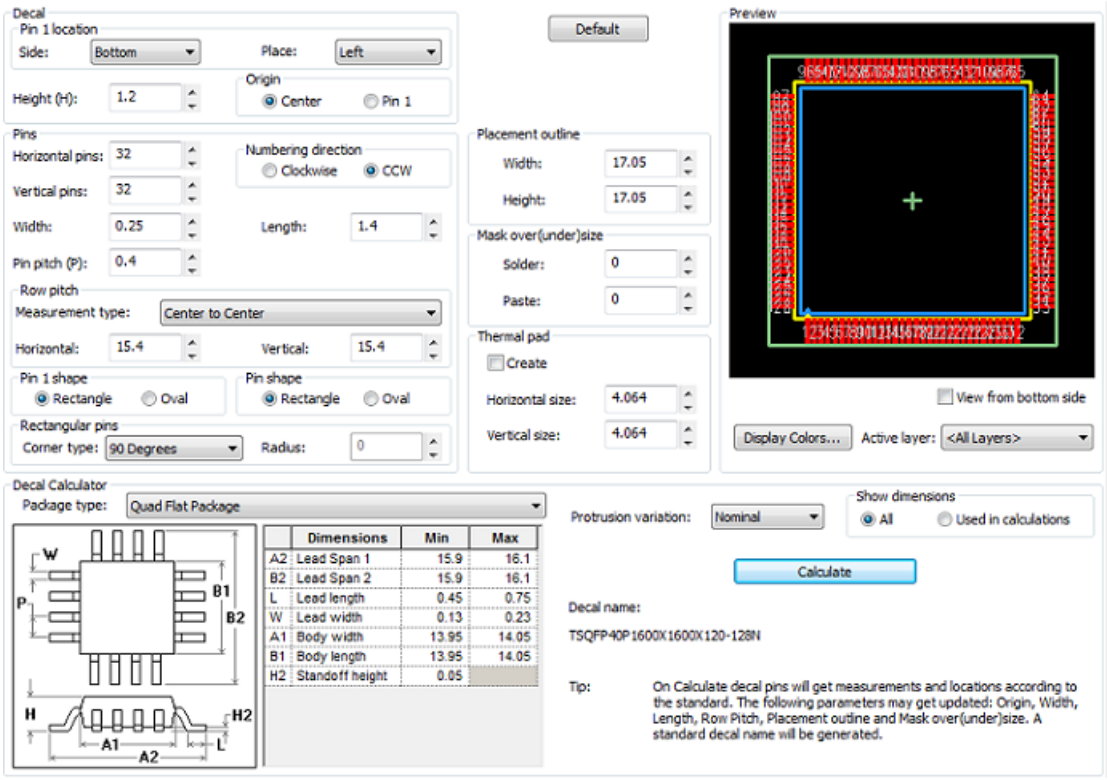


Figure 3. 128-Pin TQFP Footprint

Table 2. 128-Pin TQFP Footprint Dimensions

Designator	Description	Size
A	Pad pitch	0.4 mm (15.75 mil)
B	Pad width	0.25 mm (9.84 mil)
C	Pad length	1.4 mm (55.12 mil)
D	Horizontal row pitch (pad center to pad center)	15.4 mm (606.30 mil)
E	Vertical row pitch (pad center to pad center)	15.4 mm (606.30 mil)
F	Solder mask oversize is dependent on fab capabilities and tolerances	0 mm (0 mil) to 0.05 mm (2.0 mil)
G	Solder paste oversize	0 mm (0 mil)

3.2 PCB Stack-up and Trace Impedance

An important component of any layout is determining what PCB stack-up to use. The PCB stack-up configuration determines several elements of the design:

- Number of layers available for routing
- Number of layers available for power and ground planes
- Single-ended trace impedance, capacitance per inch and propagation delay per inch of a trace of a particular width. These factors are important for longer trace lengths (typically longer than 6 inches) on critically timed interfaces or on interfaces that are near the maximum capacitive load.
- Trace width and spacing required to achieve the differential impedance targets for USB and Ethernet connections

3.2.1 Four-Layer Stack-up

A four-layer stack-up (two signal layers, two power planes) is recommended for most designs. A four-layer stack-up has the following benefits:

- A solid ground plane reference for USB and Ethernet signals that have a specific impedance target.
- Low-impedance power and ground connections to components and decoupling capacitors through the planes.
- High-speed signals have lower impedance, smaller propagation delay and more immunity to crosstalk due to the closer distance to the reference plane on a four-layer design as compared to a two-layer design.
- Analog signals have more immunity to crosstalk, and the analog modules in the device can provide higher precision results when used with the solid ground plane reference that a four-layer stack-up provides.

Figure 4 shows a typical configuration for an FR-4, 0.062-in (1.5748-mm) circuit board with four layers of 1-oz copper.

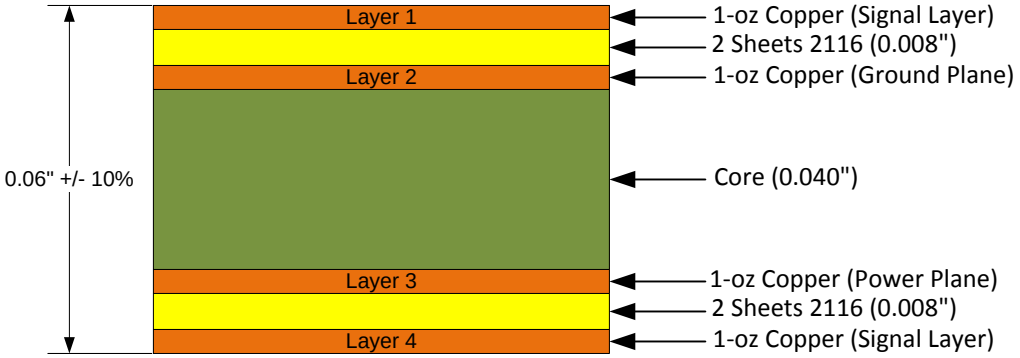


Figure 4. Typical Four-Layer PCB Stack With Routing Assignments

For this example, a solid ground plane is on layer 2 and a power plane is on layer 3. The outer signal layers each consist of 1/2-oz base copper with 1/2-oz plating to total 1-oz copper. Each 1-oz copper layer is 1.4 mil (.0014 in or 0.0355 mm) thick. The height of traces above the ground plane is defined by the thickness of the PCB prepreg material—in this case, 0.008 in (0.2032 mm) thick. Therefore, total thickness is:

$$\text{Total thickness} = 0.062 \text{ in} = 4 \times 0.0014 \text{ in} + 0.040 \text{ in} + 2 \times 0.008 \text{ in} \quad (1)$$

3.2.2 Two-Layer Stack-up

A two-layer stack-up may be acceptable given the following considerations:

- No timing-sensitive high-speed interfaces are being used
- USB and Ethernet are either not being used on the design or the distance to connectors is short
- The design allows for adequate power and ground routing with good decoupling placement and ESD protection

Figure 5 shows a typical configuration for an FR-4, 0.062-in (1.5748-mm) circuit board with two layers of 1-oz copper (no plating).

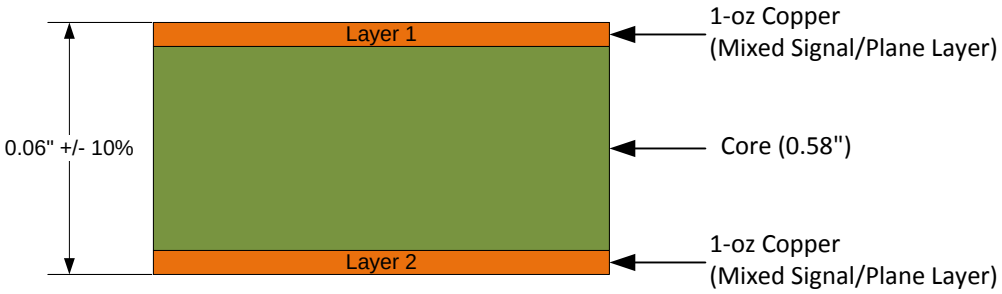


Figure 5. Typical Two-Layer PCB Stack with Routing Assignments

For this example, the top and bottom layers are used for both signal routing and copper power floods. The 1-oz copper mixed plane is 1.4 mil (.0014 in or 0.0355 mm) thick. The height of traces above any ground pour is defined by the thickness of the PCB core material—in this case, 0.058 in (1.4732 mm) thick. Therefore, total thickness is:

Total thickness = 0.061 in = 2 × 0.0014 in + 0.058 in (2)

3.2.2.1 Six-Layer Stack-up

Stack-ups greater than four layers can be used if desired for high-density designs.

Figure 6 shows a typical configuration for an FR-4, 0.062 in (1.5748 mm) circuit board with six layers of 1-oz copper (no plating).

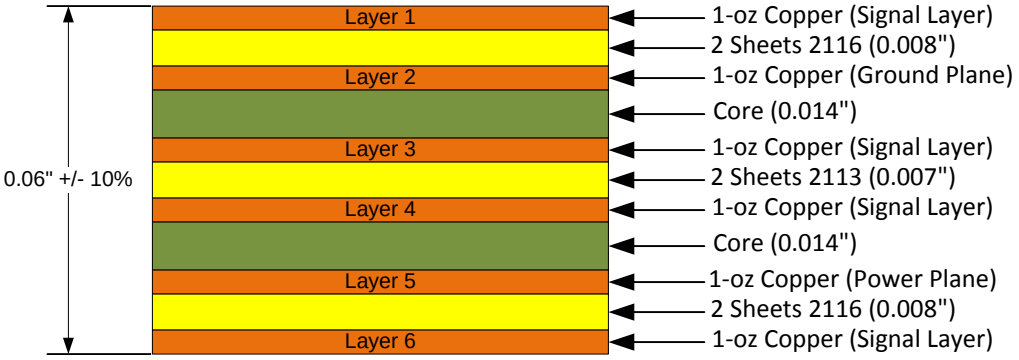


Figure 6. Typical Six-Layer PCB Stack with Routing Assignments

For this example, a solid ground plane is on layer 2 and a power plane is on layer 5. The 1-oz copper planes are 1.4 mil (0.0014 in or 0.0355 mm) thick. The height of traces on the outer layers (1 and 2) above the planes is defined by the thickness of the PCB prepreg material—in this case, 0.008 in (0.2032 mm) thick. The height of the traces on the inner layers (3 and 4) above the planes is defined by the thickness of the PCB core material—in this case, 0.040 in (1.016 mm) thick. In between layers 3 and 4 is additional prepreg material—in this case, 0.007 in (0.1778 mm) thick. Therefore, total thickness is:

Total thickness = 0.0594 in = 6 × 0.0014 in + 2 × 0.008 + 2 × 0.014 in + 0.007 in (3)

There are some additional routing considerations for the internal layers (3 and 4) when using a six-layer stack-up:

- These internal layers (3 and 4) are considered asymmetric stripline relative to the ground and power planes (layers 2 and 5, respectively) (see Figure 7). The calculations for impedance of traces on these layers are different from the calculations for layers 1 and 6.
- Generally, traces on layers 3 and 4 are higher in capacitance per inch and have a higher propagation delay
- Traces on layers 3 and 4 can affect each other through crosstalk if they run parallel and over each other.
- Traces on layers 3 and 4 are better shielded from external EMC radiation or interference because they

are shielded by the power and ground planes.

3.2.3 Trace Properties: Impedance, Inductance, Capacitance, Propagation Delay

Impedance (Z_O), capacitance per inch (C_O), inductance per inch (L_O), and propagation delay (t_{PD}) are all important considerations when routing high-speed signals and low-impedance power nets. Differential trace impedance is important for Ethernet and USB differential signals. All of these properties are dependent on the trace width used (W), distance away from the reference plane (H), thickness of the trace (T) and relative permittivity of the dielectric (E_R), see Table 3. Differential impedance is also significantly affected by the distance between the differential traces (S).

Some PCB design tools have an integrated trace impedance calculator that factors in trace geometry, trace length, board stack-up, and the board material dielectric constant. Several free programs are also available that can perform similar calculations. The Saturn PCB Toolkit from Saturn PCB Design, Inc is an example of one of these free programs that has been used for most of the impedance calculations in this document.

3.2.3.1 Single-Ended Trace Impedance

The first step in calculating these single-ended trace properties is to identify the transmission line type of the trace. The microstrip transmission line type (see Figure 7) is most common on two-layer and four-layer boards as well as layers 1 and 6 of six-layer boards. The asymmetric stripline transmission line type is most common on layers 3 and 4 of six-layer boards.

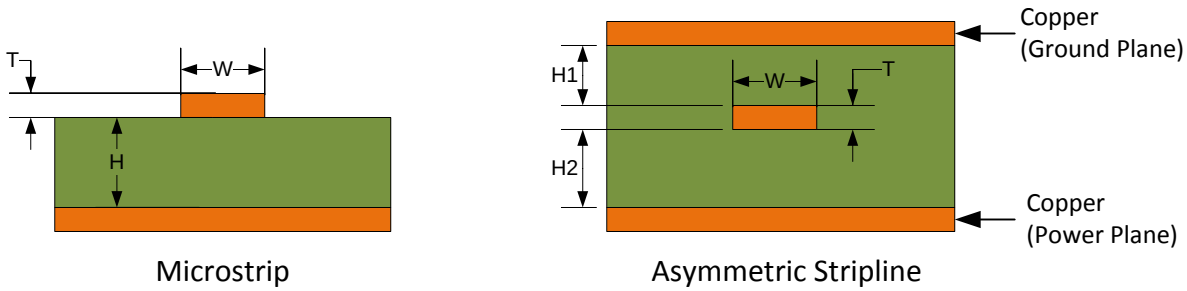


Figure 7. Transmission Line Type

The typical dielectric constant (E_R) for FR-4 material is about 4.3. The following examples use this parameter as well as the stack-ups defined in Section 3.2 to generate some typical PCB geometries. They are intended as starting points for PCB designs. You should repeat the calculations for your own design because even small changes in the PCB stack-up can significantly change the impedance.

Table 3. Single-Ended Trace Properties by Width and Stack-up

Configuration and Layer	W (mil)	T (mil)	H, H1 (mil)	H2	E_R	Z_O (Ω)	C_O (pF/in)	L_O (nH/in)	t_{PD} (ps/in)	Notes
Four layer (1,4) Six layer (1,6)	4	1.4	8	N/A	4.3	85.26	1.64	11.90	139.58	4-mil trace and space rules (0.8-mm routing rules) can be used to route I/O signals from the BGA package. This trace width can also be used to route I/O signals from the QFP packages.
Six layer (3,4)	4	1.4	14	22.4	4.3	82.03	2.14	14.42	175.74	4-mil trace impedance of asymmetric stripline on internal layers 3 and 4 of a six-layer board. Note: H1, H2 results in similar impedance to outer layers but higher capacitance and propagation delay.
Two layer (1)	4	1.4	58	N/A	4.3	N/A	N/A	N/A	N/A	4-mil traces are generally not applicable to two-layer designs and are outside the constraints of the PCB calculator used.
Four layer (1,4) Six layer (1,6)	5	1.4	8	N/A	4.3	79.42	1.76	11.09	139.58	5-mil trace and space rules can be used to route I/O signals from the QFP packages. These rules result in a slightly lower impedance but higher capacitance than 4-mil traces.

Table 3. Single-Ended Trace Properties by Width and Stack-up (continued)

Configuration and Layer	W (mil)	T (mil)	H, H1 (mil)	H2	E_R	Z_O (Ω)	C_O (pF/in)	L_O (nH/in)	t_{PD} (ps/in)	Notes
Six layer (3,4)	5	1.4	14	22.4	4.3	76.82	2.29	13.50	175.74	5-mil trace impedance of asymmetric stripline on internal layers 3 and 4 of a six-layer board. Note: H1, H2 results in similar impedance to outer layers but higher capacitance and propagation delay.
Two layer (1)	5	1.4	58	N/A	4.3	N/A	N/A	N/A	N/A	5-mil traces are generally not applicable to 2 layer designs and are outside the constraints of the PCB calculator used.
Four layer (1,4) Six layer (1,6)	7	1.4	8	N/A	4.3	69.98	1.99	9.77	139.58	7-mil trace and space rules can be used to route I/O signals from the QFP packages. 7-mil trace width is recommended for routing I/O signals from the QFP packages when space is available.
Six layer (3,4)	7	1.4	14	22.4	4.3	68.67	2.56	12.07	175.74	7-mil trace impedance for the internal layers using asymmetric stripline.
Two layer (1)	7	1.4	58	N/A	4.3	142.10	0.98	18.83	139.58	7-mil trace and space rules are recommended for routing I/O signals from the QFP packages on two-layer boards.
Four layer (1,4) Six layer (1,6)	10	1.4	8	N/A	4.3	59.24	2.36	8.27	139.58	10-mil traces are recommended for routing to power and ground pins of the QFP packages and the decoupling capacitors.
Six layer (3,4)	10	1.4	14	22.4	4.3	59.69	2.94	10.49	175.74	10-mil trace impedance for the internal layers using asymmetric stripline.
Two layer (1)	10	1.4	58	N/A	4.3	131.37	1.06	18.34	139.58	10-mil traces are recommended for routing to power and ground pins of the QFP packages and the decoupling capacitors.

3.2.3.2 Differential Trace Impedance

The Ethernet and USB interfaces have critical differential impedance requirements. Both Ethernet signal pairs should be routed as a 100 Ω ±10% differential pair on the top layer of the PCB with a ground plane as a reference. The USB signal pair should be routed as a 90 Ω ±10% differential pair on the top layer of the PCB with a ground plane as a reference. When possible, a single-ended impedance that is half of the differential impedance should be targeted to determine the initial trace width.

The optimal way to achieve a specific differential impedance is a two-step process. During PCB layout, the designer should use PCB tools to set the spacing and width of the traces to get close to the target characteristic impedance.

The second step is performed by the PCB fab house as they adjust the trace space and width to match their specific materials and process.

NOTE: The PCB fab notes should include annotations that specify which traces are to be *impedance controlled*.

Another key benefit of specifying controlled impedance is that the PCB manufacturer assumes on-going responsibility for maintaining the impedance of those traces. This stipulation can be a factor when lot-to-lot differences introduce variation.

While specifying controlled impedance is preferred, it may be acceptable not to if the trace length is less than approximately 2 in (50.8 mm). If good design rules are followed during layout, it should be possible to achieve routing that provides good signal integrity.

A slight variation of this method, which also avoids the additional cost of controlled-impedance PCBs, is sometimes called *controlled dielectric*. This approach involves the PCB designer using a dielectric specification that is either supplied or agreed to by the board fab house. The material and dielectric constant should be added to the PCB fab notes.

Figure 8 shows the differential impedance calculations use the Microstrip differential transmission line type as with a ground reference plane.

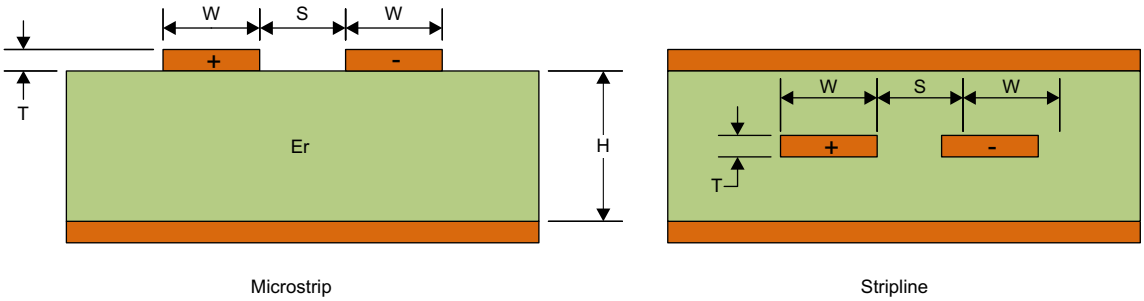


Figure 8. Differential Transmission Line Types

Table 4. Differential Properties by Width and Stack-up

Configuration and Layer	W (mil)	T (mil)	H (mil)	S (mil)	E_R	Z_{DIFF} (Ω)	Z_O (Ω)	Notes
Four layer or Six layer	12	1.4	8	24	4.3	104.1	53.5	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 100 Ω ±10% differential impedance trace with a 50 Ω ±10% single-ended impedance target using the stack-ups defined in Figure 4 and Figure 6.
Two layer (1)	30	1.4	58	7	4.3	107.84	94.19	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 100 Ω ±10% differential impedance trace using the stack-up defined in Figure 5. A single-ended impedance target of 50 Ω ±10% is not realistic with this stack-up.
Four layer or Six layer	15	1.4	8	24	4.3	90.1	46.3	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 90 Ω ±10% differential impedance trace with a 45 Ω ±10% single-ended impedance target using the stack-ups defined in Figure 4 and Figure 6.
Two layer	48	1.4	58	7	4.3	90.2	78.82	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 90 Ω ±10% differential impedance trace using the stack-up defined in Figure 5. A single-ended impedance target of 45 Ω ±10% is not realistic with this stack-up.

NOTE: The PCB fab house knows their process and materials the best. They should be contacted to confirm stack-up heights, dielectric constant (E_R), and recommended trace widths and spacing for the targeted differential impedances.

The only way to ensure that the impedance target is met by the PCB manufacturer is to specify traces as *impedance controlled*.

3.3 General Layout Design Choices

There are a number of layout design choices that can affect PCB fabrication cost, assembly costs, and operational reliability. This section describes some of these choices and the thoughts behind them.

3.3.1 Trace Width and Spacing

Trace width and spacing impact the design in many ways. The minimum trace width and space on the PCB are two factors defining the cost of the PCB, and they are highly dependent on the capabilities of the PCB fab house. As a general guideline for low volume production, there is a cost increase for a minimum width/spacing less than 7 mil (0.1778 mm). A large number of PCB fab houses can produce boards with a minimum width and spacing of 4 mil (0.1016 mm) and a maximum 1-oz. finished copper weight on the outer layers. Another common minimum width and spacing capability point is 5 mil (0.1270 mm). These factors are some of the reasons behind the trace width choices in Table 3 and why 7-mil trace width and space is recommended for routing I/O signals from the QFP packages.

The BGA package is more dense and requires the 4 mil (0.1016 mm) trace and space rules to be able to route the I/Os from that package (see Section 3.3.3).

The routing of power and ground nets should be done with the wider and lower-impedance traces wherever possible. Accordingly, trace width routes should be 10 mil (0.2540 mm) or wider from decoupling caps and for main power nets and 7 mil (0.1778 mm) or 10 mil (0.2450 mm) from the QFP power pins. For the BGA, it may be necessary to route using a 4-mil trace for a short distance until a wider 7-mil or 10-mil trace can be used.

When routing a signal that is going to be used as a fast-edge-rate clock, provide two times the spacing requirement from adjacent signals where possible to reduce crosstalk to and from the clock net. For example, if routing with a 7-mil wide trace and space rule, make sure there is 14-mil spacing between the clock and adjacent signals.

3.3.2 Via Sizes

PCB fab houses can vary in their capabilities for through-hole vias. Via size is often limited by the smallest mechanical drill diameter a PCB fab house uses. The minimum via pad size is usually required to be the drill size plus an additional adder. Drill size + 10 mil is quite common for a via pad size. Drill size + 8 mil and drill size + 12 mil are also common.

The amount of the adder is related to the IPC-6012 class of inspection requested by the customer and annular ring requirement of the customer. Boards fabricated and inspected with the IPC-6012 Class 2 requirement allow for one void per hole in not more than 5% of the holes. Boards fabricated and inspected with the IPC-6012 Class 3 requirements allow for no voids per hole. A PCB fab house usually requires a larger adder for Class 3 boards. A PCB fab house maintains a minimum annular ring, typically 1 mil, around each via hole, but the customer could choose to allow tangency where the hole is up to the edge of the pad but "breakout" has not occurred. This method can allow for a smaller diameter via pad if needed.

Table 5 lists some common via sizes along with some of characteristics calculated using the Saturn PCB Toolkit.

Table 5. Via Sizes and Properties

Via Type	Via Pad Size (mil)	Drill Size (mil)	Via Height (mil)	Reference Plane Opening Diameter (mil)	E_R	Via Capacitance (pF)	Via Inductance (nH)	Via Resistance (mΩ)	Via Impedance (Ω)	Notes
16D6	16	6	62	24	4.3	0.75	1.49	2.08	44.48	Small, lower capacitance but higher resistance via. Some PCB fab houses may not be able to accommodate this size. Useful for tight spaces and dense routes.
18D8	18	8	62	26	4.3	0.85	1.40	1.62	40.63	The largest via pad size (18 mil) that can be used to break out route of the BGA package with 4-mil spacing. Pad size is 10 mil over drill size of 8.
18D9	18	9	62	26	4.3	0.85	1.36	1.46	40.01	The largest via pad size (18 mil) that can be used to break out route of the BGA package with 4-mil spacing. Pad size is 9 mil over drill size of 9.
20D10	20	10	62	28	4.3	0.94	1.33	1.32	37.57	A standard via pad size (20 mil) that is 10 mil over the drill size of 10. Good for vias for power traces and general I/O traces. Achievable by a large number of PCB fab houses.
22D10	22	10	62	30	4.3	1.03	1.33	1.32	35.81	A standard via pad size (22 mil) that is 12 mil over the drill size of 10. Good for vias for power traces and general I/O traces. Achievable by an even wider number of PCB fab houses.

3.3.3 212-Ball BGA Escape Routing

The populated balls on the 212-ball BGA package (see Section 3.1.1) and the choice of their functions are arranged to allow all I/O signals to be routed from the BGA on a four-layer board (see Section 3.2.1) using 4-mil traces with 4-mil spacing and 18-mil diameter vias. This section describes how to route all I/O signals away from the BGA, also known as *escaping the BGA* with the following considerations in mind:

- Standard process 4-mil trace, 4-mil space, and 18-mil diameter vias, also known as 0.8-mm routing rules, are the smallest needed to escape the BGA.
- The BGA can be routed using a minimum of a four-layer board with two routing layers on top and bottom, a ground plane, and a power plane.
- Required power routing and capacitor decoupling placement for all power rails can be achieved using 0402-sized capacitors.
- Routing of impedance-controlled traces is a priority.

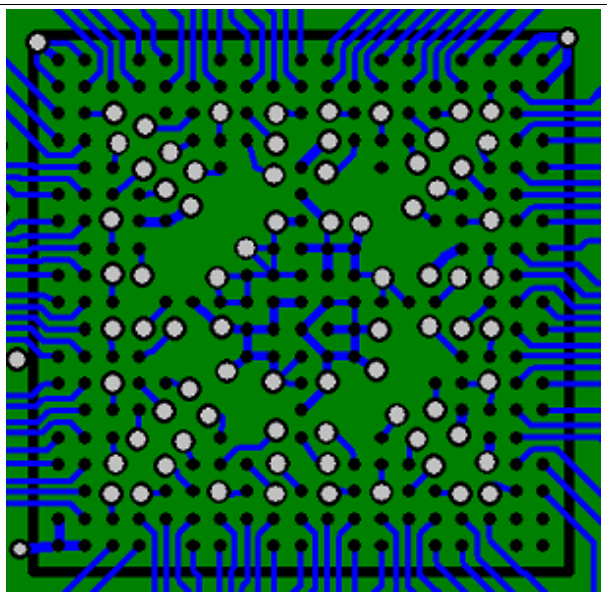


Figure 9. Top Layer 212-Ball BGA Escape Routing

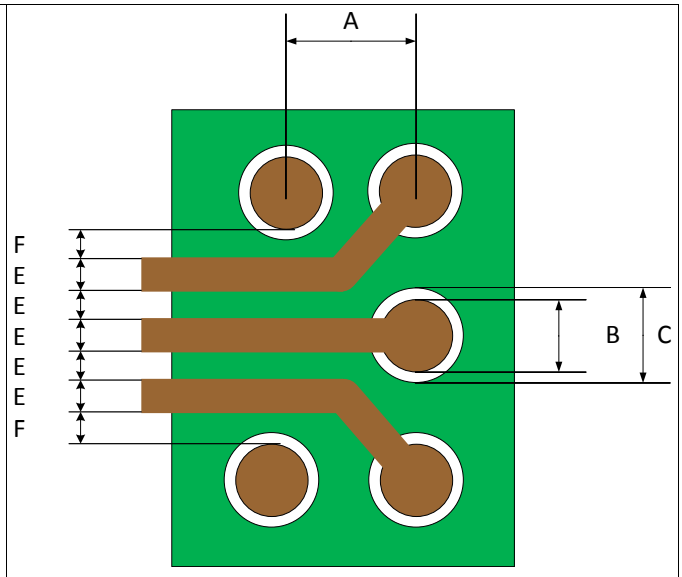


Figure 10. BGA Escape Routing Through Depopulated Ball Location

Figure 9 shows the recommended top layer routing pattern used to escape the BGA. The black dots are the 0.25 mm (9.84 mil) BGA landing pads (also shown as B in Figure 10). The black circles with white centers are 0.457-mm (18-mil) vias.

Some things to note about Figure 9:

- For the outer two rows of balls, all but four signals route on the top layer to escape the BGA.
- Routing from the second row of balls between balls with a 0.5 mm (19.69 mil) spacing and 0.1 mm (4.0 mil) trace and space is not possible. Traces from the second row of balls must be routed through the opening left by the depopulated ball in the first row as shown in Figure 10 where E is 0.1 mm (4 mil) and F is 0.12 mm (4.76 mil).
- All other balls require vias to the backside or power planes. The placement of the vias is important to enable all traces on the back side to escape. See Figure 11. It may be necessary to use a very small grid spacing to align the vias with 4-mil spacing.
- Each set of three balls that connect to GND on the three of the corners of the BGA can share a via to GND.
- The balls near the center of the BGA are either power (V_{DD}) or ground (GND). These balls are connected together in a web-like structure with 6 mil wide traces to provide a low impedance connection to power or ground. This web structure is preferred over a copper pour, which may cause assembly issues due to uneven ball melting.
- The location of the vias in the center of the BGA allow for placement of two 0402 decoupling capacitors on the back side of the board directly under the BGA, as shown in Figure 11.

- Impedance controlled differential signals are routed with 0.1 mm (4 mil) trace/spacing until they escape the perimeter of the BGA and can be routed with the desired trace width and spacing to meet the impedance target.
- All V_{DD}, V_{DDA}, GND, GNDA, V_{REFA+}, and V_{REFA-} signals are routed as 0.1524-mm (6-mil) traces within the BGA escape area.
- All V_{DDC} signals are routed as 0.2032-mm (8-mil) traces within the BGA escape area.
- All other signals are routes as 0.1-mm (4-mil) traces within the BGA escape area.

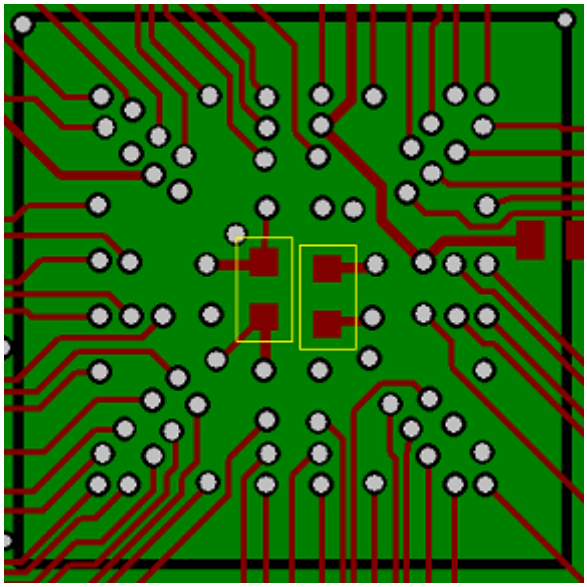


Figure 11. Bottom Layer 212-Ball BGA Escape Routing

Figure 11 shows the bottom layer escape routing under the BGA from the vias. In the center of the bottom layer are two 0402-sized 0.1-µF decoupling capacitors connected between VDD and GND.

3.3.4 PCB Design Rules: 90° PCB Traces

For many years, it has been common PCB design practice to avoid 90° corners in PCB traces. In fact, most PCB layout tools have a built-in miter capability to automatically replace 90° angles with two 45° angles.

The reality is that the signal-integrity benefits of avoiding 90° angles are insignificant at the frequencies and edge-rates seen in microcontroller circuits (even up to and past 1 GHz/100 ps) (see High-Speed Digital Design: a Handbook of Black Magic).

Additionally, one report could find no measurable difference in radiated electromagnetic interference (EMI) (see Right Angle Corners on Printed Circuit Board Traces, Time and Frequency Domain Analysis).

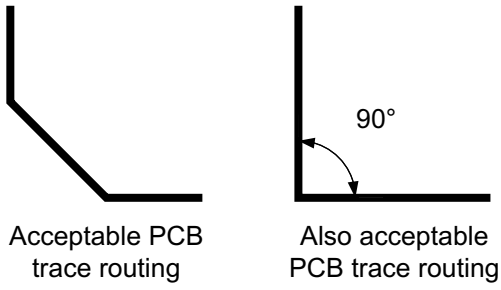


Figure 12. Acceptable PCB Trace Routing

NOTE: Loops in PCB traces are not acceptable, despite the references that indicate that the signal-integrity benefits of avoiding 90° angles is negligible. Loops in traces form antennas and add inductance. The data shows that if your layout does have antenna loops, then mitering the angles to 135° is not going to help. Avoid loops in PCB traces.

Despite these conclusions, there are a few simple reasons to continue to avoid 90° angles:

- There is a higher possibility of an acid-trap forming during etching on the inside of the angle (especially in acute angles). An acid trap causes over-etching which can be a yield issue in PCBs with small trace widths.
- Routing at 45° typically reduces overall trace length. This practice frees board area, reduces current loops, and improves both EMC emissions and immunity.
- It looks better. This consideration is an important factor for anyone who appreciates the art of PCB layout.

3.3.5 Copper Pours

While solid ground and power planes are highly desirable, small areas of copper pour should be used cautiously. It is often not a good idea to pour every available area on the routing layers of multi-layer boards. On one- and two-layer board designs, multiple pours might be necessary, because dedicated plane layers are not available.

If using small copper pours, never leave them floating or unconnected. Isolated conductor areas can cause unwanted coupling and EMC problems if they act as antennas. Small copper pours should have solid connections to a ground net or trace. Ideally, use several vias to provide a low-impedance connection. Ensure even coverage of the copper pours with vias along each side of the pour to avoid a peninsula.

3.3.6 Chassis Ground

When properly designed, a chassis ground routed on the PCB can be a very effective feature for addressing a range of EMC challenges.

One specific benefit is improved electro-static discharge (ESD) immunity due to the provision of a safe discharge path that avoids sensitive circuitry in the center of the board.

In general, a chassis ground on the PCB works in conjunction with the overall enclosure to improve electro-magnetic emissions and especially immunity.

The chassis ground should be routed or poured copper around the perimeter of the PCB, ideally on all layers. If the ground is not present on all PCB layers, then other layers should be pulled back from the chassis ground to avoid coupling. The chassis ground should not route over the top of any power or ground layer.

Typically, the chassis ground should have a break or void in it to prevent loops that could cause loop antenna effects. However, depending on the size of the board, enclosure design, and ground connection point locations, it might still be acceptable or preferable to have a continuous chassis ground around the board.

A chassis ground is particularly important in systems with external connectors, metal enclosures, or apertures in the enclosure (see Figure 13).

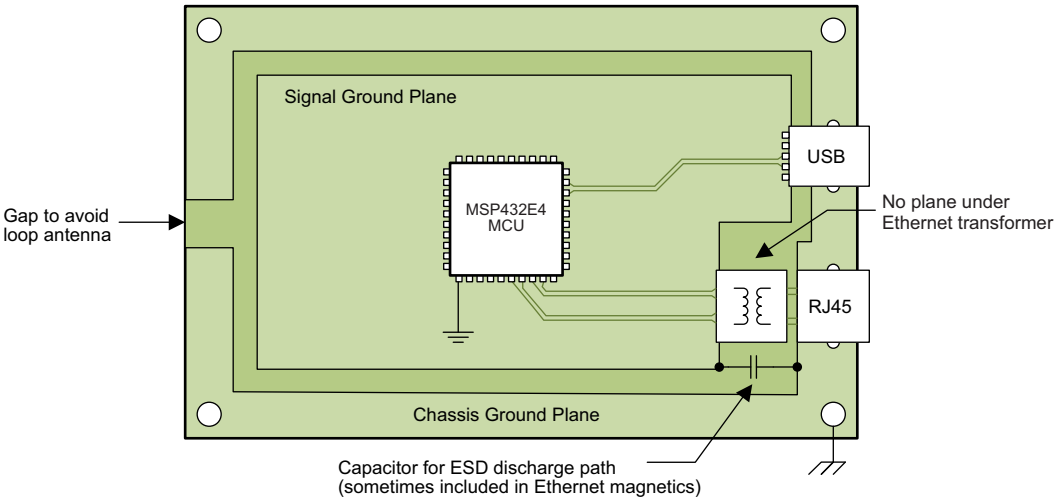


Figure 13. Chassis Ground Guidelines

3.3.7 Routing Across Plane Splits

Avoid discontinuities in ground planes and power planes under high-speed signals (see Figure 14). For all signals, a break in the ground plane removes a direct path for any return current to flow through. This consideration is important even for balanced differential pairs because perfect matching is seldom achievable, and ground current is inevitable.

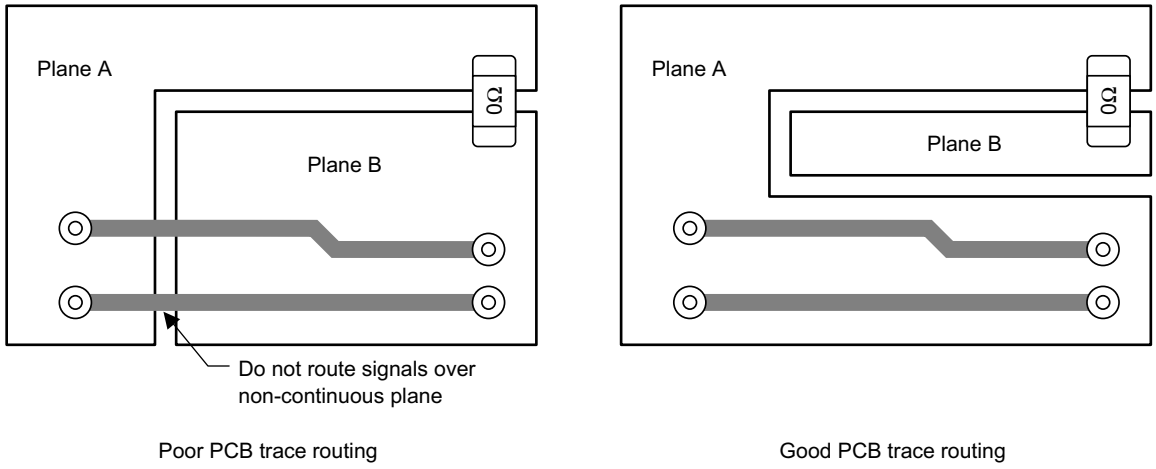


Figure 14. Examples of PCB Trace Layout

MSP432E4 microcontrollers provide programmable drive strength for all digital output pins. When initially bringing up the design, the drive strength for the output pins of a high-speed interface should be set to 8 mA to avoid any marginal timing requirements associated with a drive strength that is too low. However, if a signal is showing signal integrity issues such as ringing and reflections, the GPIO drive strength can be lowered to improve the performance as long as timing requirements are still met.

It is strongly recommended to avoid the practice of routing signals across a split plane as it can be a source of EMI radiation due to the return current flow path. Slow-edge-rate signals such as the open-collector I^2C or UART signals and mostly static GPIOs may be routed across a plane split.

3.3.8 Routing Differential Traces

- For each differential pair, the traces within the pair should be run parallel to each other and be matched in length. Matched lengths minimize delay differences and avoid an increase in common-mode noise and increased EMI (see Figure 15).
- It may be impossible to maintain parallelism immediately near the connector, ESD component, or microcontroller. For these cases, minimize the distance the traces are not parallel and keep them localized near the start or endpoints of the traces.
- Ideally there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace pair on a single layer if possible
- Choose ESD components in packages that support good differential routing of the signals they are protecting without the need for stubs or vias. Many packages have no-connect pins that allow routing of the differential signal through the protection circuit and a no-connect pin to maintain signal spacing.

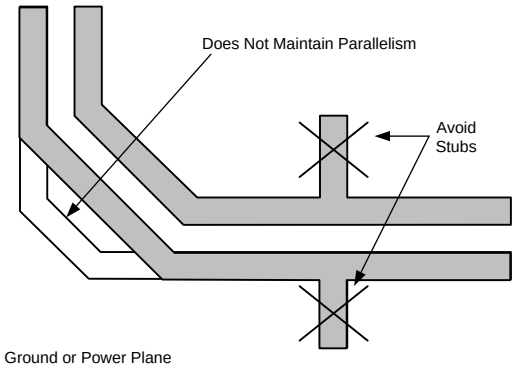


Figure 15. Differential Signal Pair

- Avoid stubs in differential signal pairs where possible (see Figure 15 and Figure 16). Where termination or bias resistors are needed, one terminal should be located directly on the trace. Both resistors should be located at the same distance from the source and load.

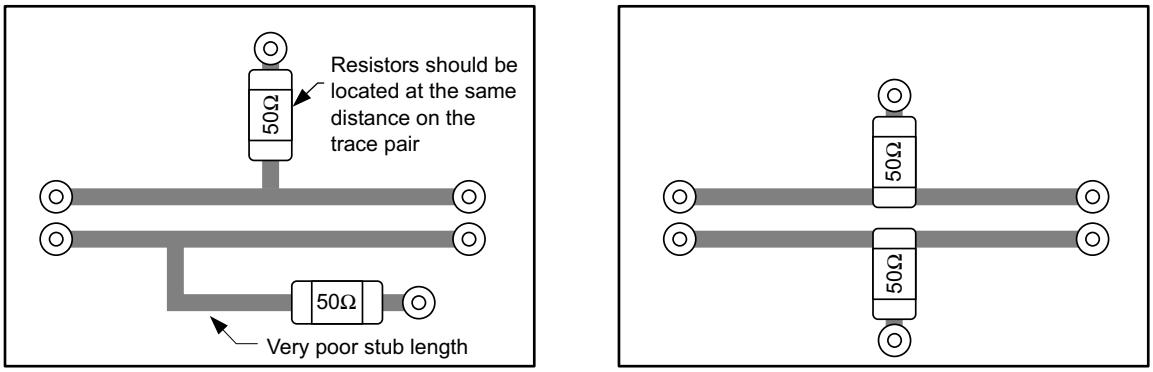


Figure 16. Examples of Differential Pair Layout

- PCB trace lengths should be kept as short as possible.
- Differential signal traces should not be run such that they cross a plane split (see Figure 17). A signal crossing a plane split may cause unpredictable return current paths and result in an impedance mismatch, which can affect signal quality and potentially create EMI problems.

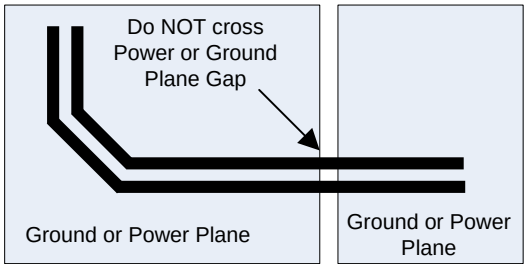


Figure 17. Differential Signal Pair Plane Crossing

3.4 Power

This section describes design considerations related to the microcontroller power supply.

3.4.1 Microcontroller Power Supply

MSP432E4 microcontrollers require only a single 3.3-V power supply connected to V_{DD} and V_{DDA}. Other supply rails are generated internally by on-chip low-drop-out (LDO) regulators. The most visible internal supply rail is the core voltage (V_{DDC}) because it has dedicated power pins for filter and decoupling capacitors.

During normal microcontroller operation, the power-supply rail must remain within the electrical limits listed in the data sheet [V_{DD} (min) and V_{DD} (max)]. For optimal performance of the on-chip analog modules, the supply rail should be well regulated and have minimal ripple. Electrical noise sources such as motor drivers, relays, and other power-switching circuits should each have a separate supply rail, especially if analog-to-digital converter (ADC) performance is a factor.

The microcontroller has analog power-on reset (POR) and power-OK (POK) circuits that release and assert when the V_{DDA} power-supply rails reach specific thresholds. The microcontroller also has digital power-OK (POK) and brownout reset (BOR) circuits that release and assert when the V_{DD} power-supply rails reach specific thresholds. Details on the operation and threshold levels of these circuits can be found in the device-specific data sheet.

The supply connected to V_{DD} must accommodate a short period (40 µs to 60 µs) of additional inrush current that occurs as the decoupling capacitors connected to the LDO on the V_{DDC} rail charge up to the V_{DDC} voltage level. Internal circuitry limits the inrush to the I_{INRUSH}(max) specified in the data sheet. The supply connected to V_{DD} can self limit the current it supplies to something less than the maximum I_{INRUSH}; however, self limiting extends the time it takes to bring V_{DDC} up to operating voltage.

External supervisors may also be used to assert the external reset signal $\overline{RST}$ under power-on, brownout, or watchdog expiration conditions.

3.4.2 LDO Filter Capacitor (V_{DDC})

All MSP432E4 microcontrollers have an on-chip voltage regulator to provide power to the core. The voltage regulator requires a filter capacitor to operate properly (see the C_{LDO} parameter in the corresponding microcontroller data sheet for acceptable capacitor value range).

The C_{LDO} capacitance is the sum of the capacitor values on the V_{DDC} pins. The recommended V_{DDC} capacitor solution, taking tolerance into account, consists of two or more 10%-tolerance ceramic chip capacitors totaling 3.3 µF to 3.4 µF (examples are one each of 3.3 µF and 0.1 µF capacitors or one each 2.2 µF, 1.0 µF, and 0.1 µF). Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

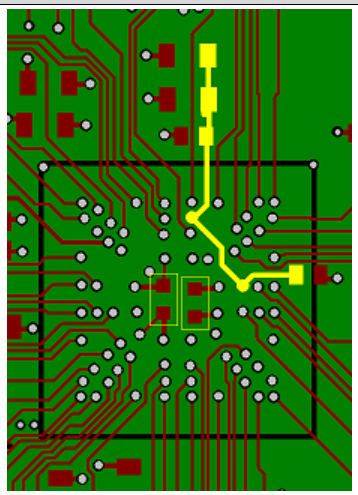
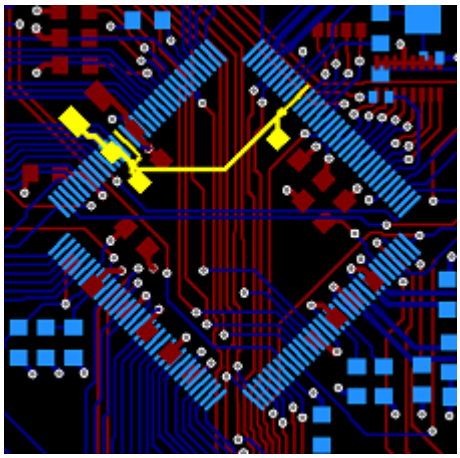
The following recommendations should be followed when placing and routing the capacitors connected to V_{DDC}.

- The larger values of capacitance should be placed closest to the pin specified in the *LDO Regulator Characteristics* section of the data sheet, and the 0.1-µF capacitor can be placed near the other V_{DDC} pins.

- The ESR MAX specification in the data sheet for C_{LDO} must be adhered to and should include any via and trace resistance from the pin or ball to the capacitors.
- All V_{DDC} pins should be routed together using wide traces for lower resistance.

See Table 6 for examples of recommended V_{DDC} routing and C_{LDO} capacitor placement.

Table 6. V_{DDC} Routing and Capacitor Placement for MSP432E4 Devices

212-Ball BGA Package	128-Pin TQFP Package
	
• Highlighted trace is VDDC routed with 0.2032-mm (8-mil) trace. • 2.2-µF, 1.0-µF, and 0.1-µF capacitors placed closest to ball E10 • 0.1-µF capacitor placed near ball H16	• Highlighted trace is VDDC routed with 0.254-mm (10-mil) trace • 2.2-µF, 1.0-µF, and 0.1-µF capacitors placed closest to pin 115 • 0.1-µF capacitor placed near pin 87

NOTE: V_{DDC} is an internally generated voltage rail. Connect V_{DDC} to only the C_{LDO} filter capacitors. Do not connect V_{DDC} to any external source or load.

3.4.3 Decoupling Capacitors

Ideally, MSP432E4 microcontrollers should have one decoupling capacitor in close proximity to each power-supply pin. Decoupling capacitors are typically 0.1 µF in value and should be accompanied by a bulk capacitor near the microcontroller. The combined V_{DD} and V_{DDA} bulk capacitance of the microcontroller is typically between 2 µF and 22 µF, with values on the upper end of that range providing measurable ripple reduction in some applications, especially if the circuit board does not have solid power and ground planes. Bulk capacitance is particularly important if the microcontroller is connected to high-speed interfaces or must source significant GPIO current (that is, greater than 4mA) on more than a few pins.

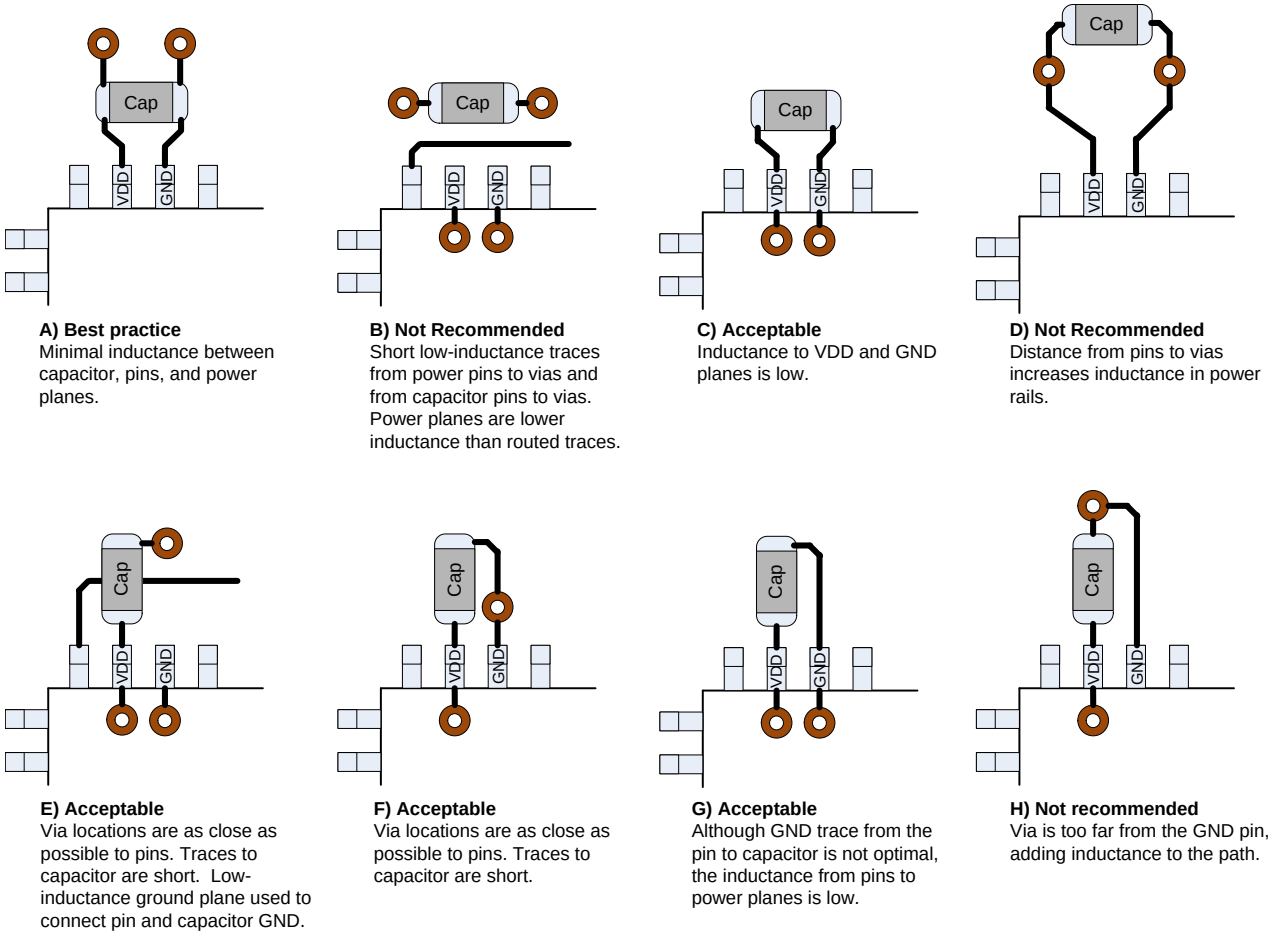
For optimal performance, place one decoupling capacitor adjacent to each V_{DD} power and ground pin pair. At a minimum, there should be one decoupling capacitor on each side of the microcontroller package connected between V_{DD} and ground.

V_{DDA} and GNDA and packages that support V_{REFA+} and V_{REFA-} have specific decoupling requirements as defined by C_{REF} in the data sheet (see Section 3.4.5 for additional details).

Decoupling capacitors should be 6.3 V to 25 V, X5R/X7R ceramic chip types. Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

The capacitance of most ceramic capacitors decreases with increasing voltage. Avoid using capacitors at close to their rated voltage unless reduced capacitance is acceptable. X7R capacitors may lose 15% to 20% of their capacitance at rated voltage while Y5V capacitors may drop 75% to 80% (Comparison of Multilayer Ceramic and Tantalum Capacitors, AVX Technical Bulletin).

Figure 18 shows different options for routing PCB traces between the MSP432E4 microcontroller power pins and a decoupling capacitor.



A) Best practice
Minimal inductance between capacitor, pins, and power planes.

B) Not Recommended
Short low-inductance traces from power pins to vias and from capacitor pins to vias. Power planes are lower inductance than routed traces.

C) Acceptable
Inductance to VDD and GND planes is low.

D) Not Recommended
Distance from pins to vias increases inductance in power rails.

E) Acceptable
Via locations are as close as possible to pins. Traces to capacitor are short. Low-inductance ground plane used to connect pin and capacitor GND.

F) Acceptable
Via locations are as close as possible to pins. Traces to capacitor are short.

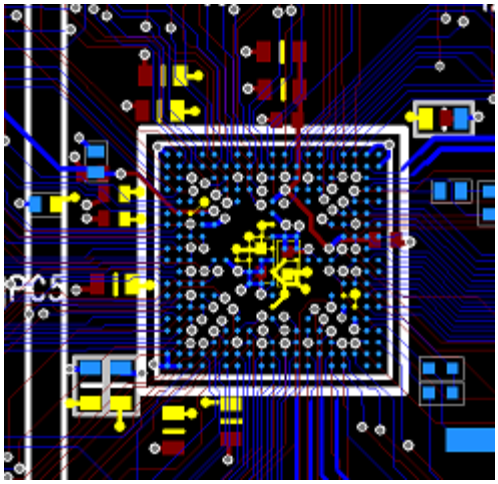
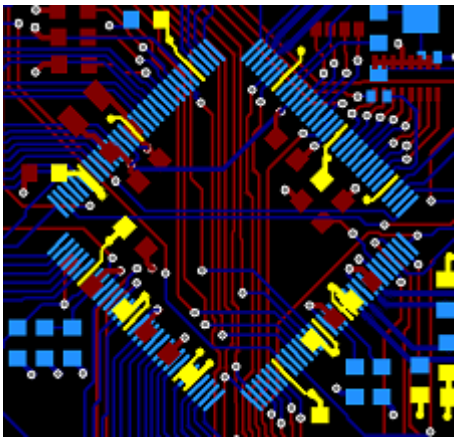
G) Acceptable
Although GND trace from the pin to capacitor is not optimal, the inductance from pins to power planes is low.

H) Not recommended
Via is too far from the GND pin, adding inductance to the path.

Figure 18. QFP PCB Routing Options

Table 7 shows recommended example placement and routing of the V_{DD} and V_{DDA} decoupling capacitors.

Table 7. V_{DD} Routing and Capacitor Placement Examples for MSP432E4 Devices

212 BGA Package	128 TQFP Package
	
• The highlighted traces show the VDD net and decoupling capacitor locations. • Blue traces and pads are on the top. Red traces and pads are on the bottom. • Two decoupling caps are located on the back directly under the BGA.	• The highlighted traces show the VDD net and decoupling capacitor locations. • Blue traces and pads are on the top. Red traces and pads are on the bottom. • Most of the decoupling caps shown in this example are on the back. • There is at least one decoupling capacitor on each side of the chip.

3.4.4 Splitting Power Rails and Grounds

The MSP432E4 microcontrollers are designed to operate with V_{DD} and V_{DDA} pins connected directly to the same 3.3-V power source. Some applications may justify separation of V_{DDA} from V_{DD} to allow insertion of a filter to improve analog performance. Before deciding to split these power rails, the power architecture of the device should be reviewed to determine which on-chip modules are powered by each supply. The device-specific data sheet contains a drawing that shows power architecture.

Filter options include filter capacitors in conjunction with either a low-value resistor or inductor (or ferrite bead) to form a low-pass filter.

If the V_{DD} and V_{DDA} pins are split, ensure that V_{DDA} power is applied before or simultaneously with V_{DD} and that V_{DDA} is removed after or simultaneously with V_{DD}.

If V_{DDA} is the reference source for the ADC, the ADC achieves better performance when powered with a separate V_{DDA} power rail and filtered with 0.01-µF and 1-µF capacitors (C_{REF}) between V_{DDA} and GNDA.

The GND and GNDA pins should always be connected together—preferably to a solid ground plane or copper pour.

3.4.5 V_{REFA+} and V_{REFA-}

V_{REFA+} and V_{REFA-} can be used as the reference voltage for the ADC maximum and minimum conversion values.

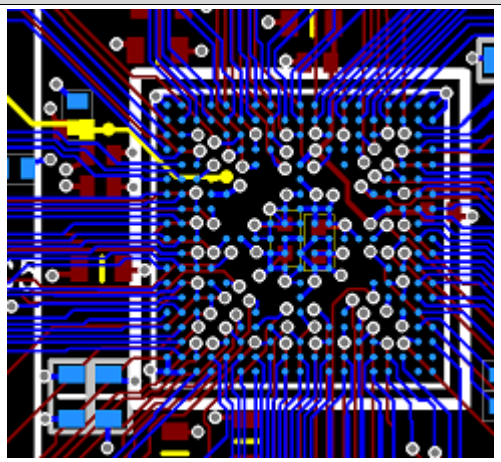
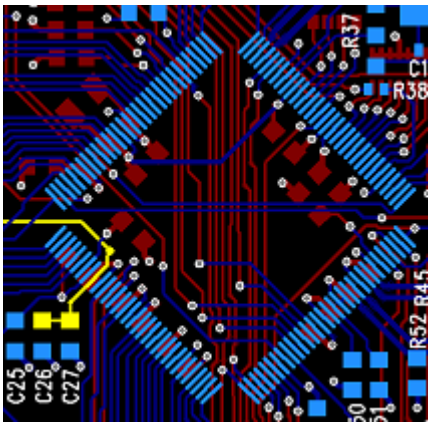
Some MSP432E4 MCUs have V_{REFA+} and V_{REFA-} brought out to dedicated pins, some parts have a dedicated pin for V_{REFA+} and V_{REFA-} is internally connected to GNDA, and some parts do not have dedicated pins for V_{REFA+} or V_{REFA-}, and instead V_{REFA+} is internally connected to V_{DDA}, and V_{REFA-} is internally connected to GNDA.

Designs that require high-precision ADC conversions and use MCUs that have dedicated V_{REFA+} or V_{REFA-} pins should ensure that the references pins are connected to a high precision voltage reference. If the ADC conversions are not required to be high precision, then V_{REFA+} can be externally connected to V_{DDA} and V_{REFA-} can be externally connected to GNDA.

NOTE: Do not leave V_{REFA+} or V_{REFA-} unconnected. V_{REFA+} must power up after or simultaneous to V_{DDA}.

For optimized ADC precision, V_{REFA+} should be supplied from a high-precision reference such as the TI REF3230. V_{REFA-} should be connected to GNDA and a 0.01-µF and 1-µF filter capacitor pair (C_{REF}) should be placed as close as possible to the VREFA+ and VREFA- pins. The Enable and V_IN of the REF3230 should be driven from V_{DD} or V_{DDA} to ensure the correct power-up sequence.

Table 8. Example VREFA+ and VREFA- Routing and Capacitor Placement Examples

212 BGA Package	128 TQFP Package
	
• The highlighted trace is the VREFA+ net. • The 1-µF capacitor is located on the top. The 0.01-µF capacitor is located on the bottom. • In this example, VREFA- is a dedicated pin connected directly to GND.	• The highlighted trace is the VREFA+ net • C26 and C27 are the 1-µF and 0.01-µF capacitors placed close to the device. • This device has V_{REFA-} internally connected the GNDA pin, which is connected to digital GND on this design.

3.4.6 V_{BAT}

The MSP432E4 MCUs supports a V_{BAT} supply for battery-backed RAM retention and RTC operations when the main VDD supply is not powered. V_{BAT} has a maximum ramp time, as specified in the data sheet as V_{BATRMP}. If V_{BAT} is to be driven from a coin cell battery or switched, an RC filter must adhere to the V_{BATRMP} rise time requirement (see Figure 19).

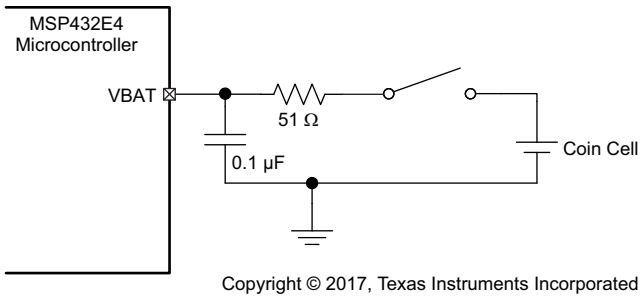


Figure 19. VBAT RC Filter

If a dedicated battery is not going to be used, V_{BAT} can be connected to the same net driving the V_{DD} pins without adding the RC filter.

No dedicated decoupling is needed for the V_{BAT} pin.

NOTE: If a single-ended clock source is used to drive XOSC0 to the RTC or Hibernation module, the voltage level of V_{BAT} affects the acceptable XOSC0 input levels. See the Hibernation oscillator input characteristics in the data sheet.

3.5 Reset

This section describes design considerations related to reset.

3.5.1 External Reset Pin Circuits

A special external reset circuit is not normally required. MSP432E4 microcontrollers have an on-chip Power-On-Reset (POR) circuit with a delay to handle power-up conditions.

The $\overline{\text{RST}}$ input pin can be used to hold off initialization of the device if asserted prior to power on reset, or to create the equivalent of a power on reset if asserted after power has been applied. The input pin can be configured to perform either a system reset, power-on-reset, or a simulated full initialization. See the *External RST Pin* section of the *System Control* chapter in the device data sheet for specific details.

The $\overline{\text{RST}}$ pin should never be left floating. It can be driven from a voltage supervisor or other control chip. It can be connected to an external RC combination or it can be pulled up using a 1-kΩ to 100-kΩ resistor connected to V_{DD}.

The $\overline{\text{RST}}$ pin input contains a glitch filter to prevent noise from causing a system reset.

The $\overline{\text{RST}}$ input pin is one of several device reset controls. See the *System Control* chapter in the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for details.

Because the $\overline{\text{RST}}$ signal routes to the core as well as most on-chip peripherals, it is important to protect the $\overline{\text{RST}}$ signal from noise. This protection is particularly important in applications that involve power switching where fast transitions can couple into the reset line. The reset PCB trace should be routed away from noisy signals. Do not run the reset trace close to the edge of the board or parallel to other traces with fast transients.

If you choose to use a capacitor it should be located as close to the pin as possible.

If the $\overline{\text{RST}}$ signal source is another board, it is recommended to add a buffer IC on the MSP432E4 board to filter the signal.

A simple push-switch can be used to provide a manual reset. To protect against possible device damage due to electrostatic discharge and to avoid ringing on the $\overline{\text{RST}}$ signal caused by switch bounce and stray inductance, add a low-value resistor (100 Ω) in series with the switch.

Reset circuit options are shown in the data sheet.

3.6 Crystal Oscillators

This section describes design considerations related to the microcontroller oscillators.

3.6.1 Crystal Oscillator Circuit Components

The following sections describe the components for the crystal oscillator circuit.

3.6.1.1 Main Oscillator Circuit

The MSP432E4 family of microcontrollers has a main oscillator circuit that can be used as a clock source for the device. This clock source is required for parts that contain and use the USB, Ethernet, or CAN interfaces.

MSP432E4 MCUs that support the integrated Ethernet PHY require a 25-MHz crystal on the main oscillator circuit. If the integrated Ethernet PHY is not used, any of the supported crystals as specified in the data sheet can be used.

Some of the MSP432E4 MCUs bring the GNDX2 signal of the main oscillator circuit out to a pin on the part. When the GNDX2 signal is available, connect it to the digital ground plane for proper operation (see Figure 20). Early designs may show the crystal load capacitors and GNDX2 pin connected only to each other without a connection to digital ground. Either is a valid configuration, but the low-impedance connection to the digital ground helps isolate the circuit from external system noise sources.

When the GNDX2 signal has not been brought out to a pin, then it is connected to a GND pin internally. Connect these devices as shown in Figure 21.

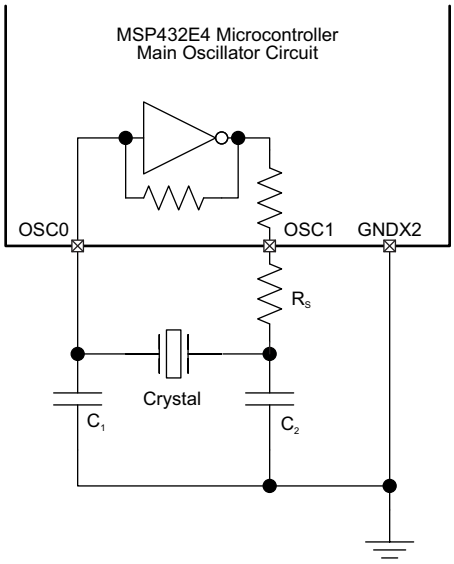


Figure 20. Main Oscillator Circuit With GNDX2

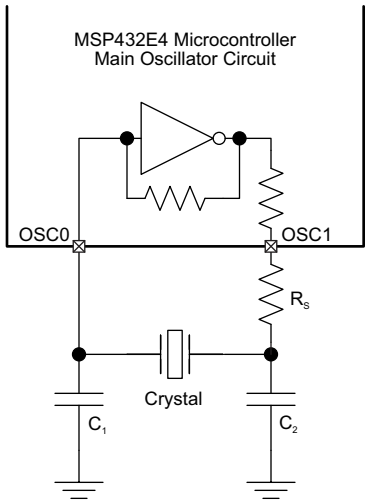


Figure 21. Main Oscillator Circuit Without GNDX2

The device-specific data sheet provides a list of recommended crystals that have been simulated to work with the main oscillator and includes recommended values for C_1, C_2, and R_S. It may be possible to substitute other manufacturer's crystals with like crystal parameters and frequencies. Crystals with C_L values of 18pF or greater or that support a maximum drive of less than 200µW are not robust enough to be used.

It is possible to use a single-ended clock source such as an external oscillator to drive the OSC0 input of the main oscillator circuit. See the device-specific data sheet for input specifications. When a single-ended clock source is used, leave the OSC1 pin unconnected and connect GNDX2, if present, to GND.

3.6.1.2 Hibernate Oscillator Circuit

Some MSP432E4 MCUs have a Hibernation module that runs from a 32.768-kHz clock source used to accurately clock the real time clock (RTC) circuit within the module even when only V_{BAT} is supplied to the system. See the data sheet for details on the Hibernation module and the hibernation clock source specifications.

There are many readily available crystals that meet the hibernation clock source specification in the data sheet, so there is no need to provide a specific recommended list.

Some MSP432E4 MCUs bring the GNDX signal of the hibernate oscillator circuit out to a pin. When the GNDX signal is available, connect it to the digital ground plane for proper operation (see Figure 22). Early designs may show the crystal load capacitors and GNDX pin connected only to each other without a connection to digital ground. Either is a valid configuration, but the low-impedance connection to the digital ground helps isolate the circuit from external system noise sources.

When the GNDX signal has not been brought out to a pin, then it is connected to a GND pin internally. For this configuration, implement the circuit shown in Figure 23.

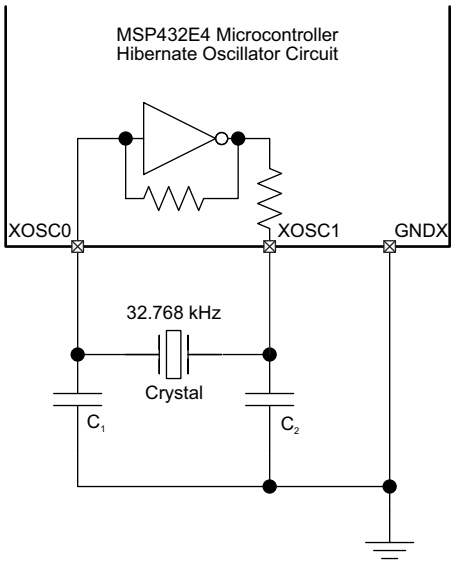


Figure 22. Hibernate Oscillator Circuit With GNDX

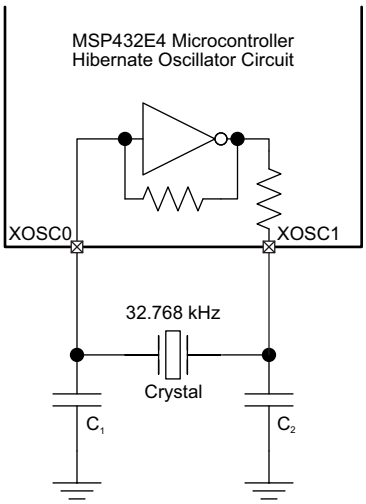


Figure 23. Hibernate Oscillator Circuit Without GNDX

Capacitors C_1 and C_2 must be sized correctly for reliable and accurate oscillator operation. Crystal manufacturers specify a load capacitance (C_L) which should be used in Equation 4 to calculate the optimal values of C_1 and C_2.

$$C_L = (C_1 \times C_2) / (C_1 + C_2) + C_S \quad (4)$$

C_S is the stray capacitance in the oscillator circuit. Stray capacitance is a function of trace lengths, PCB construction, and microcontroller pin design. For a typical design, C_S should be approximately 2 pF to 4 pF. Because C_1 and C_2 are normally of equal value, the calculation for a typical circuit simplifies slightly to Equation 5.

$$C_1 \text{ and } C_2 = (C_L - 3 \text{ pF}) \times 2 \quad (5)$$

C_1 and C_2 should stay within the maximum and minimum specifications listed in the hibernation clock source specifications section of the data sheet. Capacitors with an NP0/C0G dielectric are recommended and are almost ubiquitous for small-value ceramic capacitors.

It is possible to use a single-ended clock source such as an external oscillator to drive the XOSC0 input of the Hibernate oscillator circuit. See the data sheet for input specifications. When a single-ended clock source is used, leave the XOSC1 pin unconnected and connect GNDX, if present, to GND.

3.6.2 Crystal Oscillator Circuit Layout

The key layout objectives should be to minimize both the loop area of the oscillator signals and the overall trace length. A poor oscillator layout can result in unreliable or inaccurate oscillator operation and can also be a noise source. Ideal trace length is less than 0.25 in (6 mm). Do not exceed 0.75 in (18 mm).

Figure 24 shows a preferred layout for a small surface-mount crystal. The GND side of each capacitor routes directly to a via that provides a low-impedance connection to the GND plane.

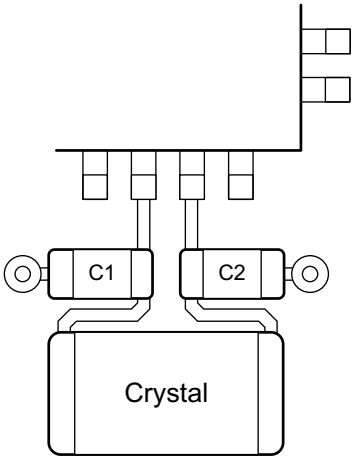


Figure 24. Recommended Layout for Small Surface-Mount Crystal

Some crystal circuits require a series resistor (R_S) to limit the drive power delivered to the crystal. This component should be a small chip resistor located between capacitor C_2 and the OSC1 pin of the device.

Figure 25 shows a recommended layout for a small surface-mount crystal for a device that contains a GNDX pin between the XOSC0 and XOSC1 signals. The GND side of each capacitor can share the via with the GNDX pin using a 10-mil trace to provide a low-impedance connection to the GND plane. If the distance between capacitors and the GNDX pin is greater than 200 mil, each should have its own via to GND.

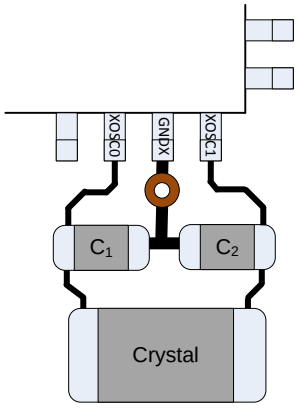


Figure 25. Recommended Layout for Crystal With GNDX Connection

3.7 JTAG Interface

This section describes design considerations related to the microcontroller JTAG interface.

3.7.1 Debug and Programming Connector

When designing a board that uses an MSP432E4 microcontroller, it is preferable to provide connections to all JTAG/SWD signals. In pin-constrained applications, SWD can be used instead of JTAG. SWD only requires two signals (SWCLK and SWDIO), instead of the four signals that JTAG requires, freeing up two additional signals for use as GPIOs. Check that your preferred tool-chain supports SWD before choosing this option.

The most common Arm® debug connector is a 2×10-way 0.1-in pitch header. Although it is robust, the 0.1-in header is too large for many boards and is considered legacy implementation. An alternate connector definition, which is now quite popular, uses a 0.05-in half-pitch 2×5 connector known as the Cortex® Debug Connector. Table 9 lists the applicable assignments for both connectors.

Table 9. Applicable Debug Connector Pin Assignments

JTAG or SWD Signal	Legacy Arm 20-Pin (0.1-in Pitch)	Cortex Debug Connector 10-Pin (0.05-in Pitch)
TCK/SWCLK	9	4
TMS/SWDIO	7	2
TDI	5	8
TDO/SWO	13	6
$\overline{\text{RESET}}$	15	10
GND	4, 6, 8, 10, 12, 14, 16, 18, 20	3, 5, 9
TVCC	1	1

The MSP432E4 microcontrollers have default internal pullup resistors on TCK, TMS, TDI, and TDO signals. External pullup resistors are not required if these connections are kept short. If the JTAG signals are greater than 2 in (51 mm) or routed near an area where they could pick up noise, TCK should be externally pulled up with a 10-kΩ or stronger resistor or pulled down with a 1-kΩ or stronger resistor to prevent any transitions that could unexpectedly execute a JTAG instruction.

3.8 CoreSight™ ETM Trace Port Connections

The MSP432E4 family of microcontrollers includes the Arm Embedded Trace Macrocell (ETM) for instruction trace capture. Trace data is output on pins TRD0 to TRD3 and clocked with TRCLK. See the data sheet to determine the GPIOs on which the trace signals are available. Arm defines a 2×10 0.05-in pitch connector with a key on pin 7 as a standard to interface to debuggers supporting JTAG with trace data capture. Figure 26 shows this connector definition with signal names corresponding to those found in the device-specific data sheet.

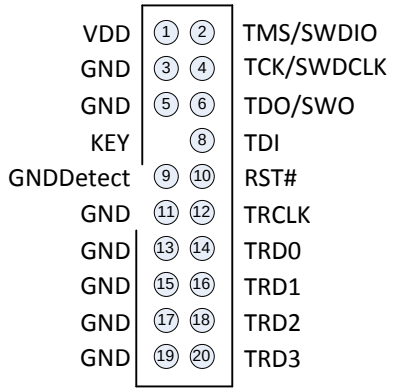


Figure 26. Cortex ETM Connector

On MSP432E4 MCUs, TRCLK runs at 1/2 of the system clock speed, which can be a high frequency. The traces for TRD0 to TRD3 and TRCLK should be less than 6 in (152 mm) in length. The TRCLK and TRD0 to TRD3 I/O pads should be configured for 8-mA drive strength initially and reduced on an individual basis if needed.

On some MSP432E4 microcontroller development kits, the 2×10 0.05-in pitch connector is used, but PA1 (U0TX) is connected to pin 14 (TRD0) and PA0 (U0RX) is connected to pin 16 (TRD1) to provide a debug UART interface to the onboard ICDI.

3.9 System

This section describes system-level design considerations related to the MSP432E4 family of microcontrollers.

3.9.1 I/O Drive Strengths

The MSP432E4 microcontrollers have GPIO pads with programmable drive strength. For outputs driving high-speed buses, capacitance loads greater than 15 pF, or LEDs, the 8-mA drive strength should be selected. Higher drive strengths can be selected based on the V_{OL}, V_{OH}, and total GPIO current per side limits given in the data sheet.

Some GPIO pads are limited to 2-mA drive strength. If these pads are to be used as outputs, they should be limited to capacitance loads less than 15 pF or signals that can support the longer rise and fall times associated with a 2-mA drive strength. See the device-specific data sheet for a list of GPIO pins that support only 2-mA drive.

The GPIOs that are shared with the USB functions USB0DP and USB0DM are fixed at 4-mA drive strength and cannot be configured as open drain. These limitations must be considered if these pins are used as outputs.

3.9.2 Series Termination Resistors

Series termination resistors provide two different functions. The first function is for outputs with fast rise and fall times driving light loads to help match the output impedance of the driver to the impedance of the net being driven. This configuration helps with several items:

- Lower overshoot or undershoot at the input destination.
- Reduce ringing near the transition region of the input that could cause false clocking or timing violations.
- Limit crosstalk induced on neighboring signals.
- Reduce EMC emissions.

Output series termination is best placed within 0.5 in (12.7 mm) of the output pin. The values used are system dependent but are often 0 Ω, 10 Ω, 22 Ω, or 33 Ω.

The second function of series termination resistors is to protect input and output pins from ESD strikes by limiting the currents and voltages seen at these pins. This protection is particularly important for signals that go to connectors that are exposed outside the system and for signals that go through connectors to other boards or cables that remain in the system. Higher-speed signals that go from board to board typically have resistor values of 10 Ω to 33 Ω. Lower-speed signals that connect to cables or external connectors typically have resistor values of 50 Ω to 150 Ω.

3.9.3 ESD and EMC Protection

Any signal from the MSP432E4 microcontroller that is exposed outside the system enclosure through a connector should have ESD protection. Common examples are Ethernet and USB signals. Section 4.1 describes ESD protection for Ethernet. Section 4.3 describes ESD protection for USB.

In some system environments, signals that stay internal but come through a connector from another board or cable can be subject to radiated noise from electrical noise sources such as motor drivers, relays, and other power-switching circuits. Radiated noise is particularly a concern for two-layer boards that do not have a solid ground plane to shield the signals from this type of noise. For signals that fall into this category, TI recommends including PCB footprints in the design to allow for the components in Figure 27 or Figure 28. Package options for the TVS diodes that support multiple I/O are also available.

The exact resistor values and TVS diode configuration highly depends on the system and environment. Timing requirements of the interface, input or output signal direction, exposure to electrical noise sources, and IEC test level must be taken into account when determining what values to use.

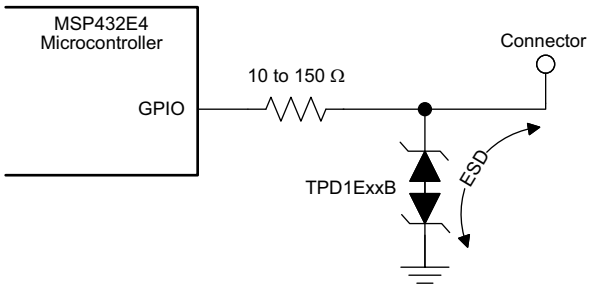


Figure 27. General ESD Protection Using Bidirectional TVS Diode

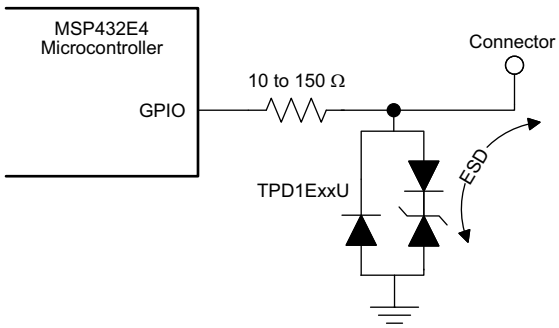


Figure 28. General ESD Protection Using Unidirectional TVS Diode

Table 10 lists some recommended TI ESD protection options for use with the MSP432E4 microcontrollers.

Table 10. ESD Protection Options

Part Number	Description
TPD1E10B06	Bidirectional ESD protection for low-speed I/O with ±6-V breakdown voltage and 12-pF I/O capacitance
TPD1E05U06	Unidirectional ESD protection for high-speed I/O with 6.5-V breakdown voltage and 0.45-pF I/O capacitance
TPD2E001	2-channel low-capacitance ESD protection array for high-speed data interfaces
TPD4E1B06	Quad channel high-speed ESD protection (device side Ethernet)
TPD4S012DRYR	4-channel ESD protection for USB-HS or USB OTG

3.9.4 Interrupt Pin Selection

Any GPIO pin in the microcontroller can be used as an interrupt input pin. In most cases, there is one interrupt vector per GPIO port, so the interrupt service routine must check status registers to determine which port pin generated the interrupt. The system designer must determine if it is more desirable to group more than one interrupt within a GPIO bank or separate interrupts to unique GPIO banks. Some MSP432E4 microcontrollers have one or two GPIO banks where each individual pin in that bank has a unique interrupt vector. See the device-specific data sheet to determine which GPIO pins have this capability.

3.9.5 Clock Routing

Pay special attention to any pins or nets that are used as clock signals. The cleanest clock is one that routes directly from an output pin to an input pin without stubs, tees, or multiple destinations. Consider the following guidelines when routing clock signals:

- Give clock traces twice the spacing of other signals. For example, if a 7-mil trace with 7-mil space routing rules are being used, give 14-mil spacing between the clock and any other signal. This distance limits crosstalk from neighboring nets.
- Add a footprint for a series resistor close to the clock output pin to adjust for any ringing or EMI concerns beyond what changing the I/O drive strength can do. Typical series resistor values are 0 Ω, 10 Ω, 22 Ω, or 33 Ω.
- If probe points are added for clocks, place them as close as possible to the clock destination. Consider adding a ground point nearby for ease of measurement. Clock signals are noisiest near the middle of the net due to reflections. Clocks measured at a location other than the destination are usually not representative of how the signal appears at the destination.
- When routing a clock to multiple destinations, try to group the destination points in the same area. In most cases, it is best to daisy-chain route the clock instead of tee routing the clock to the destinations. Tee routing generally causes greater reflections unless carefully balanced.
- When routing a clock to multiple destinations, place the most timing sensitive and critical of the destination devices at the end of the net where the clock is the cleanest.
- The clock should follow the same general path as the data and control signals associated with the interface it clocks to help maintain any relative bus timings.

- Avoid crossing splits in the ground or power plane with clock signals.

NOTE: Clocks that are open collector, such as I^2C clocks running at 400 kHz, have a very slow rise time and are designed for multiple drops. The previous guidelines are not meant to restrict such clocks.

3.9.6 5-V Tolerant Inputs

The MSP432E4 microcontrollers do not have 5-V tolerant GPIO inputs with the exception of PB1, which is used as USB0VBUS. See the device-specific data sheet for details on this input.

3.9.7 Unused Pins

The preferred connection for an unused microcontroller pin depends on the pin function. Each data sheet lists the fixed function pins as well as both the acceptable practice and the preferred practice for reduced power consumption and improved electromagnetic compatibility (EMC) characteristics. If a module is not used in a system, and its inputs are grounded, it is important that the clock to the module is never enabled by setting the corresponding bit in the RCGCx register.

3.9.8 Errata Documentation

Part of any good system design includes reviewing and understanding any errata associated with the revision of device being used. The MSP432E4 SimpleLink™ Microcontrollers Silicon Errata describes any deviations from the data sheet. These advisories must be followed to ensure correct device operation.

3.10 All External Signals

This section describes design considerations related to signals that connect directly from the microcontroller to a connector that takes the signal to another board or external device.

The system design must ensure that the ground reference of any incoming signal is the same as the microcontroller ground. If the grounds do not match, the signal level seen at the input pin of the microcontroller might be significantly higher than what the data sheet specifies. Ground connections between boards should be low impedance and as short as possible.

The system design should avoid routing the V_{DD} 3.3-V supply that connects to the microcontroller directly to a connector pin that can be subject to ESD or EMC radiated emissions. If V_{DD} does need to be routed to a connector, route it through a ferrite bead and optionally a TVS diode.

Do not drive I/O signals that are sourced from cables or other boards before applying power to the microcontroller unless the strict guidelines for injection current and voltage limits from the data sheet are followed.

Implement layout options for ESD protection on external I/O signals that come directly from the microcontroller, as described in Section 3.9.3.

4 Feature-Specific Design Information

This section contains feature-specific design information and is grouped by function or peripheral:

- Ethernet PHY
- Ethernet MII/RMII
- USB
- USB ULPI
- SSI Buses
- UART
- I2C/SMBUS
- ADC
- Comparators

- Timer/PWM
- External Peripheral Interface (EPI)
- LCD Controller
- Quadrature Encoder Interface (QEI)
- GPIO
- Hibernation Signals

4.1 Ethernet Internal PHY

This section describes design considerations related to the MSP432E4 internal Ethernet PHY and details related to the network or Medium Dependent Interface (MDI) connection.

The MDI connection is accomplished through the transmit (EN0TX0P and EN0TX0N) and receive (EN0RXIP and EN0RXIN) differential pair pins. These signals connect to a termination network, then to 1:1 magnetics (transformer) then through TVS diodes for ESD protection and to an RJ-45 (see Figure 29). These names reflect the default functions. In fact, the receive and transmit pairs are identical and can perform either function because the Internal Ethernet PHY supports MDI/MDX.

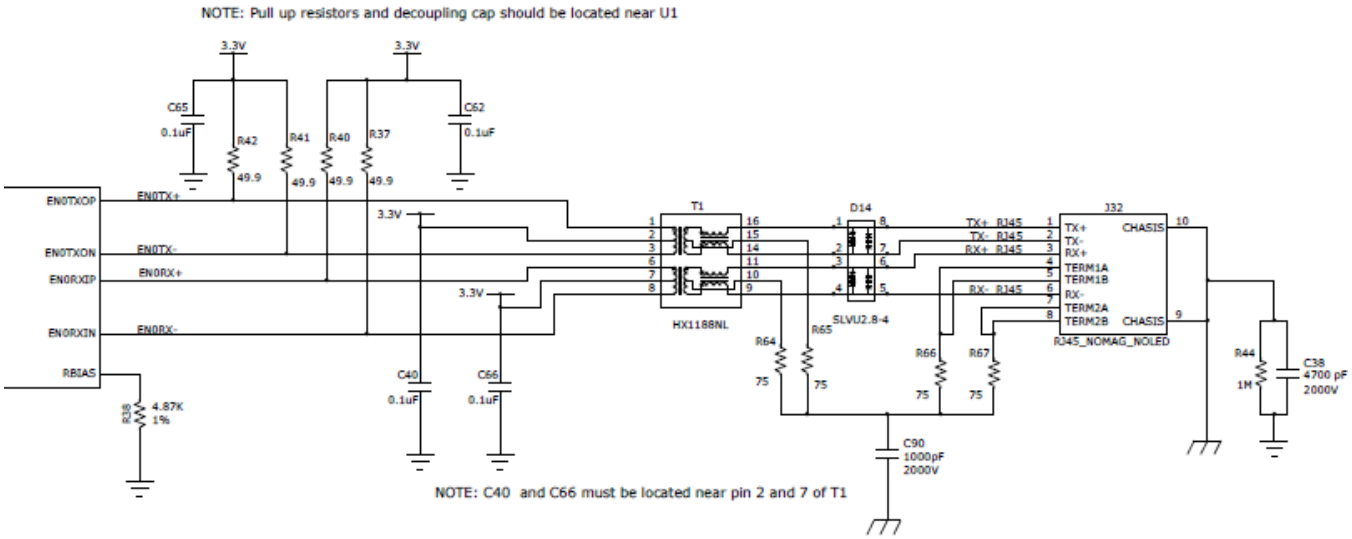


Figure 29. 10/100 Mbps Twisted Pair Interface Using Separated Magnetics

4.1.1 Termination Resistors

Four pullup resistors are required for terminating and biasing the Ethernet transceivers. See R40, R41, R42 and R37 in Figure 29. These resistors should be connected from the EN0TXOP, EN0TXON, EN0RXIP, and EN0RXIN signals to 3.3 V. The specified value for these resistors is 50 Ω. The recommended, commonly available value is 49.9 Ω, 1%. Do not use resistors with a tolerance greater than 1%. Resistor power dissipation is low because the peak voltage on the resistor is only approximately 1 V in 100-Mbps mode and 2.5 V in 10-Mbps mode. Small, 0402 (1005 metric) surface-mount resistors have an acceptable power rating.

4.1.2 Isolation Transformer

The transformer used in the MDI connection provides DC isolation between local circuitry and the network cable. The device-specific data sheets list both the part number and manufacturer's name for approved Ethernet transformer (*magnetics*) options. Other parts can be approved by similarity, but TI highly recommends checking with the manufacturer for their assessment of suitability. TI recommends magnetics with integrated common-mode choking devices to help with EMI performance.

The center tap of the transformer (microcontroller side of the transformer) should be connected to 3.3 V. Each connection point to the 3.3-V rail must be adequately filtered with a capacitor (0.1 µF or greater) if a solid power-plane is present (C40, C60 in Figure 29). If the center tap connects to a PCB trace instead of a plane, the capacitor value should be 1 µF or greater.

The center tap of the isolated windings (RJ-45 side of the transformer) has Bob Smith Termination through 75-Ω resistors (R64 and R65 in Figure 29) and a 1000-pF capacitor (C90 in Figure 29) to chassis ground. The termination capacitor should be rated to a voltage of at least 2 kV.

In certain applications, an alternate method of connecting the internal PHY to another device may be desirable. Specifically, designs for applications in which a backplane is the choice of media between devices. In these applications, DC isolation must be maintained while providing an AC signal-coupling path by using capacitors for the connection instead of magnetics. This type of configuration is not IEEE-compliant, and data sheet specifications are not ensured. For details on the transformerless configuration, see TLK110 Ethernet PHY Transformerless Operation.

4.1.3 RJ-45 Connections

Use of a metal-shielded RJ-45 connector with the shield connected to chassis ground is recommended to improve EMI performance.

Bob Smith Termination to the RJ-45 connector involves 75-Ω termination resistors connected to the unused differential pair connections on the RJ-45 connector (R66 and R67 in Figure 29). Bob Smith termination is used to reduce noise resulting from common mode current flows and to reduce susceptibility to any noise from unused wire pairs on the RJ-45.

NOTE: A modified Bob Smith termination is required for Power Over Ethernet (PoE) applications, which consists of DC blocking capacitors in series with the 75-Ω termination resistors.

4.1.4 RBIAS Resistor

A resistor is required on the RBIAS pin (R38 in Figure 29) to set the bias voltage for the Ethernet module. The bias resistor is a 4.87-kΩ 1% resistor and must be located close to the microcontroller pin [ideally less than 0.25 in (6 mm)]. The other resistor terminal should have a very short trace directly to GND. The trace or via for the GND connection should not be shared with any other pin. An incorrect value of RBIAS resistor results in incorrect amplitude on the transmit differential pair.

4.1.5 Crystal Requirements

To use the internal Ethernet PHY, the main oscillator circuit of the microcontroller must be driven with a clock source of 25 MHz ±50 ppm. See Section 3.6 for additional details about the main oscillator circuit.

4.1.6 Ethernet ESD

TI strongly recommends ESD protection for the MDI differential pairs. One recommended solution is the SLVU2.8-4 TVS diode array (D14 in Figure 29). This device is placed on the differential lines between the transformer and the RJ45 connector. The JEDEC SO-8 package is well suited for routing the transmit and receive differential pairs.

A second solution that can be placed on the device side of the transformer between the termination resistors on the differential pairs and the transformer is the TPD4E1B06. This device is not shown in Figure 29.

4.1.7 Ethernet LEDs

The LEDs associated with the internal Ethernet PHY (EN0LED0, EN0LED1, EN0LED2) are multiplexed in several locations with some of the microcontrollers GPIOs (see the device-specific data sheet). Any of the EN0LEDx signals can perform any of the internal Ethernet PHY LED functions.

The EN0LEDx signals can be connected such that current is sourced from the GPIO through a resistor and into the anode of an LED (see Figure 30) or the GPIO can be connected to the cathode of the LED and sink current (see Figure 31). All EN0LEDx signals must be wired up in the same manner. It is common to have LEDs as part of the RJ-45, which are connected the same as discrete LEDs.

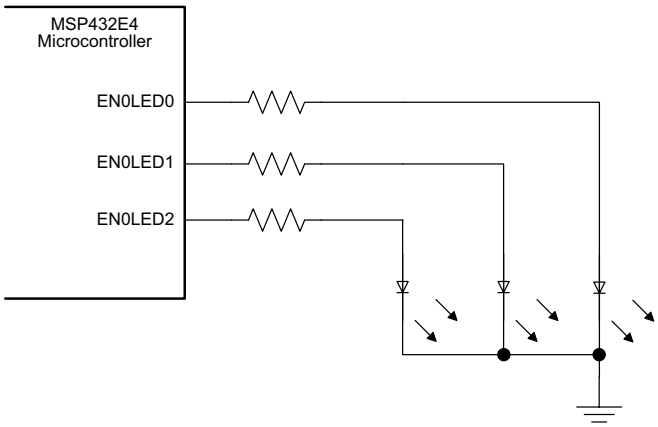


Figure 30. GPIO Sourcing LED Current

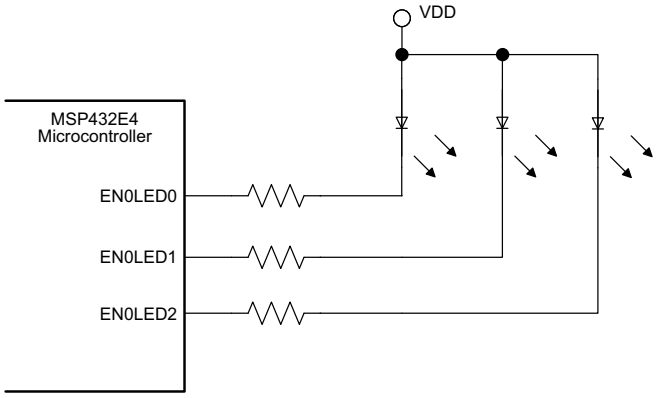


Figure 31. GPIO Sinking LED Current

4.1.8 Ethernet PHY PCB Layout

Good PCB layout and routing practices are important to ensure reliable Ethernet signaling, as shown in the example in Figure 32.

Follow these design rules and recommendations when routing the MDI interface of the Integrated Ethernet PHY for best results:

- Route the transmit and receive differential pairs on the top layer with a trace width and differential spacing tuned to the PCB stack-up for 100-Ω differential impedance as described in Section 3.2.3.2.
  - It may be difficult to implement a trace geometry that achieves both 100-Ω differential impedance and 50-Ω single-ended impedance. The most critical parameter to optimize in this design is the 100-Ω differential impedance.
- Follow the recommendations for routing differential pairs as described in Section 3.3.8. The individual traces within the differential pair should be length matched to within 0.05 in (1.27 mm).
- Separate the Ethernet transmit pair from the receive pair by at least 0.050 in (1.27 mm). This requirement is necessary to avoid cross-coupling between the RX and TX pairs.
- Place Ethernet termination resistors as close as possible to the microcontroller.
- Place the Ethernet transformer within 1 in (2.54 mm) of the RJ-45 connector.
- Place 0.1-µF capacitors close to the Ethernet transformer (see C40 and C66 in Figure 32).
- A continuous ground plane is a good PCB design practice; however, there are special considerations when using planes and copper pours near Ethernet signals. The following restrictions apply only to Ethernet circuits.
  - Do not extend the ground plane under the transformer unless the transformer is shielded on all sides.
  - Do not extend the ground plane under the signals from the transformer to the connector (see the lack of a ground plane under T1, D14, and J8 in Figure 32).
  - Do not extend the power plane (that is, the V_{DD} plane) under the Ethernet signals unless there is a solid ground plane between the differential Ethernet signals and the power plane.
  - Make sure there are no ground plane discontinuities under or near the differential signals between the microcontroller and the transformer.
  - Create a chassis ground to which the metal shield of the RJ-45 is connected and the Bob Smith termination is connected (see Section 3.3.6).

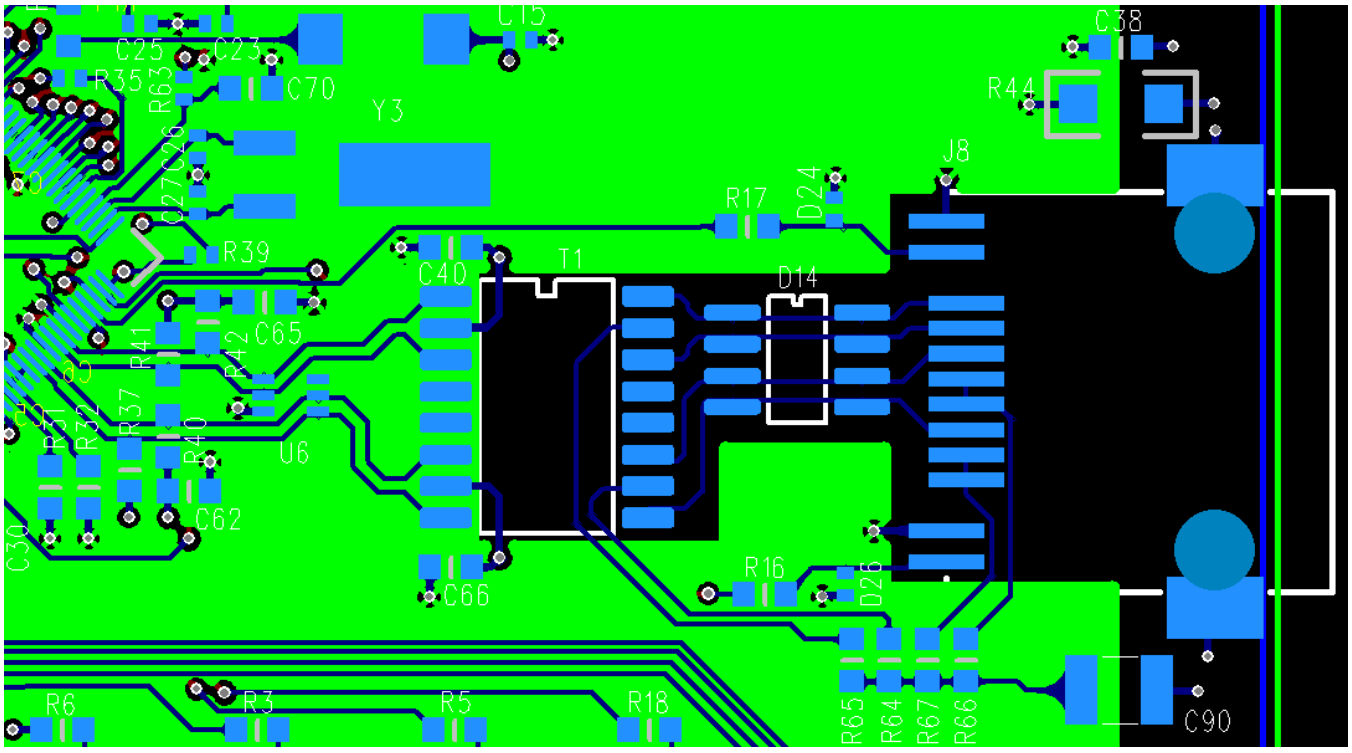


Figure 32. Ethernet PHY PCB Layout

4.2 External Ethernet PHY Interface

An external Ethernet PHY interface is available on some MSP432E4 microcontrollers. This interface connects the Ethernet Media Access Controller (MAC) within the microcontroller to an external Ethernet PHY. Data transfer occurs over the Media Independent Interface (MII) or the Reduced MII (RMII). The external Ethernet PHY register space is accessed using the Management Data Input/Output (MDIO) interface. The MDIO interface is made up of the EN0MDC and the EN0MDIO pins. Each PHY connected to the MDIO interface must have a unique address. The internal Ethernet PHY is configured for address 0 leaving addresses 1 to 7 for any external Ethernet PHY. See the data sheet of the external Ethernet PHY being used to determine how to configure the MDIO address of the PHY.

The interrupt from the external Ethernet PHY should be connected to the EN0INTRN pin function of the microcontroller. See the data sheet for full details on the MAC interface signals.

4.2.1 MII

The MII signals include EN0TXCK, EN0TXD[3:0], EN0TXEN, EN0RXCK, EN0RXD[3:0], EN0RXDV, EN0RXER, EN0COL and EN0CRS. EN0TXCK and EN0RXCK are generated from the external Ethernet PHY and run at 2.5 MHz for the 10Base-T communication speed and 25 MHz for the 100Base-T communication speed.

The MII signal trace lengths should be kept as short as possible, ideally less than 6 in (15.24 cm). TI recommends trace length matching across the MII bus signals to within 2.0 in (5.08 cm). Significant differences in the trace lengths can cause data timing issues.

GPIO drive strength for the MII signals should be set to 8 mA to achieve timings specified in the data sheet. Series resistors are recommended on the MII signals to prevent ringing and EMI concerns.

4.2.2 RMII

The RMII signals include EN0REF_CLK, EN0TXD[1:0], EN0TXEN, EN0RXD[1:0] and EN0RXDV. The RMII interface runs at a constant 50 MHz. EN0REF_CLK is a 50 MHz ±50 ppm input to both the MSP432E4 microcontroller and the external Ethernet PHY. It is important that both the microcontroller and the external PHY receive a clean clock edge from the external clock source such as an oscillator. If the microcontroller and the external PHY are close together, this can be accomplished by a well balanced tee-route. If they are more than 2 in (5.08 cm) apart, a low-skew low-jitter clock buffer such as the CDCLVC1102 can be used to provide a clean clock to the two destinations.

The EN0RXDV has a slightly different function in RMII mode compared to MII mode. In RMII mode, the EN0RXDV combines Carrier Sense and Receive Data Valid functions. See the data sheet of the external Ethernet PHY to determine the correct location to connect this signal to when in MII mode.

On some MSP432E4 MCUs, the RMII signals are available on two sets of pins. However, there is only one MAC in the microcontroller. If the user wishes to connect two external Ethernet PHYs using RMII, only one interface can be enabled at a time.

The RMII signal trace lengths should be kept as short as possible, ideally under 6 in (15.24 cm). TI recommends trace length matching across the RMII bus signals to within 2.0 in (5.08 cm). Significant differences in the trace lengths can cause data timing issues.

GPIO drive strength for the RMII signals should be set to 8 mA to achieve timings specified in the data sheet. Series resistors are recommended on the RMII signals to prevent ringing and EMI concerns.

4.3 USB

The MSP432E4 family includes microcontrollers that support an internal USB 2.0 PHY capable of full-speed operation. See the data sheet of the device being used to determine which of the following configurations the device supports: the internal PHY supports USB Device, USB Embedded Host, and USB OTG operation.

The MSP432E4 microcontrollers also have the ULPI that interfaces to a external high-speed PHY, as described in Section 4.4.

The critical component of the internal USB PHY is the bidirectional differential data pins USB0DM (D-) and USB0DP (D+). Follow these design rules and recommendations when routing the USB differential pair for best results:

- Route the USB differential pair on the top layer with a trace width and differential spacing tuned to the PCB stack-up for 90-Ω differential impedance as described in Section 3.2.3.2.
  - It may be difficult to implement a trace geometry that achieves both 90-Ω differential impedance and 45-Ω single-ended impedance. The most critical parameter to optimize in this design is the 90-Ω differential impedance.
  - The trace width and spacing to maintain the required 90-Ω differential trace impedance directly at the pins of the microcontroller and directly at the ESD suppressor and USB connector may not be possible to achieve. Minimize these deviations as much as possible, being sure to maintain symmetry.
- Follow the recommendations for routing differential pairs as detailed in Section 3.3.8. The individual traces within the differential pair should be length matched to within 0.150 in (3.81 mm).
- Avoid stubs when adding components to D+ and D– signals. Devices such as ESD suppressors should be located directly on the signal traces (see Figure 16).
- Maintain symmetry when routing differential pairs. Some PCB layout tools can assist with this kind of routing. Avoid vias if possible. If it is necessary to switch layers, then both signals in the pair should pass through a via at the same distance on the trace.
- Limit the total trace length for the USB differential pair to 12 in (30.48 cm).
- Place ESD suppressors as close as possible to the USB connector to minimize any areas of impedance discontinuities. See Table 10 for recommended ESD suppressors.
- For best ESD and EMI performance, create a chassis ground to which the metal shield of the USB connector is connected, as shown in Section 3.3.6.
- Depending on the system design, a common-mode choke may be helpful to pass EMI testing. An

ACM2012 common-mode choke by TDK is one recommended device. If EMI is a concern for the design, it is recommended that a footprint for the choke be included in the design placed close to the USB connector. Figure 33 shows how two 0805-sized resistors (R29, R30) can be placed and later replaced with an ACM2012 choke if needed during system EMI testing.

- High Speed USB Platform Design Guidelines includes more details on using a common-mode choke and can be found at http://www.usb.org.

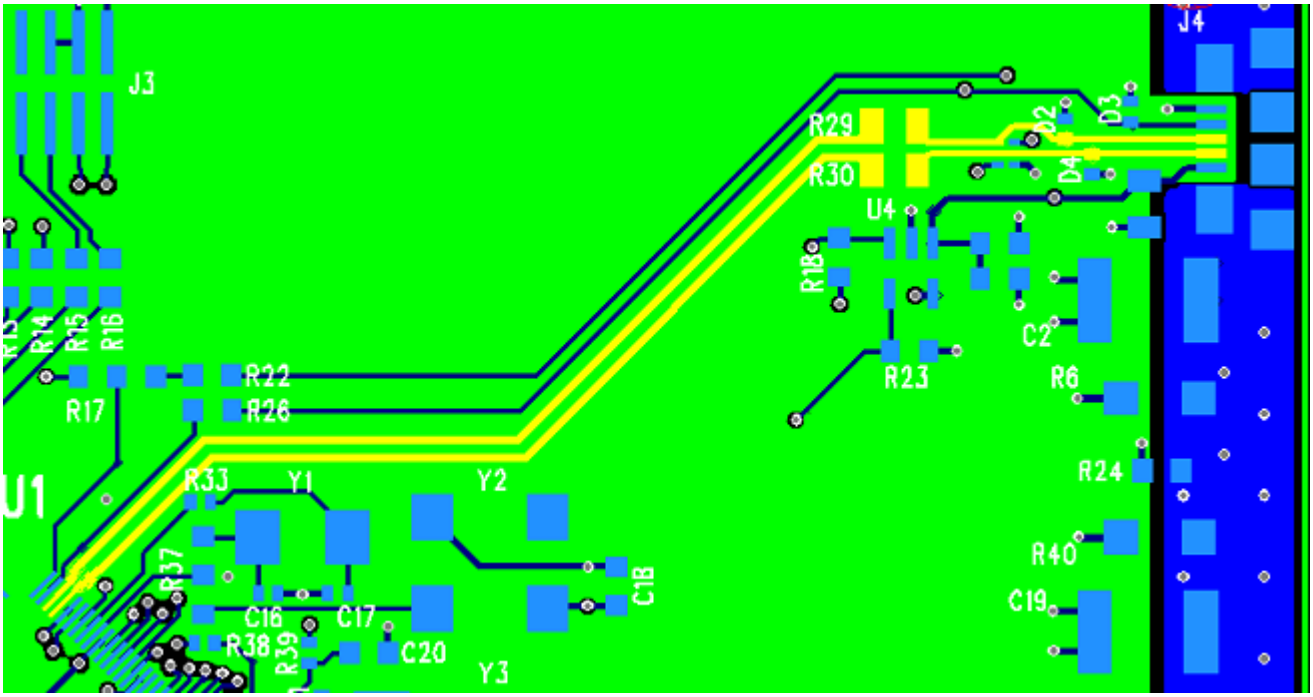


Figure 33. USB Routing Example

4.3.1 USB Device

For MSP432E4 MCUs that are used in a USB device configuration, the only signal used in addition to USB0DM and USB0DP is a GPIO to detect when 5 V is applied to or removed from the VBUS pin on the USB connector. For self-powered USB devices, software should monitor this GPIO and manage the internal USB PHY accordingly. If the microcontroller power is sourced or enabled by the VBUS pin on the USB connector, this GPIO connection is not needed. The only 5-V tolerant GPIO on MSP432E4 MCUs is PB1. For MSP432E4 MCUs that support OTG functionality, USB0VBUS is multiplexed with PB1 and should be enabled and used by software, because it is directly connected to the internal USB PHY.

When used in a USB device configuration, a 100-Ω resistor should be placed in series between VBUS on the USB connector and PB1 on the microcontroller to limit damage which might be caused by an ESD event.

If PB1 must be used for a function other than USB0VBUS, any other available GPIO could be used in its place. Because no other GPIO pins are 5-V tolerant, a 5.6-kΩ ±5% resistor in series with a 10-kΩ ±5% resistor should be wired as a voltage divider between VBUS on the connector and ground. This circuit drops the 5-V VBUS value to 3.2 V at the GPIO pin.

4.3.2 USB Embedded Host

For MSP432E4 MCUs that are used in a host configuration, the USB0EPEN and USB0PFLT signals may be used in the design in addition to USB0DM and USB0DP. These two signals typically connect to a power switch such as a TPS2051B, which controls power to the USB connector of the host. See the MSP432E4 device-specific data sheet to determine the ports on which these functions are available.

4.3.3 USB OTG

MSP432E4 MCUs that support USB OTG mode include the signals for USB Device mode, signals for USB Host mode and an additional signal USB0ID located on pin PB0. This USB ID signal is the 5th pin found on a USB micro-AB connector. If a micro-A cable end is plugged into this connector, the ID pin on the cable is tied to ground causing the MSP432E4 device to operate as a USB host. If a micro-B cable end is plugged into the USB connector, the ID pin is left floating. In this case, the internal pullup on the USB0ID signal causes the MSP432E4 MCU to operate in device mode.

To limit damage from ESD events, a 100-Ω resistor should be placed in series between the ID pin on the USB connector and USB0ID (PB0) on the microcontroller.

VBUS from the USB connector must be directly connected to USB0VBUS (PB1) of the microcontroller without a series resistor in between. In this case, USB0VBUS should be connected to an ESD suppressor such as a TVS diode, or ESD resistant VBUS switch.

4.4 USB ULPI External PHY Interface

MSP432E4 MCUs that support USB and ULPI can attach to an external USB PHY. ULPI uses 12 pins to interface between the USB controller within the microcontroller and an external PHY. The ULPI specification and additional information on ULPI can be found at the ULPI working group page.

ULPI uses a 60-MHz clock. Standard operation is for the USB PHY to generate the clock. Optionally, the PHY can receive the clock as an input. The MSP432E4 microcontroller can be configured to use the input clock from the USB PHY or to output the 60-MHz clock to the USB PHY. A option for populating a series resistor should be placed at the source device for the ULPI clock to address any system EMI issues found during systems test.

ULPI timings of both the MSP432E4 microcontroller and the external USB PHY must be reviewed and a timing budget for both control timings and data transfers should be developed to determine the best clocking scheme and maximum distance the microcontroller can be from the external USB PHY. Typically, the distance is 6 inches or less and the traces for ULPI must be length matched within 500 mils of each other.

Configure ULPI pins for 12-mA drive strength to meet timings.

4.5 SSI Buses

All of the SSI buses can communicate in advanced, bi-, or quad-SSI mode. SSI0 bus is located on GPIO port A, SSI1 bus is located on GPIO port B and port E, SSI2 bus is multiplexed between GPIO port D or port G, and SSI3 is multiplexed between using GPIO port F or port Q and port P (if using Quad SSI). All SSI buses have equivalent functionality.

Due to errata number SSI#03, SSI1 bus can be used only in legacy mode (see the MSP432E4 SimpleLink™ Microcontrollers Silicon Errata).

If the SSI bus is used, a 10-kΩ pullup should be placed on SSIxFSS to prevent any unexpected accesses before code booting and the pins being configured.

For all SSI buses, when in legacy mode SSIxXDAT0 is SSIxTX (output), SSIxXDAT1 is SSIxRX (input). If using quad-SSI mode, SSIxXDAT2 and SSIxXDAT3 are used and a 10-kΩ pullup to V_{DD} should be placed on these pins for proper operation until the flash is configured for quad access.

If operating at the maximum 60-MHz clock rate into the maximum load of 25 pF, select the 12-mA drive strength for all outputs to meet data sheet timings. Use series termination for any outputs.

4.6 UART

Eight UART modules (U0 to U7) are available on MSP432E4 devices. Basic RX and TX functionality is the same between them. The following are important considerations when selecting UART pins to use:

- Example software commonly uses U0RX on PA0 and U0TX on PA1 for debug messages and input. If a debug port is to be implemented, this location is recommend.
- UART0 and UART1 offer modem flow control and modem status, UART2 to UART4 offer modem flow control, and UART5 to UART7 offer only RX and TX.

4.7 I²C

An MSP432E4 MCU can have up to ten I²C buses. The buses appear on the I2C0SCL to I2C9SCL and I2C0SDA to I2C9SDA signals. Each bus is functionally equivalent to the others and can be either a master or a slave. See the *Inter-Integrated Circuit (I2C) Interface* chapter of the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for detailed information.

The I²C bus requires signals to be configured in open-collector mode. The I2CSDA pin requires the associated GPIO to be configured as an open-collector signal in the GPIOODR register. The I2CSCL pin should not be configured in this manner, as the pad is designed differently. The GPIOPinTypeI2C() API should be used for the I2CSDA pin, and the GPIOPinTypeI2CSCL() API should be used for the I2CSCL pin. The I²C pins must be externally pulled up to 3.3 V for proper operation. Typical pullup values are 2.2-kΩ resistors, but the value depends on bus speed and total bus capacitance. See the *Pull-up resistor sizing* section of the I2C-bus specification and user manual from NXP for details on how to calculate the minimum and maximum pullup resistor values.

Only 3.3-V I²C buses are directly supported. 5-V and 1.8-V buses can be supported with the use of external level shifters.

An I²C bus that is pulled up and connected to a 3.3-V power rail different from the one attached to the V_{DD} of the MSP432E4 MCU can be pulled low by the ESD structures of the MCU when V_{DD} to the device is not powered.

4.7.1 Routing Considerations

An I²C bus should be routed such that the I2CxSCL and I2CxSDA signals follow similar layer transitions and stay within approximately 1000 mil of each other. It is not recommended that these signals be routed as a differential pair and there is no length-matching requirement for them.

I²C signals should not be routed next to signals that can cause significant cross talk to the I2CxSCL signal. Cross talk noise could interfere with the I²C transaction and cause a bus error requiring an I²C bus reset.

4.8 ADC

This section describes design considerations related to the ADC module.

4.8.1 ADC Inputs

To achieve the best possible conversion results from an ADC, it is important to start with a good schematic design.

All ADCs require a voltage reference (or occasionally a current reference), whether the voltage reference is provided from an on-chip source or through an external pin. Any deviation in the reference voltage from its ideal level results in additional gain error (or slope error) in the conversion result.

For optimal ADC performance, a precision voltage source should be used to supply the V_{REF+} pin when available as a separate pin on the part or V_{DDA} pin on parts that have V_{REF+} internally connected to V_{DDA}. See Section 3.4.5 for additional details on the filter capacitance required for ADC performance. See the device-specific data sheet for I_{VREF} specification maximum that the precision voltage source must supply.

Up to 24 pins on the MSP432E4 devices support analog inputs AIN00 to AIN23. All inputs can be used in single-ended mode, while differential mode is supported for consecutive even-and-odd pairs. All analog inputs are equivalent in function and capability. Selection of which analog inputs to use should be based on ease of PCB routing and pin muxing selection.

Optimal ADC accuracy is achieved with a low-impedance source (R_S) and a large input filter capacitor (C_S) (see Figure 34). As the signal source impedance increases and capacitance decreases, noise on the conversion result increases. Noise sources include coupling from other signals, power supplies, external devices, and from the microcontroller itself.

See the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for specifics on the analog input impedance with respect to the sample-and-hold circuit. A 500-Ω effective input impedance (Z_S) is required to support the maximum input sampling period of 250 ns. This input impedance allows the voltage on the ADC input pin to charge C_{ADC} to the input pin voltage going through R_{ADC}. See Figure 34 for the ADC input equivalency diagram, and see the data sheet for the values of C_{ADC} and R_{ADC}.

If voltage rails are to be monitored, adequate capacitance is required to hold the voltage during the sampling period. The exact amount of capacitance (C_S) depends on the accuracy required, the amount of time between samples, and the resistor values used for any voltage divider circuit.

The MSP432E4 MCUs allow the ADC sample period to increase, which provides additional time for the C_{ADC} capacitor in Figure 34 to charge and higher effective input impedance (Z_S).

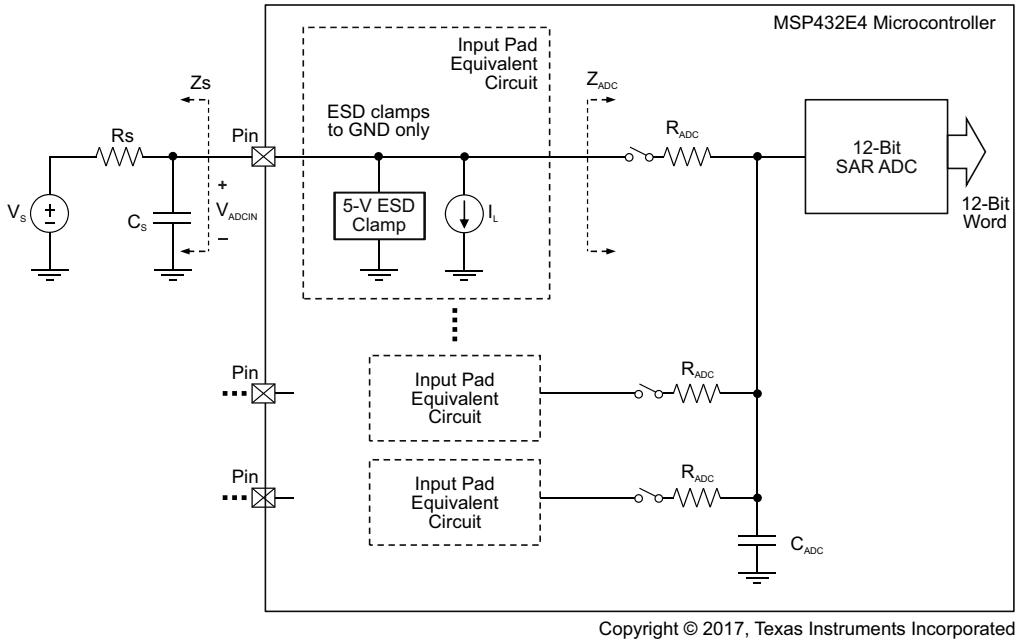


Figure 34. ADC Input Equivalency Diagram

If resistor dividers are used to scale an input voltage, then best results can be achieved with low-value resistors. The resistor from the ADC input to ground should ideally be less than 1 kΩ, but low values increase the power consumption of the system. Avoid values greater than 10 kΩ unless a large filter capacitor is present. If the voltage rail or other input being monitored is powered up when the V_{DD} and V_{DDA} supplies to the MCU are not, take care to not exceed the input injection current specified in the data sheet.

Ceramic filter capacitors of 1 µF or greater can substantially improve noise performance. The trade-off is a reduction in signal bandwidth (as a function of the source impedance) and phase shifting.

Input protection should also be considered, especially when converting signals from external devices or where transient voltages might be present. The ADC pins on some MSP432E4 MCUs (in ADC mode) are not 5-V tolerant but do allow some margin over the 3.0-V span. See the data sheet for specific information.

Increased source impedance can provide a degree of protection to the ADC. Semiconductor clamping circuits can also be used—typically zener diodes or clamping diodes to 3.3 V and GND. When specifying diodes, consider leakage current over temperature (I_R) because this parameter affects overall conversion accuracy.

4.9 Comparators

Three independent integrated analog comparators are available on MSP432E4 MCUs. See the *Analog Comparators* chapter of the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for details.

When selecting comparator pins, the following should be considered:

- C0+ (PC6) can be used as a common reference input to all three comparators.
- C0- (PC7), C1- (PC4) and C2- (PJ5) are the unique negative inputs for each comparator.
- Pins used for comparator inputs must not exceed the maximum injection current if voltage is applied to them prior to the device's V_{DD} supply being powered up.

4.10 Timer and PWM

Several general-purpose timer pins are available on MSP432E4 devices. See the general-purpose timers chapter in the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for details. Each timer module has a CCP0 and a CCP1 pin associated with it. Each timer module can be configured as two independent 16-bit timers or a combined 32-bit timer.

When selecting timer pins, consider the following:

- Timer modules configured for 32-bit mode use the CCP0 pin input. The CCP1 pin input is not used.
- 32-bit modes are one-shot input, periodic input, and RTC input.
- PWM outputs operate in 16-bit mode only and, therefore, CCP0 and CCP1 can be used independently as PWM outputs.

4.11 External Peripheral Interface (EPI)

The MSP432E4 device supports the EPI with a dedicated 8-, 16-, or 32-bit parallel bus. The EPI has a variety of memories and peripherals that can work with the EPI module.

4.11.1 Single SDRAM

In SDRAM mode, the maximum frequency is 60 MHz. Pins used for this mode are EPIOS0 to EPIOS19 and EPI0S28 to EPI0S31 (see the device-specific data sheet for the SDRAM signal functions).

4.11.2 Host Bus Mode

Host bus supports 8- and 16-bit interfaces used in SRAM, PSRAM, and NOR flash memory. EPI0S0 is the LSB of the address and should be connected to A0 of 16-bit memories. The three main strobes are Address Latch Enable (ALE), Write (WRn), and Read (RDn), and the polarity of these pins can be configured in software. Depending on the mode, all of the EPI pins may be used (EPI0S0 to EPI0S35). See the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for more information on how these signals are used in the various modes.

4.11.3 Routing Considerations

In EPI mode, the MSP432E4 device pins are characterized with a 35-pF output capacitance. To maintain timing margins over the full operating speed of the EPI module, EPI signal capacitance, including both load and trace capacitance, must be 35 pF or less, and the GPIO drive strength must be configured for 8 mA. Additionally, when EPI0S31 is used as a high-speed clock pin, it must be configured to 12 mA to maintain timing margins. It is not necessary to include the MSP432E4 device pin and pad characteristics when evaluating total capacitance. Limit total trace length to 6 in (15.24 cm) for full operating speed. Make an effort to keep trace lengths for clock and data similar lengths and give the clock signal 2x width spacing from other signals to avoid crosstalk.

4.12 LCD Controller

Some MSP432E4 MCUs include an LCD controller. This controller works with character-based panels, passive matrix LCD panels, active matrix LCD panels, and OLED panels using either LIDD or Raster mode.

The signal interface to the LCD panel is likely to be an ESD-exposed interface. TI recommends using series resistors on all of the LCD interface signals. The value of the resistor can be 10 Ω to 150 Ω, depending on the system environment and the required speed of the LCD interface.

Configure the LCD outputs for 8-mA drive strength to achieve the timings specified in the device-specific data sheet.

4.12.1 LIDD Mode

The LIDD controller supports the synchronous and asynchronous LCD interface. The pins used in LIDD mode are LCDDATA00 to LCDDATA15, LCDAC, LCDCP, LCDFP, LCDLP, and LCDMCLK. For a detailed explanation, see the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual.

4.12.2 Raster Mode

MSP432E4 MCUs with the LCD peripheral can function in Raster mode with up to a 24-bit bus. Pins used for this mode are LCDDATA00 to LCDDATA23, LCDAC, LCDCP, LCDFP, LCDLP and LCDMCLK. For a detailed explanation, see the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual.

4.13 Quadrature Encoder Interface (QEI)

Some MSP432E4 MCUs support connection to a quadrature encoder that tracks position and direction of rotation and estimates velocity. The frequency of the QEI inputs can be as high as ¼ of the processor frequency. Pins used for the QEI are IDXn, PhAn, and PhBn.

Place a series resistor followed by a capacitor to digital ground on each QEI input to filter the inputs from noise that would violate the input electrical specifications of the MCU. A common value for the series resistor is 100 Ω and for the capacitor is 1 nF. The electrical specifications of the quadrature encoder being attached and the system environment determine the optimum resistor and capacitor values for the system.

Some quadrature encoders may output at 5-V levels, requiring a resistor divider or 5-V tolerant input buffer be placed in series to bring the signal levels down to 3.3 V.

4.14 GPIO

Most pins on an MSP432E4 device can be used as GPIOs. GPIO pins are designated by the letter P followed by the port letter (A to T) and the pin number (0 to 7). GPIO pins can be used for inputs sampled by software, inputs that generate interrupts, outputs that drive logic inputs high or low, or outputs that drive LEDs.

A TI PinMux for MSP432E4 MCUs is available. This utility lets a user graphically configure the device GPIOs and peripherals.

See the *Specifications* chapter of the device-specific data sheet where important operational conditions are detailed.

The following considerations should be taken into account when selecting and designing with pins configured as GPIO inputs:

- Pins are 3.3-V tolerant and are not 5-V tolerant.
- Maximum injection current limits are defined for pins that have their V_{IN} greater than V_{DD} (that is, GPIOs that have power applied before the MSP432E4 MCU is powered).
- GPIO port pins PP0 to PP7 and PQ0 to PQ7 can be configured to use a unique interrupt vector table entry per port pin. Other GPIO ports only have the option of an interrupt vector table entry per port letter requiring the input port value to be read to determine which specific pin on the port generated the interrupt.
- GPIO pins can be configured with an internal pullup or pulldown. See the *Specifications* chapter of the device-specific data sheet for the internal pullup and pulldown values. It may be desirable to use external pullups or pulldowns in situations where a more consistent rise/fall time is required.
- GPIO port pins PK4 to PK7 can be configured to cause a wake from hibernate mode.
- GPIO port pins PM4 to PM7 can be configured as tamper input detects.

The following considerations should be taken into account when selecting and designing with pins configured as GPIO outputs:

- Pins PM4 to PM7 and PJ1 have 2-mA maximum output capability when configured as outputs.

- Pins PL6 and PL7 have a fixed 4-mA output drive strength and cannot operate in open-drain mode. On devices that support USB, these pins function as USB0DP and USB0DM.
- At system power-on reset, pins power up as GPIO inputs with no pullup or pulldown configured. Pins used as outputs that are required to be at a high or low value at system power up should be externally pulled up or down. The exception to this statement is JTAG pins which power-on with internal pullups enabled and configures for JTAG.
- A total of four GPIO pins may be used simultaneously to each sink 18 mA, but the V_{OL} is specified as 1.2 V when operating in this manner. There should be a maximum of two high-current pins per physical die side (defined in the *Specifications* chapter of the device-specific data sheet).

4.15 Hibernate Signals

Some of the MSP432E4 MCUs contain a Hibernation module that can be used to put the device in its lowest-power mode. See the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for a detailed description of the Hibernation module.

The V_{BAT} pin can be used to power the Hibernation module. See Section 3.4.6 for system considerations related to V_{BAT}.

The Hibernation module can be clocked by a 32768-kHz external clock source or, if the real-time clock is not used, by the internal Hibernation Low-Frequency Oscillator (HIBLFIOSC). See Section 3.6.1.2 for system level considerations of this clock source.

The $\overline{\text{WAKE}}$ pin on the MSP432E4 device is used to wake the device from hibernation mode. This pin can also be used to generate an interrupt when in run mode, sleep mode, or deep sleep mode. This pin can be connected to a switch to ground and pulled up externally with a 1-MΩ resistor connected to the same supply voltage that the V_{BAT} pin is connected to.

If the $\overline{\text{WAKE}}$ pin is not used, connect it to system ground.

The $\overline{\text{HIB}}$ pin on the MSP432E4 device can be used to control the regulator supplying V_{DD}. See the MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual for details on the Hibernate functionality.

If the $\overline{\text{HIB}}$ pin is not used, it can be left unconnected.

Some additional hibernate features can be used when VDD3ON hibernation mode is used:

- Four GPIOs can be configured as external wake sources.
- Four GPIOs can be configured as tamper detect inputs.
- The hibernation clock source can be output on a GPIO configured for the RTCCLK function.

See the device-specific data sheet for specific details of these functions.

5 System Design Examples

Table 11 lists example designs using the MSP432E4 microcontrollers.

Table 11. MSP432E4 Example Designs

Part Number	Description	Device	Device Package	Key Features	PCB Layer Count
MSP-EXP432E401Y	SimpleLink MSP432E401Y LaunchPad™ development kit	MSP432E401YTPDT	128-pin TQFP	USB, Ethernet, Headers	4

6 Conclusion

Applying good system design practices from the earliest design stages ensures a successful board bring-up. The design process should include thorough design reviews using the information in this application report, other embedded system design resources, and reports created by the design team. These efforts will be rewarded with a reliable and properly performing MSP432E4 microcontroller-based design.

The use of the SimpleLink MSP432E4 SDK also minimizes software changes to the start-up routines that configure the I/Os, enabling application code to be moved to the new devices with minimal functional changes.

7 References

The following related documents and software are available on the TI MSP432™ website:

1. MSP432E411Y SimpleLink™ Ethernet Mixed-Signal Microcontroller
2. MSP432E401Y SimpleLink™ Ethernet Mixed-Signal Microcontroller
3. MSP432E4 SimpleLink™ Microcontrollers Technical Reference Manual
4. SimpleLink™ MSP432E4 Software Development Kit (SDK)
5. MSP430™ System-Level ESD Considerations

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