Application Report
SLAA758–November 2017

An Efficient LDO-less Power Supply Solution for AFE76xx

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ABSTRACT

This application report provides a more efficient power supply solution to power up the RF-sampling analog front-end AFE76xx from Texas Instruments. The device uses DC-DC converters to replace LDOs on the original EVM, which improves system efficiency without sacrificing performance. The new power solution is described with some filter techniques, to suppress noise caused by DC-DC converters. This report illustrates the performance and improved efficiency of the new solution.

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1 System Overview

1.1 AFE76xx: Quad-Channel RF Sampling Analog Front End

The AFE76xx is a family of high performance, quad channel, 14-bit, integrated RF sampling analog front ends (AFEs), with 9-GSPS digital-to-analog converters (DACs) and 3-GSPS analog-to-digital converters (ADCs), capable of synthesizing and digitizing wideband signals. The high dynamic range of the device is suitable for 3G/4G signals for wireless base stations. An integrated, low-jitter, phase-locked loop/voltage-controlled oscillator (PLL/VCO) provides the high frequency sampling clock synchronized to a lower frequency reference clock. Figure 1 shows the functional block diagram of the AFE76xx.

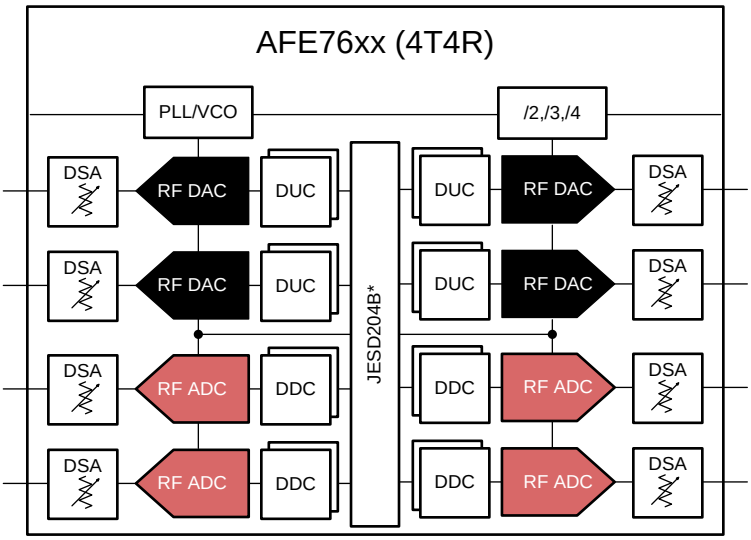

Figure 1. Functional Block Diagram of AFE76XX

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1.2 Power Supply Solution of AFE76xx

The power rails of the AFE76xx are divided into several blocks according to the subsystem which they supply.To achieve optimal performance, the AFE76xx evaluation module (EVM) uses low dropout voltage regulators (LDOs) to power up almost all the power rails, as shown in Figure 2. In addition, each net generally follows this convention:

- Each power net includes a ferrite bead (FB) to isolate from other power nets.
- Each power net includes a group of bypass caps close to the AFE76xx supply pin.
- Each power net includes a group of bypass caps close to the DC-DC converter.

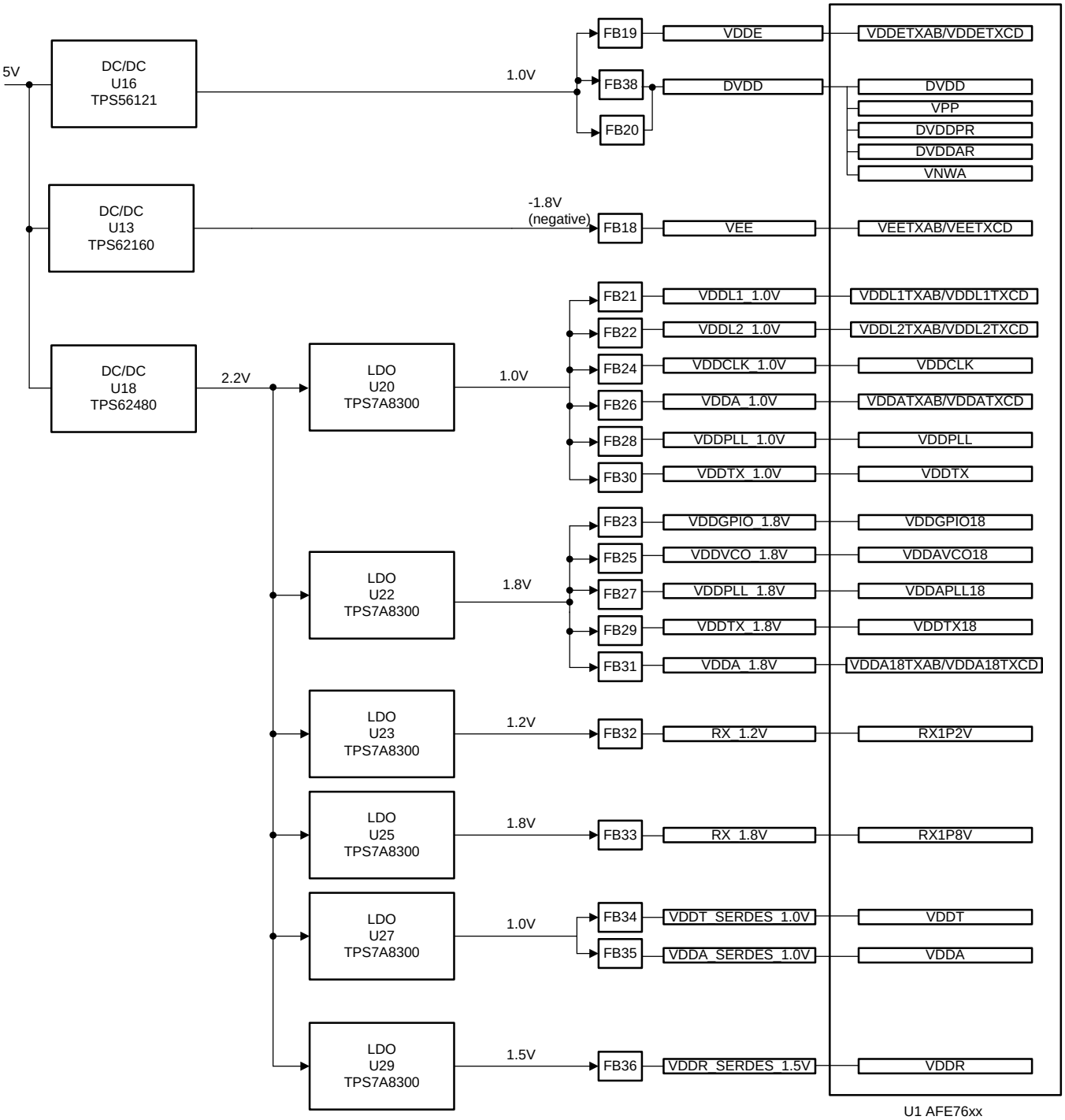

Figure 2. Default Power Tree of AFE76xx EVM

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LDOs have low noise and no switching frequency spurs, which is critical to the performance of an RF sampling system; however, LDOs have lower efficiency due to the internal regulation transistor. The heat dissipation problem caused by low efficiency creates a big challenge to prevent the PCB from overheating.

This application report introduces a more efficient power supply solution to power up the AFE76xx. The device uses DC-DC converters to replace LDOs, which improves power efficiency of the system without sacrificing performance.

1.3 Key System Specifications

Power supply degradation manifests in two areas: spurious output and phase noise. The switching spurs in the DC-DC converters can couple onto analog outputs and result in degraded spurious performance. Noisy converters infect the internal oscillator (PLL/VCO) performance and yield degraded phase noise performance. These are the key specifications used to confirm the power solution is properly working.

PARAMETER	SPECIFICATION
TX Spurious Output	-80 dBc or better
TX RMS Jitter	305 fsec

2 Test Results

2.1 Hardware Platform

The hardware platform for demonstrating the performance with minimum rails uses the TSW4086 combined with the TSW2086 daughter board. The TSW4086 utilizes the AFE768x in a 2T/2R/1F configuration. The TSW2086 is the power supply board that provides the supply rails to the TSW4086. The daughter board mechanics allows future expansion of the power supply solution to power 2 or more TSW4086 analog boards. Figure 5 is a new power supply solution with DC-DC converters used on the TSW2086 reference design. The solution reduced the overall power solution IC count from 9 devices to 5.

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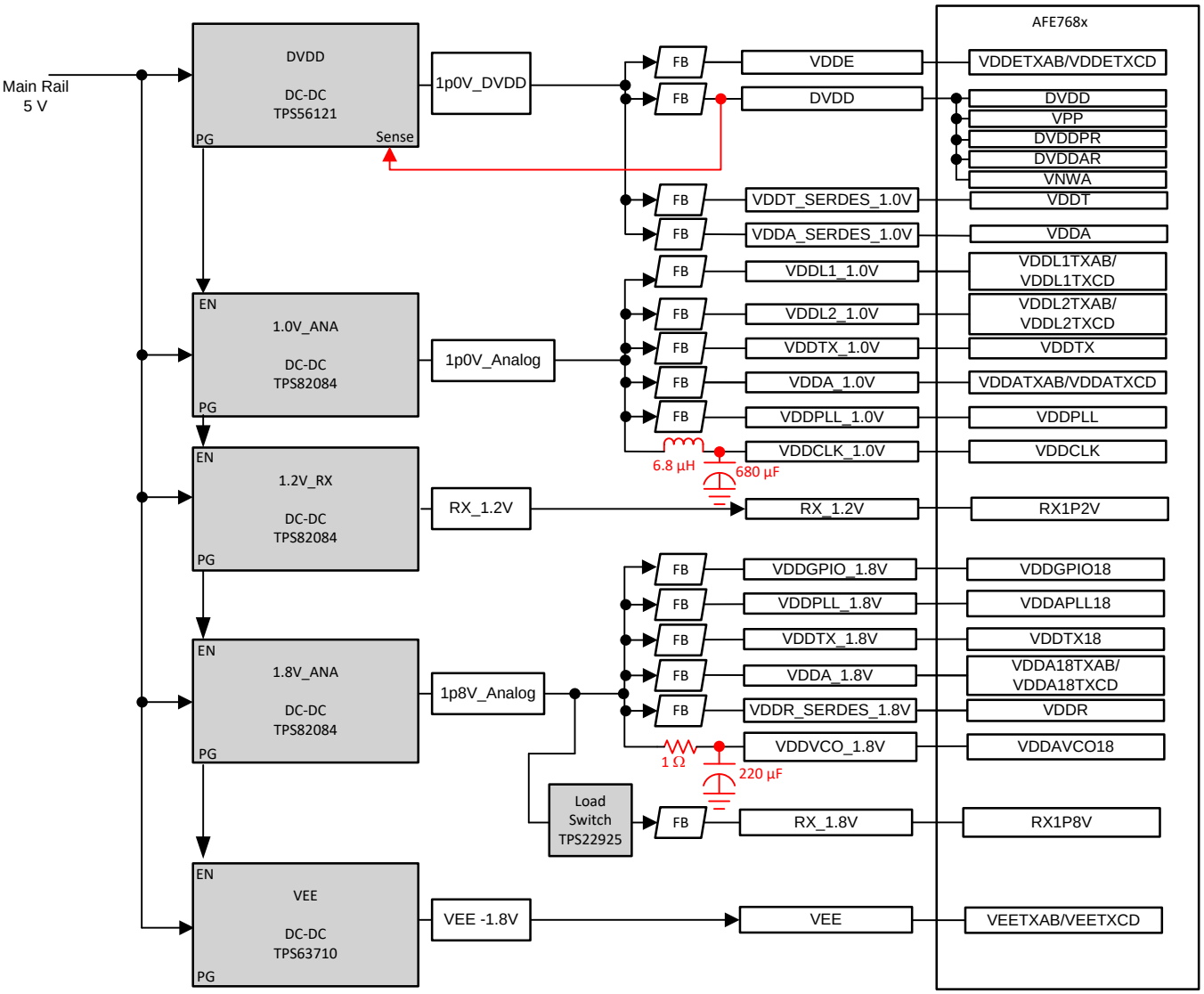

Figure 3. TSW2086 DC-DC Power Supply Solution Block Diagram

2.2 Supply Filtering and Isolation

The individual nets are are filtered and isolated using ferrite beads. In particular, the ferrite bead / EMI filter device NFM31PC276B0J3L from Murata is particularly useful as it has a filter notch at around 2 MHz where the switching frequencies reside.

2.3 PLL/VCO Filtering

The power nets for the PLL (Phased Lock Loop) and the VCO (Voltage Controlled Oscillator) are particularly sensitive to noise and spurs. Since the PLL/VCO supplies the clock to the data converters, any degradation seeping into those circuits is directly channeled to the analog outputs. Empirical measurements show that there are two sensitive nets that require additional filtering: VDDCLK (1.0V) and VDDVCO (1.8V).

The VDDVCO (1.8V) does not draw much current. For this net, an RC filter is acceptable. An RC filter with series 1-ohm and shunt 220-uF yields a corner frequency about 720-Hz and minimally drops the voltage by about 20-mV which is well within the compliance range. This filter is sufficient to reject DC-DC noise from infecting phase noise performance of the VCO.

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The VDDCLK (1.0V) draws higher current (~500-mA) and thus requires an LC filter. An LC filter with series 6.8-uH inductance with a shunt 680-uF capacitor yields a corner frequency around 2.3-kHz. This filter is sufficient for squelching noise on this net from infecting the VCO. The DC resistance (DCR) of the inductor, Coilcraft 1812PS-682KLB for example, is 0.13-Ω which generates 58-mV voltage drop. This voltage drop almost takes up half of the voltage margin of this power rail so it must be considered carefully.

2.4 Layout Considerations

Spurious performance is dependent on the layout structure. The DC-DC converters are generally switching from 500-kHz to 2-MHz. The switching spurs are generally very large. Switching spurs infiltrate unwanted circuits via conducted path or radiated path. Conducted spurs are mitigated with the aforementioned ferrite bead isolation, supply filtering, and adequate low frequency bypass capacitors. Radiated emissions are more difficult to control.

The primary location for radiated emissions is right at the DC-DC converter itself and the switching inductor. Modules that place the switching inductor on top of the DC-DC converter IC confine the radiated emissions to the surface area of the chip. The emissions radiate perpendicular to the device. In other words, with the IC laying flat on the PC board, the radiated emissions shoot upwards and downwards through the board itself.

Since the switching spurs are large in amplitude and at low frequency, localized shielding or PCB ground planes do little to attenuate the spurs. Indeed, switching spurs penetrate ground planes easily and infect internal, sensitive power traces. As such, it is imperative that the layout keep sensitive routing from running on an internal layer directly underneath the DC-DC converter. Further, no other board with sensitive internal nets should be placed directly above or below. Even physical spacing as much as 1 inch is not sufficient to reduce the spurious coupling. Instead, the DC-DC switchers should be offset from any sensitive area or other boards so that there is nothing directly above or below the converters that will be contaminated by switching spurs.

3 Testing Results

3.1 Spurious Outputs

The spurious output performance comparing the standard EVM to the TSW2086 power supply board is shown in Figure 4. Small switching supply spurs are observed, but are lower than the 80 dBc specification.

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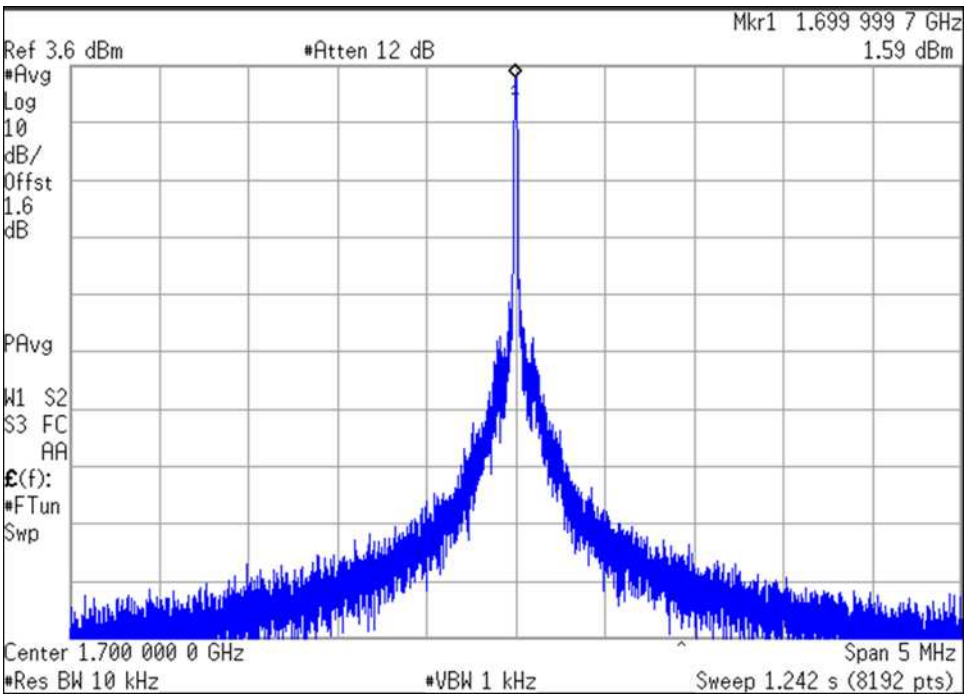

Figure 4. TX Output Spectrum with TSW2086 Power Solution

3.2 Phase Noise

The phase noise performance is shown for a couple of cases to illustrate the sensitive nets. Figure 5 shows the performance of the standard EVM compared with the TSW2086, unfiltered and with VDDVCO RC filtered. Without the filtering, there is a noise hump around 20 kHz. Introducing the filtering gets the phase noise back to its original form.

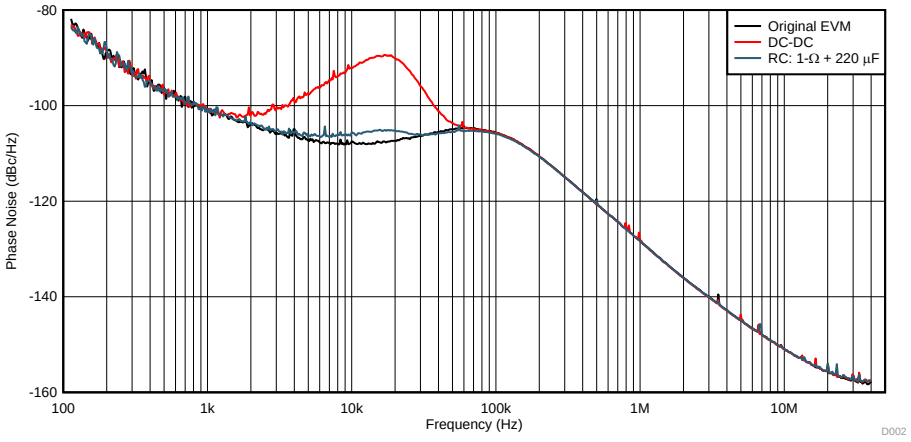

Figure 5. VDDVCO Power Net Supply Comparison

Figure 6 shows the performance of the standard EVM and the TSW2086 with and without VDDCLK LC filtered. Without the filtering, the phase noise degrades with a noise hump peaking around 10 kHz. With the LC filter, the phase noise recovers to the standard EVM's value.

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3.3 Efficiency Comparison

The standard mode with the DAC sampling at 5898.24-MSPS and the ADC sampling at 2949.12-MSPS on the original EVM consumes a total power of 21.3 W. This value includes the power consumed by the AFE76xx, LMK04828, and the power loss of the power supply solution and cooling fan. The total power consumed by the EVM with a DC-DC power solution is only 16.9 W. The DC-DC solution saves 4.3 W of power for the system which significantly improves system efficiency.

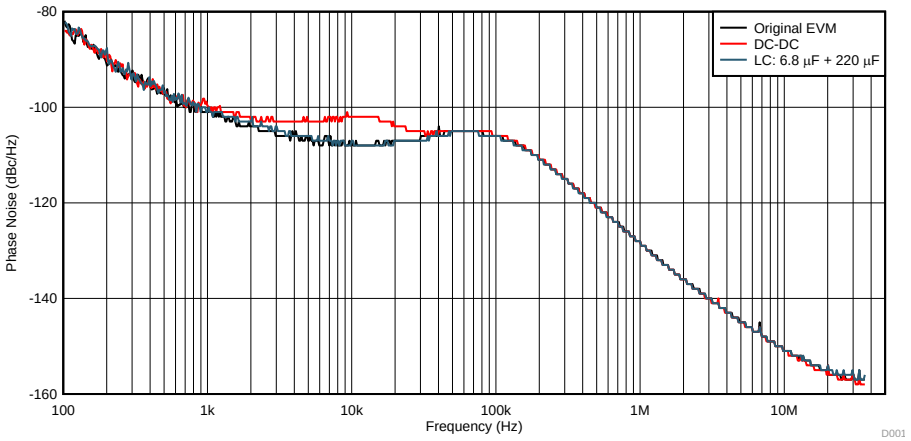

Figure 6. VDDCLK Power Net Supply Comparison

4 Conclusion

The measured results support the following conclusions:

- With two exceptions, the power supply rails operate with DC-DC converters directlywithout sacrificing performance.
- VDDAVCO18 and VDDCLK are the most sensitive power nets. With an RC filter and an LC filter added on these two nets, the DAC core and PLL power rails operate with DC-DC converters without sacrificing performance.
- The DC-DC converter solution saves approximately 4 W of total power compared to the LDO solution.
- The DC-DC converter solution reduces the number of power devices from 9 to 5, and reduces the distinct part numbers of the power devices from 4 to 3.
- A similar configuration with the current capability of the DC-DC converters scaled up appropriately is possible to power two, three, or four AFE76xx devices.

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