Application Report
SLAA288A–June 2006–Revised August 2018

MSP430FW42x Scan Interface SIFCLK Adjustment

MSP430 Applications

ABSTRACT

The scan interface has an integrated RC oscillator that can be used for the timing state machine. Because of frequency drift caused by temperature and voltage changes, the clock signal may change. An integrated hardware counter allows measurement of the SIFOSC clock signal based on a reference clock. This application report describes how to measure and adjust the SIFCLK.

Related source code is available from www.ti.com/lit/zip/slaa288.

Contents

Trademarks

1 Introduction

The timing state machine (TSM) of the MSP430FW42x scan interface supports different clock sources. The ACLK is used as the clock source for defining the sample rate. For single-measurement steps, the ACLK clock source, SMCLK clock signal from the MSP430™ clock module, or TSM internal oscillator (SIFOSC) can be chosen as the clock source.

An accurate clock source is needed to optimize the current consumption of the system. Note that a certain time is needed to settle the comparator and DAC of the scan interface analog front end. In the data sheet, the worst-case times are given. For optimized current consumption, the minimum wait time should be used. Moreover, the excitation pulse in an LC-sensor solution should be short to reduce the current consumption. Accurate adjustment of single-measurement steps requires a stable clock source signal.

2 Timing State Machine Oscillator

The internal clock generator, SIFOSC, makes the scan interface independent from SMCLK. The frequency of the SIFOSC varies between individual devices, with temperature, and with supply voltage. The SIFFNOM control bit defines the nominal frequency for 1 MHz or 4 MHz. Four control bits (SIFCLKFQx bits) in the SIFCTL5 control register can adjust the frequency close to the nominal frequency of 1 MHz or 4 MHz.

A software routine can measure and calibrate the SIFOSC frequency. An 8-bit counter that is used for the measurement is implemented within the SIFOSC oscillator. Setting the control bits SIFCLKEN and SIFCLKGON resets the SIFCNT3 counter. Beginning with the next rising edge of ACLK, the SIFOSC clock cycles are counted. Reading SIFCNT3 while counting always results in reading a 0x01. Depending on the SIFFNOM setting, the cycles during either 1 (SIFFNOM = 0) or 4 (SIFFNOM = 1) ACLK periods are counted. This results in similar counts independent of the SIFFNOM setting. The *Scan IF* chapter of the MSP430x4xx Family User's Guide shows a simplified block diagram for the SIFOSC oscillator. Figure 1 shows a more detailed diagram.

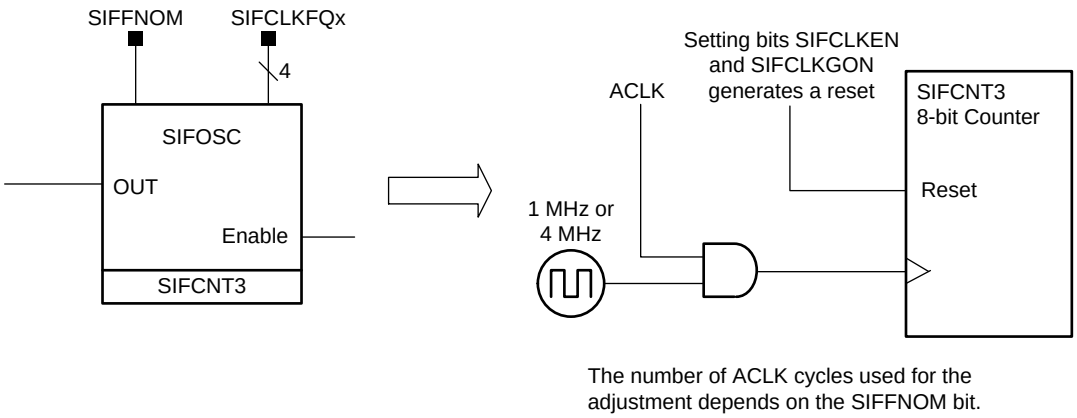

Figure 1. Scan Interface Timing State Machine Oscillator (SIFOSC)

The calibration routine can be removed for the final product. However, such a software routine can be kept and periodically activated during the entire product lifetime. The period of running the calibration cycle must be defined by the application requirement (for example, the frequency accuracy that is required versus temperature and supply voltage).

3 Calibration Routine

The calibration routine includes the measurement of the SIFOSC frequency and the adjustment of SIFOSC.

Figure 2 shows how to do the measurement. The Measure_SIFOSC function returns the measurement result.

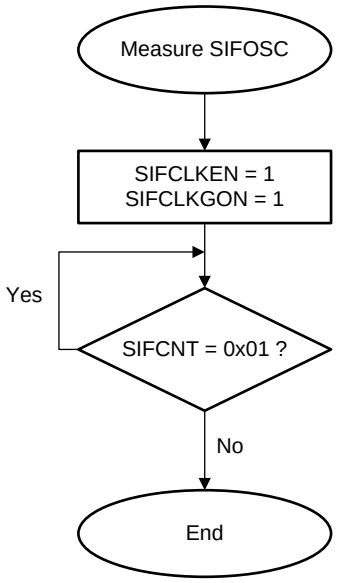

Figure 2. Algorithm to Measure Scan Interface Internal Oscillator

Based on this measurement algorithm, the SIFOSC oscillator can be tuned to a target frequency. Usually, the targeted frequency is 1 MHz or 4 MHz, depending on the SIFFNOM bit setting.

Figure 3 shows a possible algorithm to calibrate the scan interface oscillator, SIFOSC. The algorithm makes sures that the adjusted frequency of the oscillator is below the targeted frequency. This means that scan interface timings based on this clock have at least the duration of the target frequency, but never less than that.

The number of ACLK cycles used for the counting depends on the SIFFNOM setting. If 4 MHz is selected (SIFFNOM = 0), four ACLK cycles are used for the measurement. For a 1-MHz selection (SIFFNOM = 1), only one ACLK cycle is used for SIFOSC measurement. This makes sure that the same number of counts for the 1-MHz and 4-MHz setting are used during the measurement. For these target frequencies, the SIFCNT3 counter should reach 128 (Target in Figure 3 = 128).

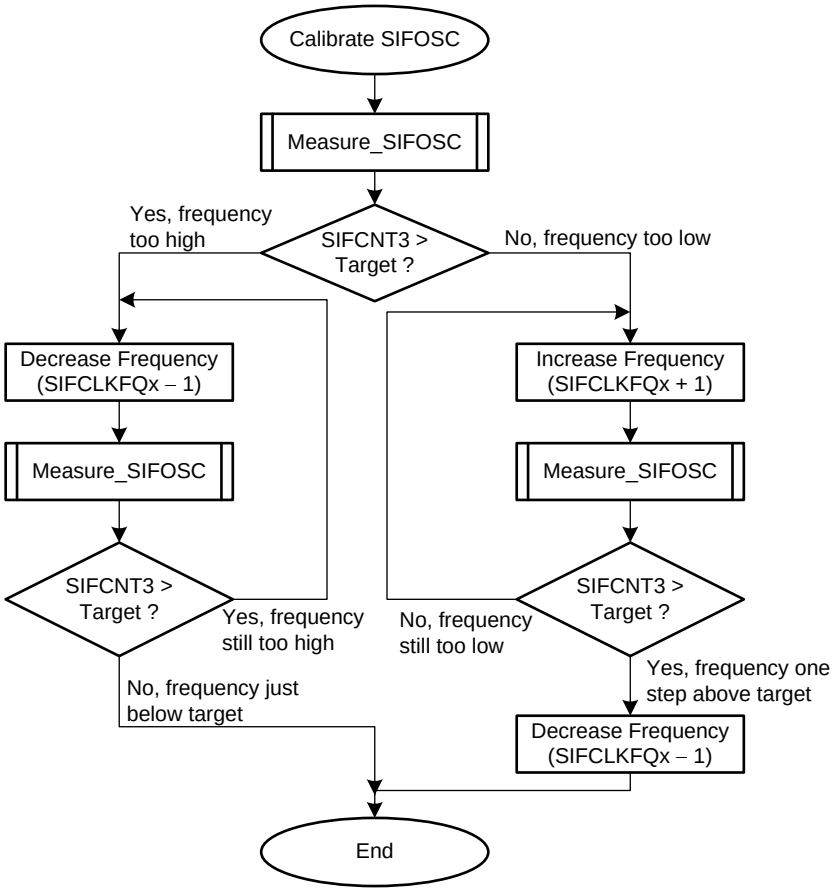

Figure 3. Algorithm to Calibrate Scan Interface Oscillator SIFOSC

4 Measurements

Figure 4 shows the measurement of the SIFOSC adjustment. At the beginning, the SIFCLKFQx bits were set to 0x00. This means that the lowest frequency for SIFOSC is selected. Then, the Calibrate_SIFOSC function is called. As soon as the SIFCLKFQx bits were changed, the output frequency of the SIFOSC oscillator was measured.

The red arrows in Figure 4 show the SIFOSC frequency that was adjusted after finishing the Calibrate_SIFOSC function.

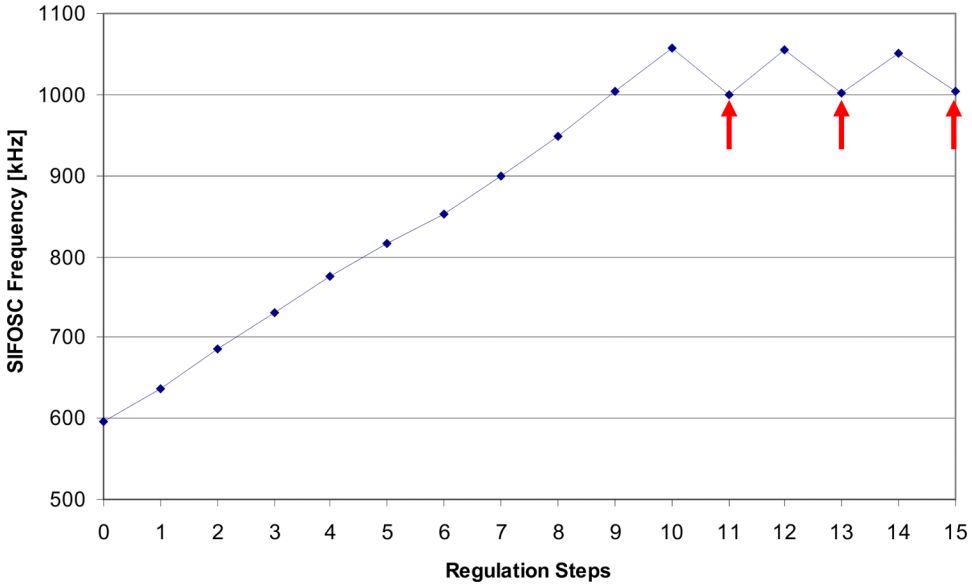

Figure 4. Measurement of SIFOSC Adjustment

5 References

1. MSP430x4xx Family User's Guide
2. MSP430FW42x Mixed-Signal Microcontrollers data sheet

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 30, 2006 to August 2, 2018	Page
• Editorial and formatting changes throughout document	1

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