Functional Safety Information

TPSI31P1-Q1
Functional Safety FIT Rate, FMD, and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPSI31P1-Q1 (SSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

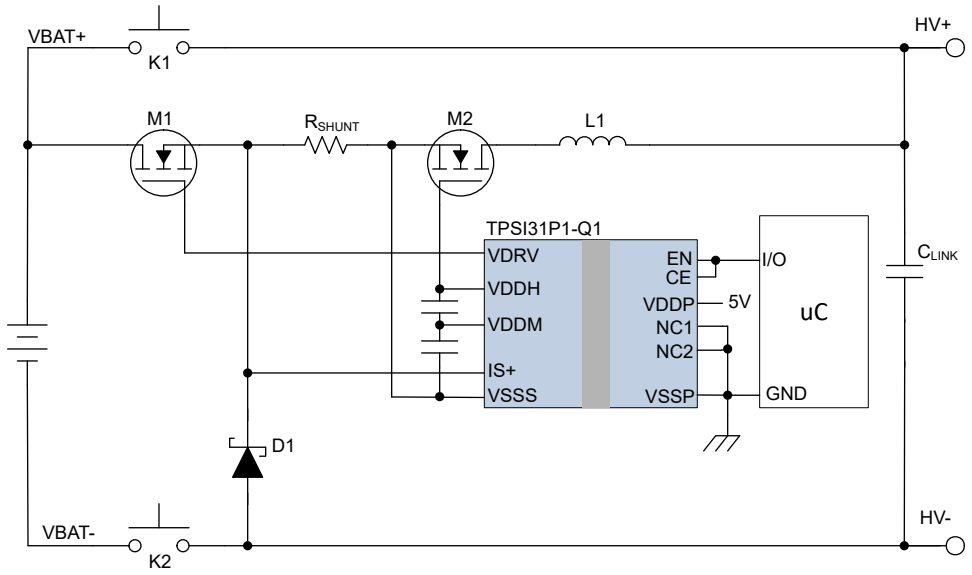

Figure 1-1. Functional Block Diagram

The TPSI31P1-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPSI31P1-Q1 device based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	19
Die FIT rate	3
Package FIT rate	16

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 250mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog and Mixed = < 50V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution for the TPSI31P1-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VDDH | VDDM rails fail to power up. VDRV remains low.	25
VDRV does not respond to EN signaling.	15
Output power not meeting specification. Longer VDDH | VDDM start-up and recovery times.	25
VDDH is not regulated, potential device damage.	15
VDRV propagation times are longer than specified.	5
Higher EMI.	5
Unpredictable power-down sequence.	5
VDRV output is held high.	5

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPSI31P1-Q1 device. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to VSSP or VSSS (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDDP (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPSI31P1-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the data sheet.

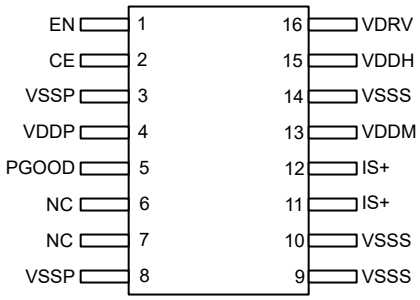

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device operated in standalone during normal operation, prior to any open or short condition being applied to the respective pin
- EN set to a static logic low or high (VDRV asserted low or high respectively)
- CE set to a static logic low or high.
- Opens or shorts occur relative to primary and secondary sides of the device and is a static event

Table 4-2. Pin FMA for Device Pins Short-Circuited to VSSP or VSSS

Pin Name	Pin No.	Ground	Description of Potential Failure Effects	Failure Effect Class
EN	1	VSSP	VDRV asserted low.	B
CE	2	VSSP	Device in standby. No power transfer. VDDH and VDDM rails discharge. VDRV is asserted low with keep-off circuitry enabled.	B
VDDP	4	VSSP	No power transfer. VDDH and VDDM rails collapse. VDRV is asserted low with keep-off circuitry enabled.	B
PGOOD	5	VSSP	PGOOD is asserted low. If PGOOD is not used, tie to VSSP.	B
NC	6	VSSP	No effect.	D
NC	7	VSSP	No effect.	D
IS+	11	VSSS	If CE = H and EN = H, VDRV is asserted high.	B
IS+	12	VSSS	If CE = H and EN = H, VDRV is asserted high.	B
VDDM	13	VSSS	VDDH and VDDM rails collapse. VDRV is asserted low with keep-off circuitry enabled.	B
VDDH	15	VSSS	VDDH and VDDM rails collapse. VDRV is asserted low with keep-off circuitry enabled.	B
VDRV	16	VSSS	If VDRV was high, VDDH and VDDM rails collapse. VDRV asserts low with keep-off circuitry enabled. If VDRV was low, no effect.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	VDRV asserted low. EN pin has an internal resistive pull-down to VSSP.	B
CE	2	Device powers off. VDDH and VDDM rails discharge. VDRV is asserted low with keep-off circuitry enabled. CE pin has an internal resistive pull-down to VSSP.	B
VSSP	3	Device has additional ground path through pin 8 (VSSP).	C
VDDP	4	No power transfer. VDDH and VDDM rails collapse. VDRV asserted low with active clamp enabled.	B
PGOOD	5	If PGOOD is unused, no effect. If PGOOD is used, and an external pull-up resistor is present, PGOOD asserted high is indicated to the system, regardless of actual status.	B
NC	6	No effect.	B
NC	7	No effect.	B
VSSP	8	Device has additional ground path through pin 3 (VSSP).	C
VSSS	9	Device has ground path through pin 14 (VSSS). Normal power transfer. VDDH and VDDM rails remain charged. VDRV follows state of EN logic level.	C
VSSS	10	Device has ground path through pins 9 and 14 (VSSS). Normal power transfer. VDDH and VDDM rails remain charged. VDRV follows state of EN logic level.	B
IS+	11	IS+ pin has a weak internal resistive pull-down to VSSS and can be susceptible to switching noise. VDRV asserts high.	B
IS+	12	IS+ pin has a weak internal resistive pull-down to VSSS and can be susceptible to switching noise. VDRV asserts high.	B
VDDM	13	VDDH and VDDM can collapse under loading or switching events.	B
VSSS	14	Device has ground path through pin 9 (VSSS). Normal power transfer. VDDH and VDDM rails remain charged. VDRV follows state of EN logic level.	C
VDDH	15	VDDH can collapse under loading or switching events.	B
VDRV	16	No drive to external switch. External switch gate control can float depending upon application circuitry.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VDRV	16	VDDH	If VDRV was low, VDDH and VDDM rails collapse. VDRV remains low with active clamp enabled. If VDRV was high, no effect.	B
IS+	12	VDDM	IS+ comparator threshold can be reached causing VDRV to be asserted low.	B
IS+	12	IS+	Normal operation.	D
EN	1	CE	EN can be tied to CE in the application, if desired.	D
PGOOD	5	NC	NC output pin can drive low causing an electrical ORing of PGOOD with an open-drain output. PGOOD can be asserted low.	B
NC	6	NC	No effect.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDDP

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	EN can be tied to VDDP in the application, if desired.	D
CE	2	CE can be tied to VDDP in the application, if desired. Device powers up depending on voltage level of VDDP.	D
PGOOD	5	Potential high current from VDDP while PGOOD is asserted low. Device can thermal cycle or be damaged.	A
NC	6	Potential high current from VDDP while NC open drain is asserted low. Device can thermal cycle or be damaged.	A
NC	7	Potential high current from VDDP while NC open drain is asserted low. Device can thermal cycle or be damaged.	A

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