Functional Safety Information

LM5001-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the LM5001-Q1 (SOIC-8 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

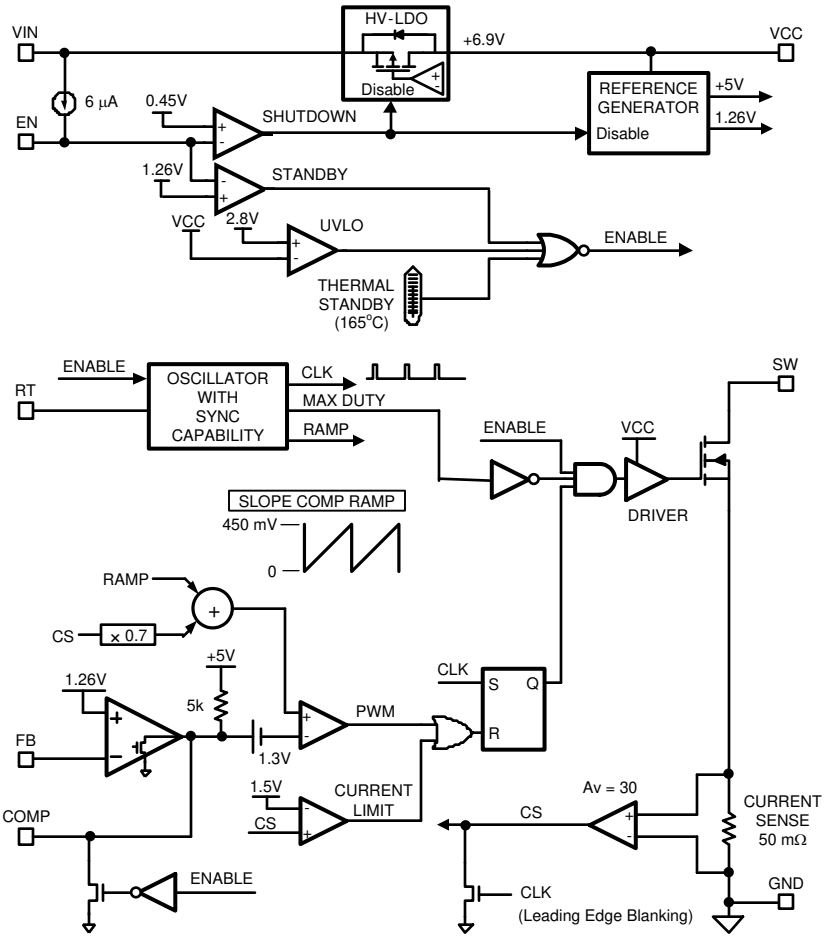

Figure 1-1. Functional Block Diagram

The LM5001-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM5001-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	25
Die FIT rate	20
Package FIT rate	5

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Switched Regulators DC-DC, Buck, Boost	20	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM5001-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	40
SW output not in specification - voltage or timing	45
SW low-side power FET stuck on	5
V_{OUT} voltage not in specification	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5001-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM5001-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5001-Q1 data sheet.

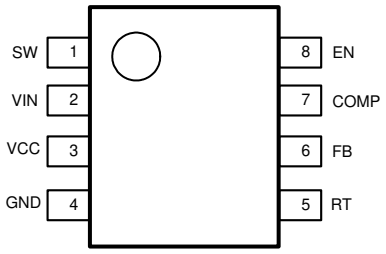

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used withing the *Recommended Operating Conditions* and *Absolute Maximum Ratings* found in the LM5001-Q1 data sheet
- For the analysis, the boost typical application as shown in the LM5001-Q1 data sheet in the *Typical Application* section is used
- V_{IN} = 12 V
- V_{OUT} = 48 V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	No switching. Input voltage is shorted to ground	B
VIN	2	No switching. No input voltage	B
VCC	3	No switching. No VCC voltage	B
GND	4	Normal configuration	D
RT	5	Oscillator runs at maximum frequency. Possible unstable output voltage	C
FB	6	Open loop operation, which can result in excessive output voltage, and in turn, can cause damage to both the IC and external circuit.	A
COMP	7	No switching	B
EN	8	No switching. Device is disabled.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	No switching. Output voltage not regulated	B
VIN	2	No switching. No input voltage	B
VCC	3	No stable VCC to sustain normal operation	B
GND	4	Possible device damage	A
RT	5	Minimum oscillator frequency is set.	C
FB	6	Open loop operation, which can result in excessive output voltage, and in turn, can cause damage to both the IC and external circuit.	A
COMP	7	Lack of proper loop compensation for stable operation	B
EN	8	Pin can be left floating and start-up	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	VIN	Internal switch shorted to VIN, device damage is likely	A
VIN	2	VCC	Damage to VCC if VIN voltage is greater then 14 V	A
VCC	3	GND	No switching. No VCC voltage	B
RT	5	FB	Switching frequency not stable	C
FB	6	COMP	Lack of proper loop compensation for stable operation.	B
COMP	7	EN	Damage to COMP if EN voltage is greater than 7 V	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1	Internal switch shorted to supply, device damage is likely	A
VIN	2	Normal operation	D
VCC	3	Internal LDO is by passed. Internal rails supplied with VIN.	D
GND	4	Possible damage to the device	A
RT	5	Exceeds RT absolute maximum voltage rating of 7 V	A
FB	6	Exceeds FB absolute maximum voltage rating of 7 V	A
COMP	7	Exceeds COMP absolute maximum voltage rating of 7 V	A
EN	8	Normal operation	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265