Functional Safety Information

TPS7B81-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the TPS7B81-Q1 (HVSSOP, WSON, and TO-252 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

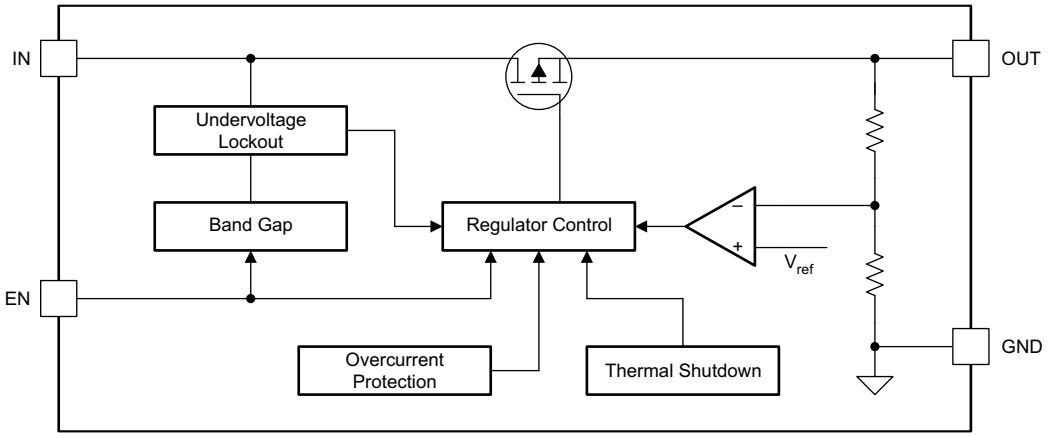

Figure 1-1. Functional Block Diagram

The TPS7B81-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 HVSSOP Package

This section provides functional safety failure in time (FIT) rates for the HVSSOP package of the TPS7B81-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	5
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 300 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 WSON Package

This section provides functional safety failure in time (FIT) rates for the WSON package of the TPS7B81-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	6
Package FIT rate	2

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 300 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 TO-252 Package

This section provides functional safety failure in time (FIT) rates for the TO-252 package of the TPS7B81-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	4
Package FIT rate	12

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 300 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator ≤ 1 Watt – (LDO)	40 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B81-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output	45
Output high (following input)	15
Output not in specification	35
Short circuit on any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B81-Q1 (HVSSOP, WSON, and TO-252 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 HVSSOP Package

Figure 4-1 shows the TPS7B81-Q1 pin diagram for the HVSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B81-Q1 data sheet.

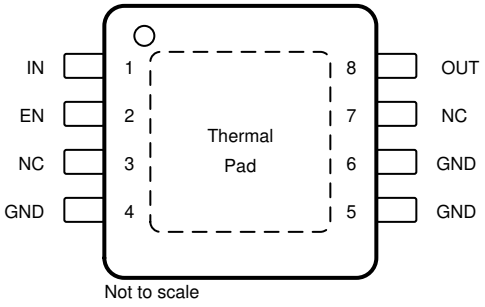

Figure 4-1. Pin Diagram (HVSSOP Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
EN	2	The device is stuck in shutdown mode, resulting in no output voltage.	B
NC	3	No effect. Normal operation.	D
GND	4	No effect. Normal operation.	D
GND	5	No effect. Normal operation.	D
GND	6	No effect. Normal operation.	D
NC	7	No effect. Normal operation.	D
VOUT	8	The device is not operational when the output is pulled to GND. Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
EN	2	The device flips between shutdown mode and normal mode because of the noise on the EN voltage. This condition can result in no output voltage.	B
NC	3	No effect. Normal operation.	D
GND	4	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B
GND	5	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B
GND	6	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B
NC	7	No effect. Normal operation.	D
VOUT	8	The output is disconnected from the load.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	EN (pin 2)	EN is pulled to the IN supply. Shutdown mode is not possible. The device is powered on as long as the input supply is present.	D
EN	2	NC (pin 3)	No effect. Normal operation.	D
NC	3	GND (pin 4)	No effect. Normal operation.	D
GND	5	GND (pin 6)	No effect. Normal operation.	D
GND	6	NC (pin 7)	No effect. Normal operation.	D
NC	7	VOUT (pin 8)	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
EN	2	EN is pulled to VBAT. Shutdown mode is not possible. The device is powered on as long as VBAT is present.	C
NC	3	No effect. Normal operation.	D
GND	4	VBAT can discharge if other GND connections on the device are still tied to GND. If all pins are floated to VBAT, this condition can result in VOUT detecting the VBAT voltage.	B
GND	5	VBAT can discharge if other GND connections on the device are still tied to GND. If all pins are floated to VBAT, this condition can result in VOUT detecting the VBAT voltage.	B
GND	6	VBAT can discharge if other GND connections on device are still tied to GND. If all pins are floated to VBAT, this condition can result in VOUT detecting the VBAT voltage.	B
NC	7	No effect. Normal operation.	D
VOUT	8	The VOUT pin can be damaged and the load being powered by the TPS7B81-Q1 instead uses the VBAT voltage.	A

4.2 WSON Package

Figure 4-2 shows the TPS7B81-Q1 pin diagram for the WSON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B81-Q1 data sheet.

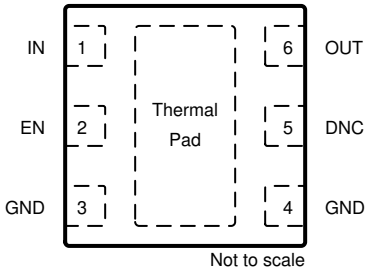

Figure 4-2. Pin Diagram (WSON Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
EN	2	The device is stuck in shutdown mode, resulting in no output voltage.	B
GND	3	No effect. Normal operation.	D
GND	4	No effect. Normal operation.	D
DNC	5	No effect. Normal operation.	D
VOUT	6	The device is not operational when the output is pulled to GND. Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
EN	2	The device flips between shutdown mode and normal mode because of the noise on the EN voltage. This condition can result in no output voltage.	B
GND	3	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B
GND	4	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B
DNC	5	No effect. Normal operation.	D
VOUT	6	The output of the device is disconnected from the load.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	EN (pin 2)	EN is pulled to the IN supply. Shutdown mode is not possible. The device is powered on as long as the input supply is present.	D
EN	2	GND (pin 3)	The device is stuck in shutdown mode, resulting in no output voltage.	B
GND	4	DNC (pin 5)	No effect. Normal operation.	D
DNC	5	VOUT (pin 6)	VOUT can fall out of regulation or increased quiescent current can be observed.	C

Table 4-9. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
EN	2	EN is pulled to VBAT. Shutdown mode is not possible. The device is powered on as long as VBAT is present.	C
GND	3	VBAT can discharge if other GND connections on the device are still tied to GND. If all pins are floated to VBAT, this condition can result in VOUT detecting the VBAT voltage.	B
GND	4	VBAT can discharge if other GND connections on the device are still tied to GND. If all pins are floated to VBAT, this condition can result in VOUT detecting the VBAT voltage.	B
DNC	5	VOUT can fall out of regulation or increased quiescent current can be observed.	C
VOUT	6	The VOUT pin can be damaged and the load being powered by the TPS7B81-Q1 instead uses the VBAT voltage.	A

4.3 TO-252 Package

Figure 4-1 shows the TPS7B81-Q1 pin diagram for the TO-252 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B81-Q1 data sheet.

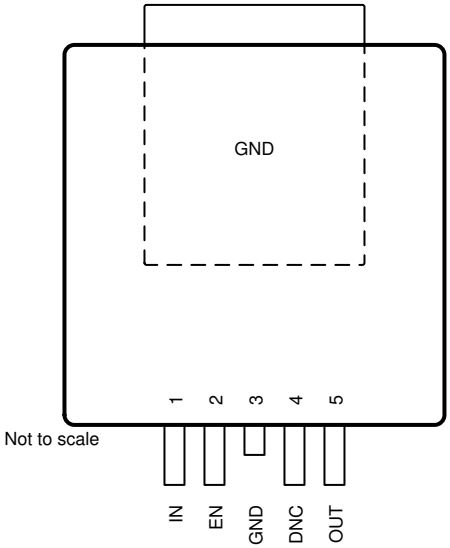

Figure 4-3. Pin Diagram (TO-252 Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
EN	2	The device is stuck in shutdown mode, resulting in no output voltage.	B
GND	3	No effect. Normal operation.	D
DNC	4	No effect. Normal operation.	D
VOUT	5	The device is not operational when the output is pulled to GND. Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
EN	2	The device flips between shutdown mode and normal mode because of the noise on the EN voltage. This condition can result in no output voltage.	B
GND	3	A floating GND pin can result in incorrect voltage regulation or no output voltage.	B
DNC	4	No effect. Normal operation.	D
VOUT	5	The output of the device is disconnected from the load.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	EN (pin 2)	EN is pulled to the IN supply. Shutdown mode is not possible. The device is powered on as long as the input supply is present.	D
EN	2	GND (pin 3)	The device is stuck in shutdown mode, resulting in no output voltage	B
GND	3	DNC (pin 4)	No effect. Normal operation.	D
DNC	4	VOUT (pin 5)	VOUT can fall out of regulation and increased quiescent current can be observed.	C

Table 4-13. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
EN	2	EN is pulled to VBAT. Shutdown mode is not possible. The device is powered on as long as VBAT is present.	C
GND	3	VBAT can discharge if other GND connections on the device are still tied to GND. If all pins are floated to VBAT, this condition can result in VOUT detecting the VBAT voltage.	B
DNC	4	VOUT can fall out of regulation and increased quiescent current can be observed.	C
VOUT	5	The VOUT pin can be damaged and the load being powered by the TPS7B81-Q1 instead uses the VBAT voltage.	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265