Functional Safety Information

LM25143

Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for LM25143 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

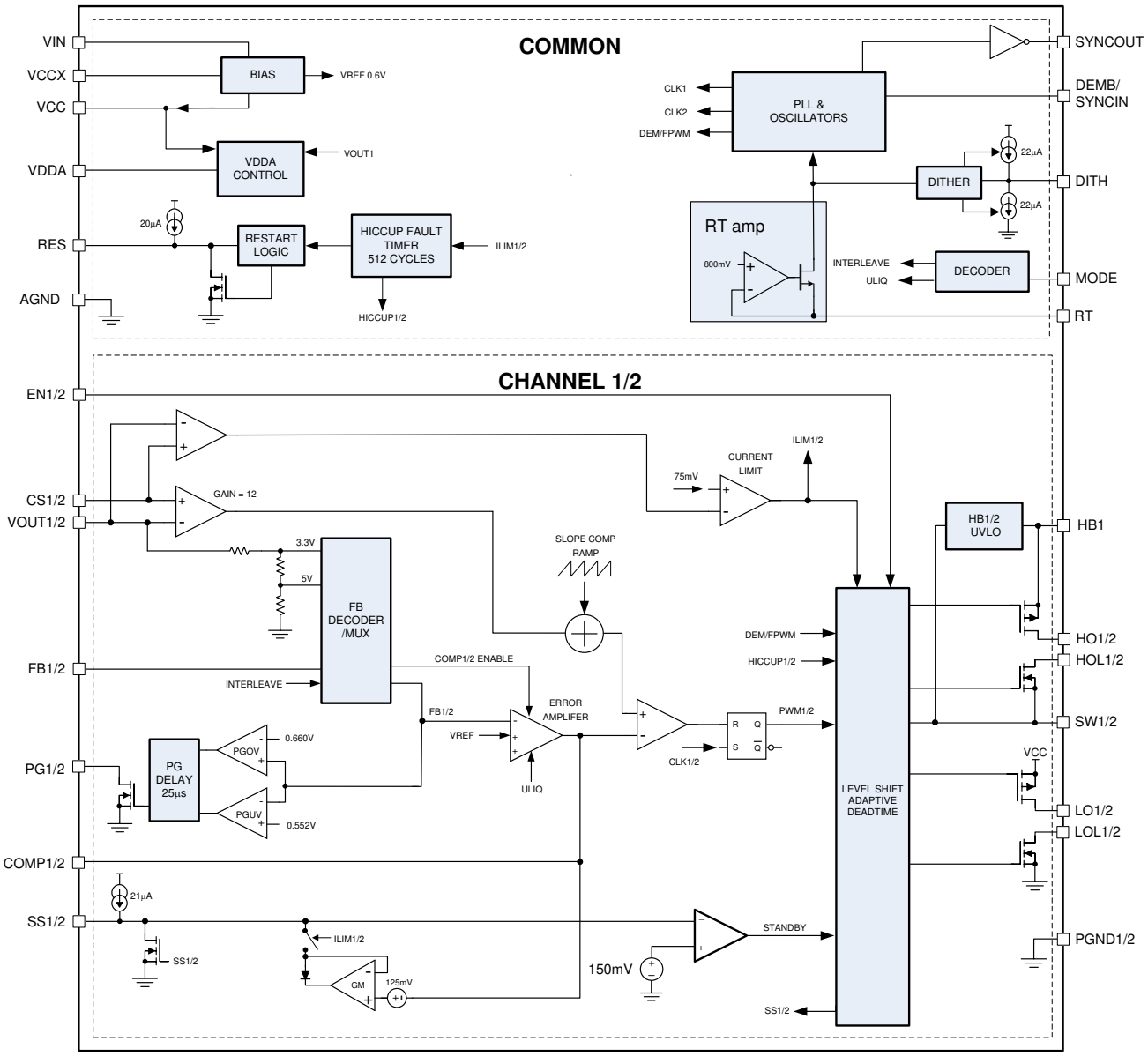

Figure 1-1. Functional Block Diagram

LM25143 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM25143 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	32
Die FIT Rate	7
Package FIT Rate	25

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =< 50V supply	32 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM25143 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW1/2 no output	45%
SW1/2 output not in specification - voltage or timing	40%
SW1/2 power FET stuck on	5%
PG1/2 false trip or fails to trip	5%
Short circuit and two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM25143. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuit to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM25143 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM25143 data sheet.

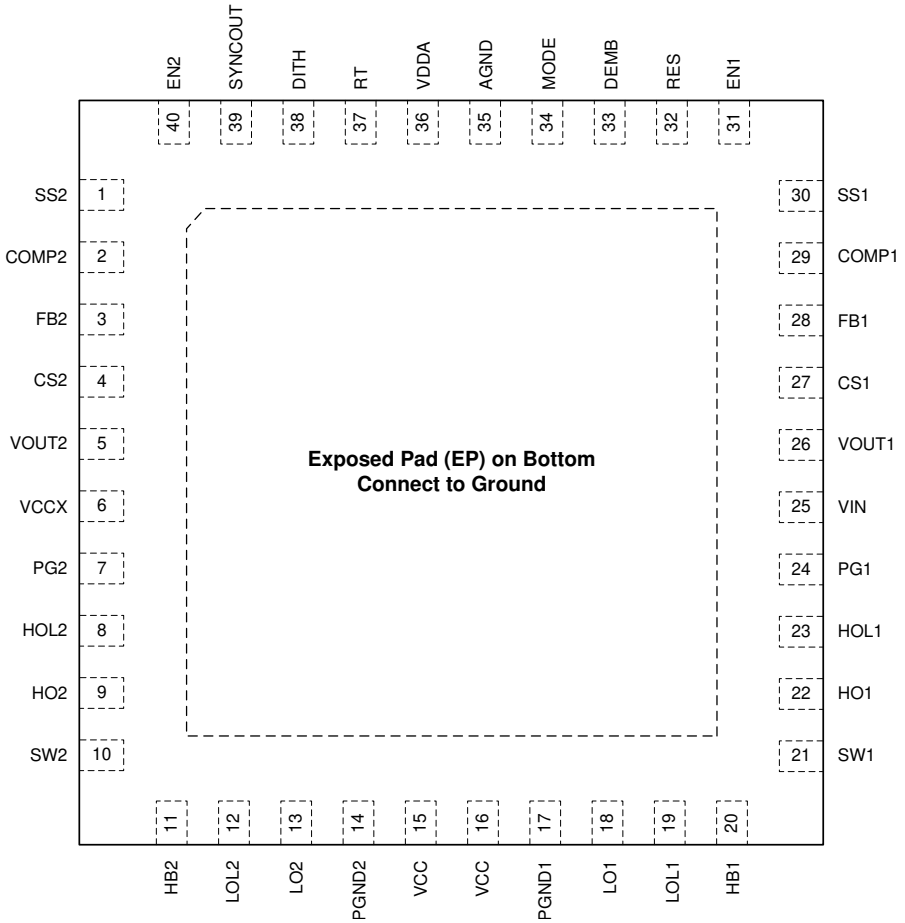

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application Circuit as per LM25143 data sheet is used
- PG1 and PG2 are pulled-up to VOUT1 and VOUT2

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SS2	1	VOUT1 = regulation, VOUT2 = 0 V	B
COMP2	2	VOUT1 = regulation, VOUT2 = 0 V	B
FB2	3	If FB = VDDA, then VOUT1 and VOUT2 = 0 V.	B
		If FB = GND, then VOUT1 = regulation and VOUT2 = 5 V.	B
CS2	4	VOUT1 = regulation, VOUT2 = oscillation	C
VOUT2	5	VOUT1 = regulation, VOUT2 = 0 V, excessive current from VIN, and enters overcurrent protection	B
VCCX	6	If VCCX = GND, then VOUT1 and VOUT2 = regulation.	D
		If VCCX is connected to VOUT2, then VOUT1 = regulation, VOUT2 = 0 V, and the internal VCC regulator is used.	B
		If VCCX is connected to an external supply, then VOUT1 and VOUT2 = regulation.	B
PG2	7	VOUT1 and VOUT2 = regulation, and PG2 is forced low.	B
HOL2	8	VOUT1 and VOUT2 = 0 V. VCC will be discharged through HB2.	B
HO2	9	VOUT1 and VOUT2 = 0 V. VCC will be discharged through HB2.	B
SW2	10	VOUT1 = regulation, VOUT2 = 0 V, and excessive current from VIN	A
HB2	11	VOUT1 and VOUT2 = 0 V. VCC regulator is loaded to current limit.	B
LOL2	12	VOUT1 and VOUT2 = regulation	D
LO2	13	VOUT1 and VOUT2 = regulation	C
PGND2	14	VOUT1 and VOUT2 = regulation	D
VCC	15	VOUT1 and VOUT2 = 0 V	B
VCC	16	VOUT1 and VOUT2 = 0 V	B
PGND1	17	VOUT1 and VOUT2 = regulation	D
LO1	18	VOUT1 and VOUT2 = regulation	C
LOL1	19	VOUT1 and VOUT2 = regulation	C
HB1	20	VOUT1 and VOUT2 = 0 V. VCC regulator is loaded to current limit.	B
SW1	21	VOUT1 = regulation, VOUT2 = 0 V, and excessive current from VIN	B
HO1	22	VOUT1 and VOUT2 = 0 V	B
HOL1	23	VOUT1 and VOUT2 = 0 V	B
PG1	24	VOUT1 and VOUT2 = regulation, and PG1 is forced low.	C
VIN	25	VOUT1 and VOUT2 = 0 V	A
VOUT1	26	VOUT1 = 0 V, VOUT2 = regulation, and excessive current from VIN	B
CS1	27	VOUT1 = oscillation, VOUT2 = regulation	C
FB1	28	If FB1 = VDDA, then VOUT1 and VOUT2 = 0 V.	B
		If FB1 = GND, then VOUT1 = 5 V expected and VOUT2 = regulation.	B
COMP1	29	VOUT1 = 0 V, VOUT2 = regulation	B
SS1	30	VOUT1 = 0 V, VOUT2 = regulation	B
EN1	31	VOUT1 = 0 V, VOUT2 = regulation	B
RES	32	VOUT1 and VOUT2 = regulation, cannot exit hiccup mode	B
DEMB	33	If DEMB = VDDA, then VOUT1 and VOUT2 = 0 V.	B
		VOUT1 and VOUT2 = regulation	C
MODE	34	If MODE = VDDA, then VOUT1 and VOUT2 = 0 V.	B
		If MODE = GND, then VOUT1 and VOUT2 = regulation.	D
AGND	35	VOUT1 and VOUT2 = regulation	D
VDDA	36	VOUT1 and VOUT2 = 0 V, no switching	B
RT	37	VOUT1 and VOUT2 = regulation, operating at the maximum switching frequency	C
DITH	38	VOUT1 and VOUT2 = regulation	C
SYNCOUT	39	VOUT1 and VOUT2 = regulation	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN2	40	VOUT1 = 0 V, VOUT2 = regulation	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SS2	1	VOUT1 and VOUT2 = regulation	D
COMP2	2	VOUT1 = regulation, VOUT2 = oscillation, and will not regulate	C
FB2	3	VOUT2 = regulation, VOUT2 = will not regulate. The controller will be configured for adjustable output.	B
CS2	4	VOUT1 = regulation, VOUT2 oscillation, and no overcurrent detection	A
VOUT2	5	VOUT1 = regulation, VOUT2 = oscillation, and will not regulate	A
VCCX	6	VOUT1 and VOUT2 = regulation	D
PG2	7	VOUT1 and VOUT2 = regulation, no PG2 information	C
HOL2	8	VOUT1 = regulation, VOUT2 = VIN, will not regulate, and excessive current from VIN	D
HO2	9	VOUT1 = regulation, VOUT2 = 0 V, and will not regulate	B
SW2	10	VOUT1 = regulation, VOUT2 = VIN, and high-side FET control floating	A
HB2	11	VOUT1 = regulation, VOUT2 = 0 V, and high-side gate drive floating	B
LOL2	12	VOUT1 = regulation, VOUT2 = 0 V, no gate discharge path for low-side MOSFET	B
LO2	13	VOUT1 and VOUT2 = regulation, lower efficiency	C
PGND2	14	VOUT1 and VOUT2 = 0 V, uncontrolled behavior because of the floating ground	B
VCC	15	VOUT1 and VOUT2 = 0 V	B
VCC	16	VOUT1 and VOUT2 = 0 V	B
PGND1	17	VOUT1 and VOUT2 = 0 V, uncontrolled behavior because of the floating ground	B
LO1	18	VOUT1 = regulation, lower efficiency, and VOUT2 = regulation	C
LOL1	19	VOUT1 = 0 V, no discharge path for low-side MOSFET, and VOUT2 = regulation	B
HB1	20	VOUT1 = regulation, VOUT2 = 0 V, and high-side gate drive floating	B
SW1	21	VOUT1 = no regulation, high-side FET control floating, and VOUT2 = regulation	A
HO1	22	VOUT1 = will not regulate, VOUT2 = regulation	B
HOL1	23	VOUT1 = VIN, will not regulate, excessive current from VIN, and VOUT2 = regulation	C
PG1	24	VOUT1 = regulation, VOUT2 = regulation, and no PG1 information	C
VIN	25	VOUT1 and VOUT2 = 0 V	B
VOUT1	26	VOUT1 = oscillation, will not regulate, and VOUT2 = regulation	A
CS1	27	VOUT1 = oscillation, no overcurrent detection, and VOUT2 = regulation	A
FB1	28	VOUT2 = will not regulate, the controller will be configured for adjustable output, and VOUT2 = regulation.	B
COMP1	29	VOUT1 = oscillation and will not regulate, VOUT2 = regulation	B
SS1	30	VOUT1 and VOUT2 = regulation	D
EN1	31	VOUT1 and VOUT2 = 0 V	B
RES	32	VOUT1 and VOUT2 = regulation, exit hiccup mode current limit quickly	C
DEMB	33	VOUT1 and VOUT2 = regulation, erratic switching	C
MODE	34	VOUT1 = regulation, VOUT2 = 0 V, and error amplifier CH2 is set to zero.	B
AGND	35	VOUT1 and VOUT2 = 0 V	B
VDDA	36	VOUT1 and VOUT2 = 0 V, noisy bias rail	B
RT	37	VOUT1 and VOUT2 = 0 V	B
DITH	38	VOUT1 and VOUT2 = regulation, no spread spectrum	C
SYNCOUT	39	VOUT1 and VOUT2 = 0 V, cannot be synchronized to another part	C
EN2	40	VOUT1 and VOUT2 = 0 V	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SS1	1	COMP2	VOUT1 = regulation, VOUT2 = VIN	B
COMP2	2	FB2	If FB2 = VDDA, then VOUT1 = regulation and VOUT2 = VIN.	A
			If FB2 = GND, then VOUT1 regulation and VOUT2 = 0 V.	B
FB2	3	CS2	If FB2 = VDDA, then VOUT1 = regulation and VOUT2 = 3.3 V.	B
			If FB2 = GND, then VOUT1 = regulation and VOUT = 0 V.	B
CS2	4	VOUT2	VOUT1 = regulation, VOUT2 = oscillation	B
VOUT2	5	VCCX	If VOUT2 < 6.5 V, then VOUT1 and VOUT2 = regulation,	B
			If VOUT2 > 6.5 V, then the device damage exceeds the absolute maximum raring.	A
VCCX	6	PG2	VOUT1 and VOUT2 = regulation, PG2 corrupted	B
PG2	7	HOL2	VOUT1 and VOUT2 = regulation, PG2 corrupted	B
			If HOL2 > 6.5 V and exceeds the maximum rating, PG2 is damaged	A
HOL2	8	HO2	VOUT1 and VOUT2 = regulation	D
HO2	9	SW2	VOUT1 = regulation, VOUT2 < 3 V	B
SW2	10	HB2	VOUT1 = regulation, VOUT2 = 0 V	B
HB2	11	LOL2	VOUT1 and VOUT2 = 0 V	B
LOL2	12	LO2	VOUT1 and VOUT2 = regulation	B
LO2	13	PGND2	VOUT1 and VOUT2 = regulation	B
PGND2	14	VCC	VOUT1 and VOUT2 = 0 V	A
VCC	15	VCC	VOUT1 and VOUT2 = regulation	D
VCC	16	PGND1	VOUT1 and VOUT2 = 0 V	A
PGND1	17	LO1	VOUT1 and VOUT2 = regulation	C
LO1	18	LOL1	VOUT1 and VOUT2 = regulation	D
LOL1	19	HB1	VOUT1 = 0 V, VOUT2 = regulation	B
HB1	20	SW1	VOUT1 = 0 V, VOUT2 = regulation	B
SW1	21	HO1	VOUT1 = 0 V, VOUT2 = regulation	B
HO1	22	HOL1	VOUT1 and VOUT2 = regulation	D
HOL1	23	PG1	VOUT1 and VOUT2 = regulation, PG1 corrupted	D
			If HOL1 > 6.5 V and exceeds the maximum ratings, PG1 can be damaged.	A
PG1	24	VIN	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation. If VIN > 6.5 V and exceeds the maximum rating of PG1, the device is damaged.	A
			If VIN > 6.5 V and exceeds the maximum rating of PG1, the device is damaged.	A
VIN	25	VOUT1	VOUT1 = VIN no switching, VOUT2 = regulation	B
VOUT1	26	CS1	VOUT1 = oscillation, VOUT2 = regulation	B
CS1	27	FB1	If FB1 = VDDA, then VOUT1 = 3.3 V and VOUT2 = regulation.	B
			If FB1 = GND, then VOUT1 = 0 V and VOUT2 = regulation.	B
FB1	28	COMP1	If FB1 = VDDA, then VOUT1 = VIN, excessive current from VIN, and VOUT2 = regulation.	A
			If FB1 = GND, then VOUT1 = 0 V and VOUT2 = regulation.	B
COMP1	29	SS1	VOUT1 = VIN, VOUT2 = regulation	B
SS1	30	EN1	If EN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
			If EN1 > 6.5 V, this exceeds the maximum ratings of SS1 pin and the device will be damaged.	A
EN1	31	RES	If EN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
			If EN1 > 6.5 V, this exceeds the maximum ratings of RES pin and the device will be damaged.	A
RES	32	DEMB	VOUT1 and VOUT2 = regulation	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
DEMB	33	MODE	If DEMB = MODE = GND, then configured as independent dual-output, VOUT1 and VOUT2 = regulation.	B
			If DEMB = MODE = VDDA, then configured as single-output interleaved VOUT1 and VOUT2 = 0 V.	B
MODE	34	AGND	If MODE = GND, then VOUT1 and VOUT2 = regulation and is always in independent dual-output operation.	D
AGND	35	VDDA	VOUT1 and VOUT2 = 0 V	B
VDDA	36	RT	VOUT1 and VOUT2 = 0 V, no switching	B
RT	37	DITH	VOUT1 = VOUT2 = oscillation	B
DITH	38	SYNCOUT	VOUT1 and VOUT2 = regulation, no spread spectrum	C
SYNCOUT	39	EN2	VOUT1 = regulation, VOUT2 = 0 V	B
EN2	40	SS2	If EN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
			If EN1 > 6.5 V, this exceeds the maximum ratings of SS1 pin and the device will be damaged.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SS1	1	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
		If VIN > 6.5 V, then exceeds the SS1 maximum rating and the SS1 pin is damaged.	A
COMP2	2	If VIN > 5 V and < 6.5 V, then VOUT1 and VOUT2 = 0 V.	B
		If VIN > 6.5 V, then exceeds the COMP2 maximum rating and the COMP2 pin is damaged.	A
FB2	3	If VIN < 6.5 V and FB2 = VDDA, then VOUT1 = regulation and VOUT2 = 3.3 V.	B
		If VIN < 6.5 V and FB2 = GND, then VOUT1 and VOUT2 = 0 V and there is excessive current from VIN.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the FB2 pin voltage, then the FB2 pin is damaged.	A
CS2	4	If VIN < 60 V, then VOUT1 = regulation and VOUT2 = VIN.	B
		If VIN > 60 V and exceeds the maximum ratings of the CS2 pin, then the CS2 pin is damaged.	A
VOUT2	5	If VIN < 60 V, then VOUT1 = regulation and VOUT2 = VIN.	B
		If VIN > 60 V and exceeds the maximum ratings of the VOUT2 pin, then the VOUT2 pin is damaged.	A
VCCX	6	If VIN < 6.5 V, if VCCX = VOUT2, then VOUT1 = regulation and VOUT2 = VIN.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the VCCX pin, then the VCCX pin is damaged.	A
PG2	7	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation and PG2 forced is high.	D
		If VIN > 6.5 V and exceeds the maximum ratings of the PG2 pin, the PG2 pin is damaged.	A
HOL2	8	If VIN < 6.5 V, then VOUT1 = regulation, VOUT2 = VIN – dropout, and there is no switching.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the HOL2 pin, then the HOL2 pin is damaged.	A
HO2	9	If VIN < 6.5 V, then VOUT1 = regulation, VOUT2 = VIN – dropout, and there is no switching.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the HO2 pin, then the HO2 pin is damaged.	A
SW2	10	VOUT1 = regulation, VOUT2 = VIN, and excessive current from VIN	B
HB2	11	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation and erratic switching on CH2.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the HB2 pin, then the HB2 pin is damaged.	A
LOL2	12	If VIN < 6.5 V, then VOUT1 and VOUT2 = 0 V and excessive current from VIN.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the LOL2 pin, then the LOL2 pin is damaged.	A
LO2	13	If VIN < 6.5 V, then VOUT1 and VOUT2 = 0 V and excessive current from VIN.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the LO2 pin, then the LO2 pin is damaged.	A
PGND2	14	VOUT and VOUT2 = 0 V, excessive current from VIN	B
VCC	15	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
		If VIN > 6.5 V and exceeds the maximum ratings of the VCC pin, then the VCC pin is damaged.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	16	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
		If VIN > 6.5 V and exceeds the maximum ratings of the VCC pin, then the VCC pin is damaged.	A
PGND1	17	VOUT1 and VOUT2 = 0 V, excessive current from VIN	B
LO1	18	If VIN < 6.5 V, then VOUT1 and VOUT2 = 0 V, and excessive current from VIN.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the LO1 pin, then the LO1 pin is damaged.	A
LOL1	19	If VIN < 6.5 V, then VOUT1 and VOUT2 = 0 V and excessive current from VIN.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the LOL1 pin, then the LOL1 pin is damaged.	A
HB1	20	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	C
		If VIN > 6.5 V and exceeds the maximum ratings of the HB1 pin, then the HB1 pin is damaged.	A
SW1	21	VOUT1 = VIN, VOUT2 = regulation, and excessive current from VIN	B
HO1	22	If VIN < 6.5 V, then VOUT1 = VIN – dropout, VOUT2 = regulation, and no switching.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the HB1 pin, then the HO1 pin is damaged.	A
HOL1	23	If VIN < 6.5 V, then VOUT1 = VIN – dropout, VOUT2 = regulation, and no switching.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the HB1 pin, then the HOL1 pin is damaged.	A
PG1	24	If VIN < 6.5 V, VOUT1 and VOUT2 = regulation and PG1 is forced high.	D
		If VIN > 6.5 V and exceeds the maximum ratings of the PG1 pin, then PG1 pin is damaged.	A
VIN	25	VOUT1 and VOUT2 = regulation	D
VOUT1	26	If VIN < 60 V, then VOUT1 = VIN and VOUT2 = regulation.	B
		If VIN > 60 V and exceeds the maximum ratings of the VOUT1 pin, then the VOUT1 pin is damaged.	A
CS1	27	If VIN < 60 V, then VOUT1 = VIN and VOUT2 = regulation.	B
		If VIN > 60 V and exceeds the maximum ratings of the CS1 pin, then the CS1 pin is damaged.	A
FB1	28	If VIN < 6.5 V and FB1= VDDA, then VOUT1 = 3.3 V and VOUT2 = regulation.	B
		If VIN < 6.5 V and FB1 = GND, then VOUT1 and VOUT2 = 0 V and excessive current from VIN.	B
		If VIN > 6.5 V and exceeds the maximum ratings of the FB1 pin voltage, the FB1 pin is damaged.	A
COMP1	29	If VIN > 5 V and < 6.5 V, then VOUT1 and VOUT2 = 0 V.	B
		If VIN > 6.5 V and exceeds the COMP1 maximum rating, then COMP1 pin is damaged.	A
SS1	30	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
		If VIN > 6.5 V and exceeds the SS1 maximum rating, then SS1 pin is damaged.	A
EN1	31	VOUT1 and VOUT2 regulation	D
RES	32	If VIN < 6.5 V, then VOUT1 = regulation, VOUT2 = regulation, and no hiccup mode.	C
		If VIN > 6.5 V and exceeds the RES maximum rating, then the RES pin is damaged.	A
DEMB	33	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	B
		If VIN > 6.5 V and exceeds the DEMB maximum rating, then the DEMB pin is damaged.	A
MODE	34	If MODE = GND, then VOUT1 and VOUT2 = 0 V.	B
		If MODE = VDDA = and VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	B
		If VIN > 6.5 V and exceeds the MODE pin maximum rating, then the MODE pin is damaged.	A
AGND	35	VOUT1 and VOUT2 = 0 V, excessive current from VIN	B
VDDA	36	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	D
		If VIN > 6.5 V and exceeds the VDDA pin maximum rating, then the VDDA pin is damaged.	A
RT	37	If VIN < 6.5 V, then VOUT1 and VOUT2 = 0 V.	B
		If VIN > 6.5 V and exceeds the RT pin maximum rating, then the RT pin is damaged.	A
DITH	38	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	B
		If VIN > 6.5 V and exceeds the DITH pin maximum rating, then the DITH pin is damaged.	A
SYNCOUT	39	If VIN < 6.5 V, then VOUT1 and VOUT2 = regulation.	B
		If VIN > 6.5 V and exceeds the SYNCOUT pin maximum rating, then the SYNCOUT pin is damaged.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN2	40	VOUT1 and VOUT2 = regulation	D

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265