Application Note

Features of TCAL Agile I/O Expanders

Tyler Townsend

ABSTRACT

This document demonstrates the capabilities of TCAL Agile I/O expanders and explains the benefits of using the TCAL version over the former TCA variant.

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Trademarks

1 Introduction

The TCAL family of I2C I/O expanders offers new and improved functionality on the p-port pins. The Agile I/O's can be adjusted for drive strength, power consumption, EMI, and software related flags. Here are the six features an Agile I/O can offer on a TCAL I/O expander.

- Programmable output drive strength
- Programmable pull-up and pull-down resistors
- Latchable inputs
- Maskable interrupts
- Interrupt status register
- Programmable open drain or push-pull outputs

For the examples provided in this application note, the TCAL6416 is the device in use.

2 Programmable Output Drive Strength

Agile I/O's offer programmable output drive strength that allows the I/O pad to be configured to one of four possible current levels. By programming the bits in the Output Drive Strength Registers, the user can adjust the number of transistor pairs that drive the I/O pad. Table 2-1 is from the TCAL6416 data sheet and describes registers 40, 41, 42, and 43 (Output Drive Strength Registers).

Table 2-1. Registers 40, 41, 42, and 43 (Output Drive Strength Registers)

BIT	CC-03	CC-03	CC-02	CC-02	CC-01	CC-01	CC-00	CC-00
Default	1	1	1	1	1	1	1	1
BIT	CC-07	CC-07	CC-06	CC-06	CC-05	CC-05	CC-04	CC-04
Default	1	1	1	1	1	1	1	1
BIT	CC-13	CC-13	CC-12	CC-12	CC-11	CC-11	CC-10	CC-10
Default	1	1	1	1	1	1	1	1
BIT	CC-17	CC-17	CC-16	CC-16	CC-15	CC-15	CC-14	CC-14
Default	1	1	1	1	1	1	1	1

Each P-port is assigned exactly 2 bits to configure the drive strength of the output driver. For example, P07 (which is the port 0 GPIO 7) output is configured by two bits located in register 41 called CC-07. Two configurable bits presents four different output current level options which are defined in Table 2-2. The default drive strength for an output pin is 1.00x (CC = 11).

Table 2-2. Two-Bit Combination for Adjusting Output Drive Strength on P-Port

CC – XX	Output Strength
00	0.25x
01	0.5x
10	0.75x
11	1.00x

The configurable bits for CC-XX determines the number of transistor pairs that are ON at a given time that feed the I/O pad. Figure 2-1 shows the PMOS/NMOS_EN devices that control the push-pull driving pairs that output on P00 – P07 and P10 – P17. Figure 2-1 is a simplified output stage of the p-port.

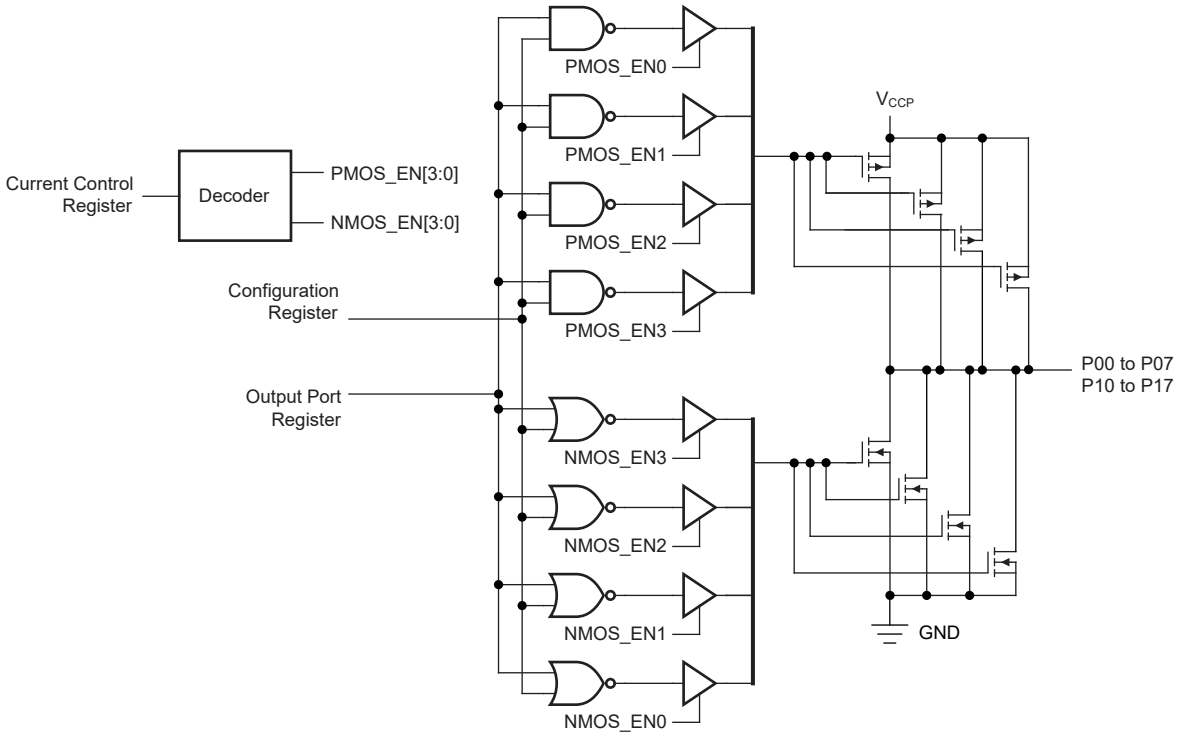

Figure 2-1. Simplified Output Stage

Reducing output drive strength has a few benefits:

- Weaker outputs slow down the slew rate reducing ringing effects.
- Different pins can have different loading conditions, some can require using the full drive strength while others need weaker drive strength. Thus, each pin can be configured separately where some need the original full drive strength configuration.
- Reduces overall power consumption.

3 Programmable Pull-Up or Pull-Down Resistors

Agile I/O's offer programmable internal pull-up or pull-down resistors accessed by register addressing. The user has the ability to internally connect a weak pull-up or pull-down resistor (approximately 100 kΩ) onto the p-port pad. Figure 3-1 is a functional diagram that shows the internal connection and control block for programmable pull-up or pull-down resistors. Pull-up or pull-down resistors are disabled when the p-port is configured as an output.

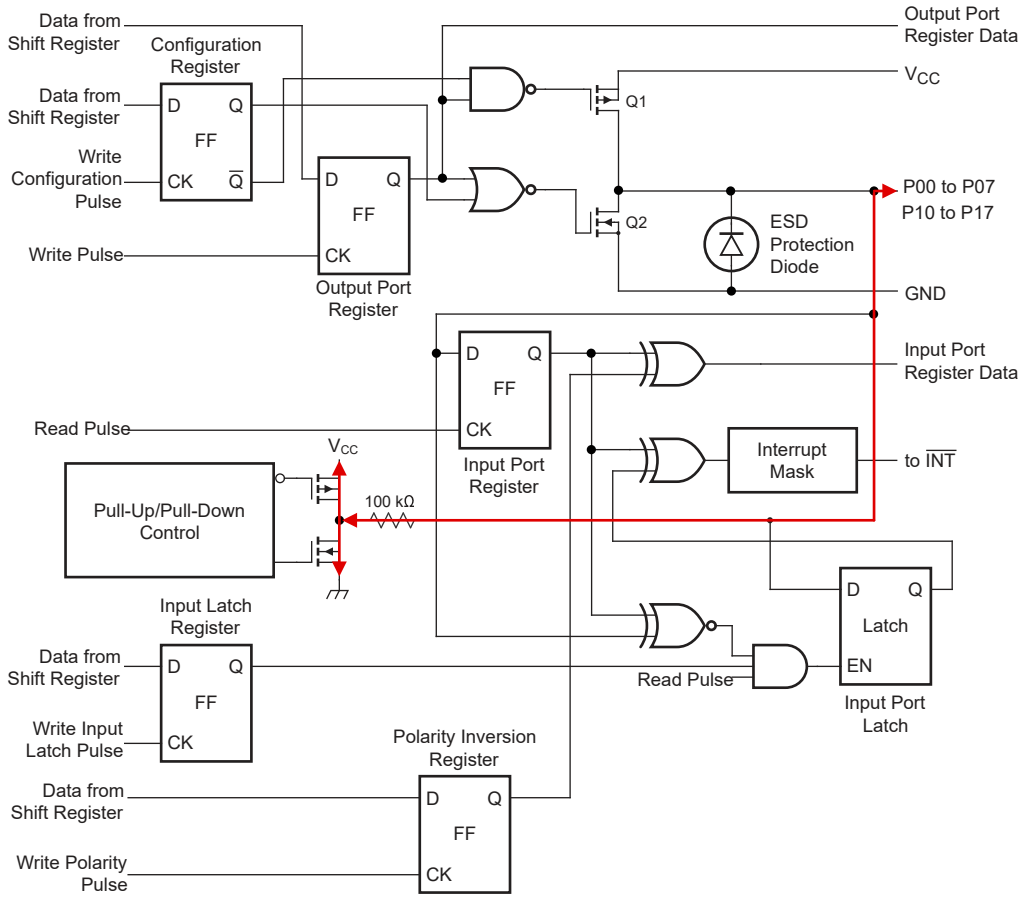

Figure 3-1. Pull-Up or Pull-Down Control Path to P-Ports

4 Latchable Inputs

Latchable inputs are useful when the user wants to maintain that an interrupt is not lost during an input's transition back to the original state. With latchable inputs disabled, a state change in the corresponding input pin generates an interrupt on /INT, and stores the input logic value into the corresponding bit of the input port register (registers 0 and 1). A read of the input register clears the interrupt flag. If the input goes back to the initial logic state before the input port register is read, then the interrupt flag on /INT clears itself which can cause issues because an interrupt can be lost if not read before the input state changes.

This behavior can be observed in the scope capture in Figure 4-1. Input P04 on the TCAL6416 is driven from a high to low logic state. After some time passes, the input is driven back to high. Note that the interrupt that was asserted to low goes back to high once the original input state on P04 is achieved. In this case, the interrupt is lost.

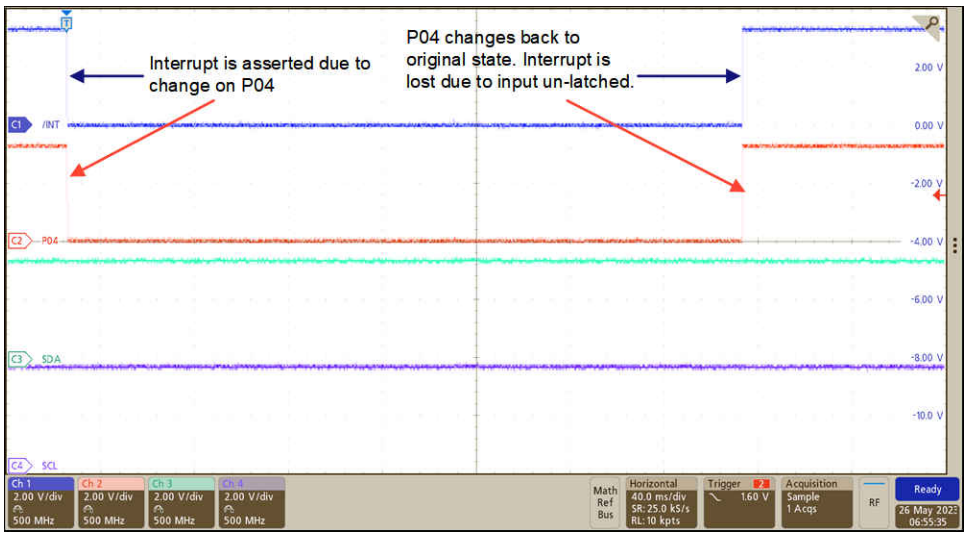

Figure 4-1. Interrupt is Asserted and Lost Due to Input Un-Latched

This situation changes when the latchable input is enabled. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt flag on /INT. In this case, if the input port register is read after the input pin returns to the initial logic state, the interrupt flag on /INT does not clear, and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. This process maintains that no triggered interrupt is lost due to a transition back to original state on the input pin. This behavior can be observed in the scope capture in Figure 4-2.

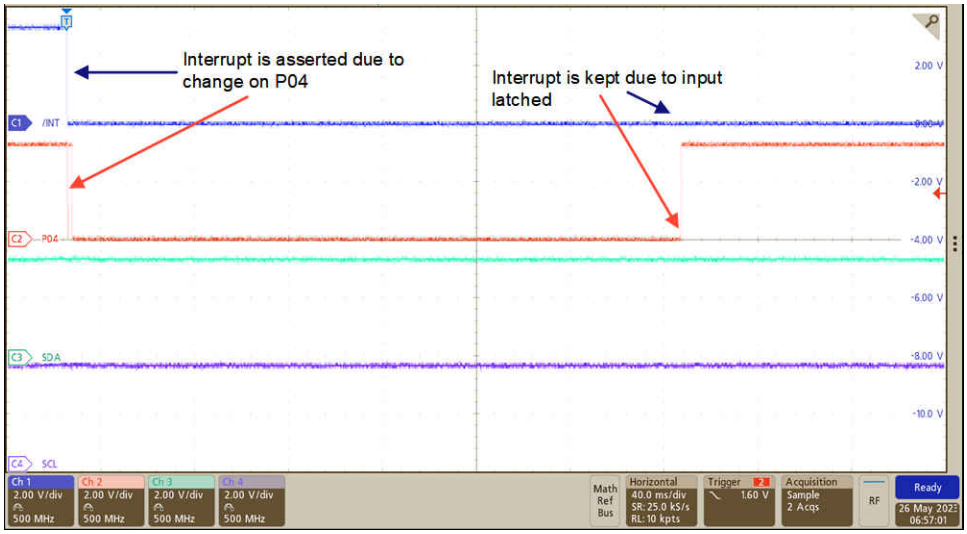

Figure 4-2. Interrupt is Asserted and Kept Due to Input Latched

This behavior is a key difference between TCA devices and TCAL devices concerning the latchable input feature of Agile I/O's.

5 Maskable Interrupt

Using Agile I/O's, the user can choose to turn off or on the built-in interrupts to the I/O expander by enabling or disabling bits in the interrupt mask register. When an interrupt is masked, changes of state on an input do not assert a signal on the interrupt pin. If the interrupt is unmasked, a change in state of an input pin does assert an interrupt.

For example, an input that changes from a 0 to a 1 does not assert an interrupt if masked.

Changing the input from a 0 to a 1 when the interrupt is unmasked does assert an interrupt.

Maskable interrupts are useful in priority switching. When one task is more important than another, the engineer can select to mask an interrupt to push that GPIO's task lower in the priority list.

Figure 5-1 shows P04 changing state from a high to low logic value. This change in state does not assert an interrupt on /INT because the interrupt is masked.

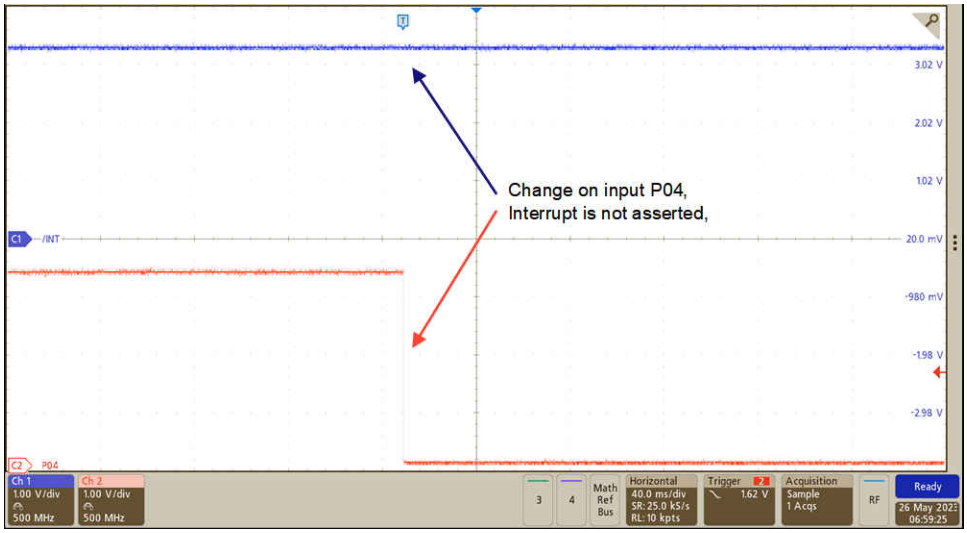

Figure 5-1. Interrupt is Not Asserted with Change on Input P04

In the alternate case in Figure 5-2, the interrupt on P04 is unmasked. In this case, expect to see the /INT pin assert with a corresponding change on the input pin.

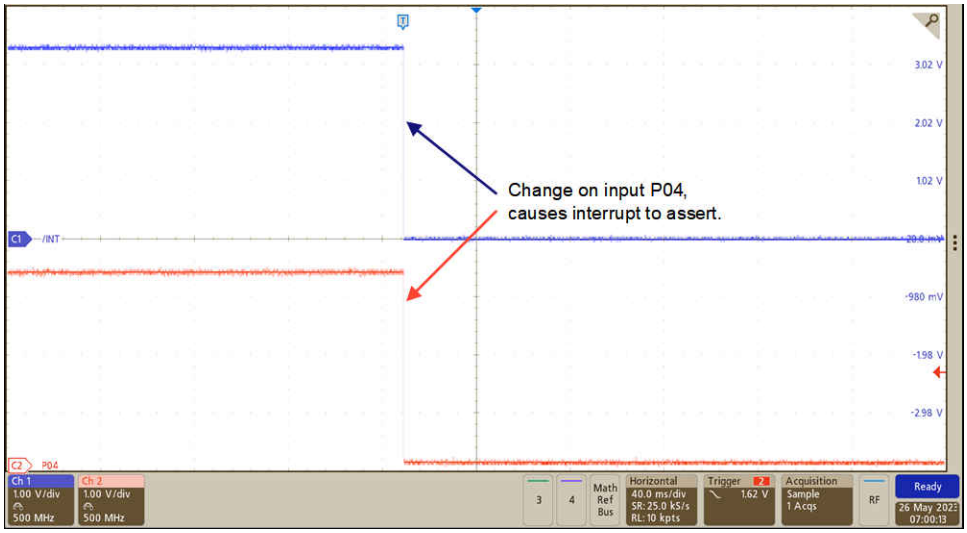

Figure 5-2. Interrupt is Asserted With a Change on P04

6 Interrupt Status Register

The interrupt status registers (0x4C and 0x4D) are read only registers used to identify the source of a triggered interrupt. When the interrupt status register is read, a logic 1 designates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin was not the source of an interrupt.

If a corresponding bit in the interrupt mask register (0x4A and 0x4B) is set to logic 1 (masked), the interrupt state bit returns to logic 0.

For the following example, the TCAL6416 p-port P04 is set to an input and changes from a high to low logic state. Inside the interrupt status register (0x4C) holds the data b00010000 or 0x10 given that the interrupt is not masked. For this example, Bit S-04 = 1 in Table 6-1. Bit S-04 equates to P04 p-port, and the logic 1 indicates that this port set an interrupt because of a change of state on the pin.

Table 6-1. Registers 4C and 4D (Interrupt Status Registers)

BIT	S-07	S-06	S-05	S-04	S-03	S-02	S-01	S-00
Default	0	0	0	0	0	0	0	0
BIT	S-17	S-16	S-15	S-14	S-13	S-12	S-11	S-10
Default	0	0	0	0	0	0	0	0

To check for an interrupt on port 1, the interrupt status register internal to the TCAL6416 (or any TCAL I/O expander) needs to be read. First, there needs to be a write to the TCAL6416 using the device address 0x21 followed by a write bit. Then the address of the interrupt status register 0x4C is sent. The next step is to read from the TCAL6416 by sending the device address 0x21 again followed by a read bit. At this point, data from the interrupt status register (0x4C) is read as 0x10 which correctly identifies that P04 interrupt was triggered thus telling us the input change occurred on p-port P04. This entire process is shown in Figure 6-1.

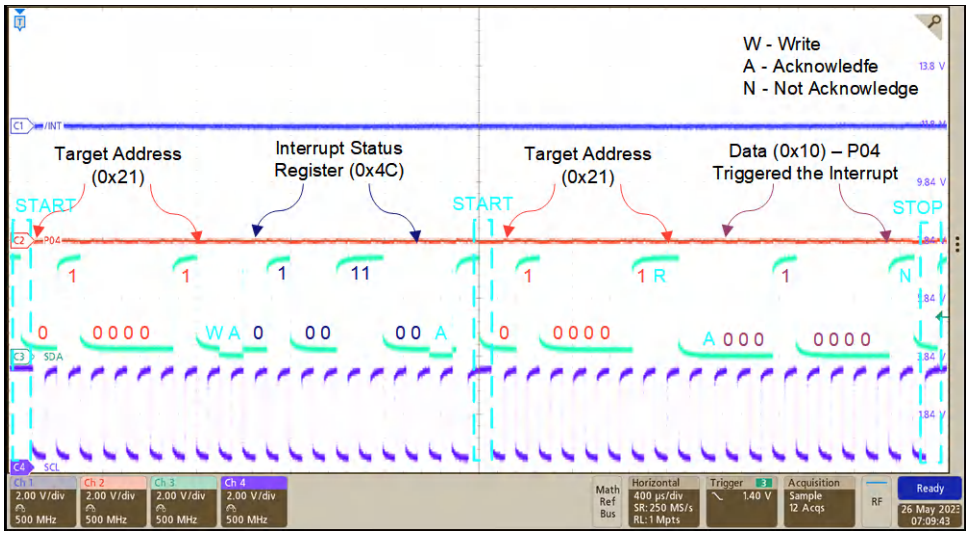

Figure 6-1. Read of Interrupt Status Register Shows that P04 Caused the Interrupt

7 Programmable Open-Drain and Push-Pull Outputs

TI's TCA and TCAL family of devices allow the GPIO pins to be configured for open-drain or push-pull outputs. TCA devices can configure open-drain I/O's by writing to the configuration and output port registers in a specific sequence.

TCAL devices have a built-in output port configuration register from register address 0x4F. The output port configuration register selects port-wise, push-pull, or open-drain I/O stage. A logic 0 configures the I/O as push-pull. A logic 1 configures the I/O as open-drain. ODEN0 configures the Port 0x and ODEN1 configures Port 1x. This information is defined in Table 7-1.

Table 7-1. Register 4F (Output Port Configuration Register)

BIT	Reserved						ODEN-1	ODEN-0
Default	0	0	0	0	0	0	0	0

The affects of using push-pull or open-drain GPIO configurations can be observed by the scope captures taken in Figure 7-1 and Figure 7-2.

The open-drain configuration requires a pull-up resistor on the p-port pin since the drain of the internal FET on the p-port is left floating. This configuration results in a slower rising edge due to the RC time constant caused by the combination of parasitic capacitance and pull-up resistance on the p-port.

The push-pull configuration differs from the open-drain as the push-pull configuration does not require an external pull-up resistor. Internal to the device exists two driving FETS, one to VCC and the other to GND in the push-pull architecture. This configuration results in very fast rise and fall times with steep slew rates, but also introduces larger overshoots and undershoots.

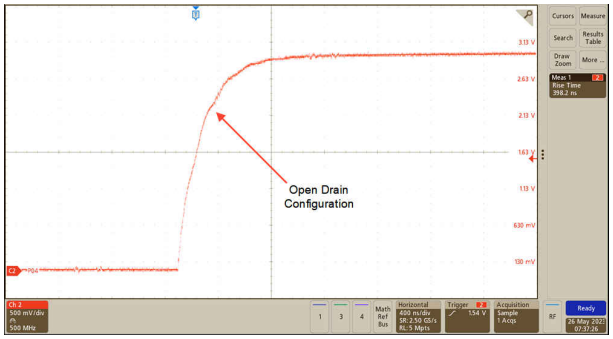

Figure 7-1. Open-Drain Configuration

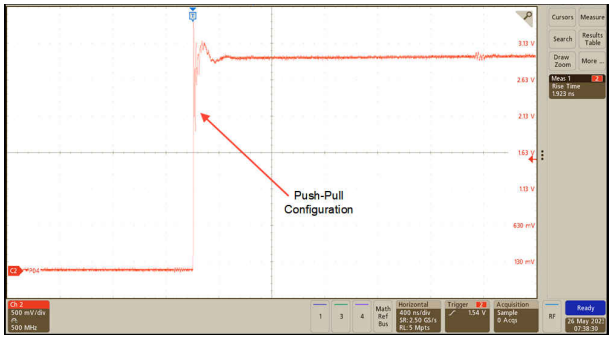

Figure 7-2. Push-Pull Configuration

8 Benefits of Using TCAL I/O Expanders Versus TCA I/O Expanders

TCAL I/O expanders are direct upgrades to the TCA I/O expanders. TCAL is pin-to-pin compatible with TCA of the same part number. For example, TCAL6408 is the direct upgrade to the TCA6408. Here are some of the benefits of using a TCAL I/O expander over a TCA I/O expander.

- Low voltage support (1.08 V – 3.6 V) for next generation processors
- Reduced BoM and board space providing reduced costs
- Newer process technology resulting in improved cost competitive designs
- Supports up to Fast-Mode Plus data rates (1 MHz) allowing increased data throughput (TCA – characterized up to 400 kHz)
- Reduced current consumption for power critical systems
- System adaptability for easy prototyping
- Fixes VCCP/VCCI power supply sequencing issue present in TCA level translating I/O expanders
- Agile I/O Features:
  - Programmable output drive strength
  - Latchable inputs
  - Mask Interrupt and Interrupt status register
  - Programmable output configuration
  - Selectable input pull-up or pull-down registers

Table 8-1 shows the current available TCAL I/O expanders offered by TI.

Table 8-1. TCAL I/O Expanders Device List

TCAL I/O Expanders Comparison Table					
	TCAL6408	TCAL6416	TCAL9538	TCAL9539	TCAL9539-Q1
#of GPIO's	8	16	8	16	16
Pin Count	16	24	16	24	24
Number of Address pins	1	1	2	2	2
Has INT and RESET Pins?	Yes	Yes	Yes	Yes	Yes
Level Translation Supported?	Yes	Yes	No	No	No
Supply Voltage	1.08 V to 3.6 V	1.08 V to 3.6 V	1.08 V to 3.6 V	1.08 V to 3.6 V	1.08 V to 3.6 V
Data Rate	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz
Standby Current	<1 uA at 1.8 V typ	<1 uA at 1.8 V typ	<1 uA at 1.8 V typ	<1 uA at 1.8 V typ	<1 uA at 1.8 V typ
Operating Temperature	-40 C to 125 C	-40 C to 125 C	-40 C to 125 C	-40 C to 125 C	-40 C to 125 C
ESD Protection	+/-4 kV HBM +/-1 kV CDM	+/-4 kV HBM +/-1 kV CDM	+/-4 kV HBM +/-1 kV CDM	+/-4 kV HBM +/-1 kV CDM	+/-4 kV HBM +/-1 kV CDM
Package Types	UQFN, X2QFN	TSSOP, WQFN	UQFN, X2QFN	WQFN	WQFN

9 Summary

TCAL Agile I/O expanders offer a wide range of capabilities on the GPIO pins. These capabilities include programmable output drive strength, integrated pull-up and pull-down resistors, latchable inputs, maskable interrupts, interrupt status register, and programmable options for open-drain and push-pull outputs. TCAL devices are also pin-to-pin compatible with the former TCA variant of I/O expanders. TCAL's are direct upgrades over the TCA's by offering agile I/O capability, low supply voltage support (1.08 V to 3.6 V), all while supporting faster data rates (<1 MHz) and better cost designs due to newer process technology.

10 References

- Texas Instruments, *TCAL6416 16-Bit I2C-Bus, SMBus I/O Expander With Interrupt Output, Reset, and Agile I/O Configuration Registers* data sheet.
- Texas Instruments, *TCAL6408 8-Bit Translating I2C-Bus, SMBus I/O Expander With Interrupt Output, Reset, and Agile I/O Configuration Registers* data sheet.
- Texas Instruments, *TCAL9538 8-Bit I2C-Bus, SMBus I/O Expander With Interrupt Output, Reset, and Agile I/O Configuration Registers* data sheet.
- Texas Instruments, *TCAL9539 Low-Voltage 16-Bit I2C-Bus, SMBus I/O Expander with Interrupt Output, Reset, and Configuration Registers* data sheet.
- Texas Instruments, *TCAL9539-Q1 Automotive Low-Voltage 16-Bit I2C-Bus, SMBus I/O Expander with Interrupt Output, Reset, and Configuration Registers* data sheet.

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