Reliability Report SN74LV8T139-EP Enhanced Product Qualification and Reliability Report



ABSTRACT

TI Device: SN74LV8T139-EP

DLA VID: V62/25610

TI qualification testing is a risk mitigation process that is engineered to assure device longevity in customer applications. Wafer fabrication processes and package level reliability are evaluated in a variety of ways that may include accelerated environmental test conditions with subsequent derating to actual use conditions. Manufacturability of the device is evaluated to verify a robust assembly flow and assure continuity of supply to customers. TI Enhanced Products are qualified with industry standard test methodologies performed to the intent of Joint Electron Devices Engineering Council (JEDEC) standards and procedures. Texas Instruments Enhanced Products are certified to meet GEIA-STD-0002-1 Aerospace Qualified Electronic Components.

Trademarks

All trademarks are the property of their respective owners.

Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing full scale quality and reliability tests on the actual device or using previously qualified devices through *Qualification by Similarity* (QBS) rules. By establishing similarity between the new device and those qualified previously, repetitive tests are eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration. The QBS rules for a technology, product, test parameters or package define which attributes are required to remain fixed for the QBS rules to apply. The attributes which are expected and allowed to vary are reviewed and a QBS plan is developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device is reviewed for conformance to the QBS rule sets applicable to that device. See JEDEC JESD47 for more information.

1

Table 1-1. Enhanced Products New Device Qualification Matrix

Wire Bond LifeMaximum Recommended Operating ConditionsN/AN/APer TI Design RuleElectrical CharacterizationTI Data Sheet103N/AElectrical CharacterizationTI Data Sheet103N/AElectrostatic Discharge SensitivityHBM per TI Data sheet3 units/voltageN/AElA/LESD22-A114 ANSI/ESDA/JEDE JS-001SensitivityCDM per TI Data sheet3 units/voltageN/AElA/LESD22-C101 ANSI/ESDA/JEDE JS-002Latch-upPer Technology3(0)1ElA/JESD22-C101 ANSI/ESDA/JEDE JS-002Latch-upPer Technology3(0)1ElA/JESD22-C101 ANSI/ESDA/JEDE JS-002IbertariaTi Data Sheet5(0)1ElA/JESD22-B10 Thetra/A on boardThermal ImpedanceTheta-JA on boardPer Pin-PackageN/AElA/JESD22-A104(')Biased Humidity or85°C / 85% / 1000 hours thours77(0)3JESD22-A101(')Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(')Or130°C / 85% / 92 hours or 110°C / 85% / 264 hours77(0)3JESD22-A114(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A114(1)Or130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A114(1)Or130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A114(1)Extended Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours<	Enhanced Products New Device Qualification Matrix (Note that qualification by similarity (<i>qualification family</i>) per JEDEC JESD47 is allowed)					
Wire Bond LifeMaximum Recommended Operating ConditionsN/AN/APer TI Design RuleElectrical CharacterizationTI Data Sheet103N/AElectrical CharacterizationTI Data Sheet103N/AElectrostatic Discharge SensitivityHBM per TI Data sheet3 units/voltageN/AElAJESD22-A114 ANSI/ESDAJEDE JS-001Electrostatic Discharge SensitivityPer Technology3(0)1ElAJESD22-C101 ANSI/ESDAJEDE JS-002Latch-upPer Technology3(0)1ElAJESD28-D81 Physical DimensionsTI Data Sheet5(0)1ElAJESD28-D81 Blasel Life Test125°C / 1000 hours or equivalent45(0)3JESD22-A108(1) ANSI/ESD22-D101Biased Humidity or or or85°C / 85% / 1000 hours or equivalent45(0)3JESD22-A101(1) JESD22-A101(1)Extended Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A101(1) JESD22-A101(1)Inbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1) JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A114(1) JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A114(1) JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A114(1)Bake Preconditioning22(0)1ANSI/JSTD-022 UL 1694Bond	Description	Condition	(Allowed		Test Method	
Electrical CharacterizationTI Data Sheet103N/AElectrical CharacterizationTI Data Sheet103N/AElectrostatic Discharge SensitivityCDM per TI Data sheet3 units/voltageN/AElectrostatic Discharge SensitivityCDM per TI Data sheet3 units/voltageN/AElectrostatic Discharge SensitivityPer Technology3(0)1ElA/JESD22-A114 ANS//SDA/JEDE JS-002Latch-upPer Technology3(0)1ElA/JESD22-C101 ANS//SDA/JEDE JS-002Physical DimensionsTI Data Sheet5(0)1ElA/JESD22-B10 ElA/JESD21Thermal ImpedanceTheta-JA on boardPer Pin-PackageN/AElA/JESD22-A101(1) Bias Life TestBias Life Test125°C / 1000 hours or equivalent45(0)3JESD22-A101(1) JESD22-A101(1)Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A101(1) JESD22-A101(1)Inbiased HAST130°C / 85% / 192 hours or 110°C / 85% / 264 hours77(0)3JESD22-A101(1) JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1) JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1) JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1) JESD22-A110(1)Inbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3 <td< td=""><td>Electromigration</td><td>Maximum Recommended Operating Conditions</td><td>N/A</td><td>N/A</td><td>Per TI Design Rules</td></td<>	Electromigration	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules	
HBM per TI Data sheet Aunits/voltage FLA/JESD22-A114 ANSI/ESDA/JEDE JS-001 Sensitivity CDM per TI Data sheet Aunits/voltage N/A EIA/JESD22-C101 ANSI/ESDA/JEDE JS-001 Latch-up Per Technology 3(0) 1 EIA/JESD22-C101 ANSI/ESDA/JEDE JS-002 Latch-up Per Technology 3(0) 1 EIA/JESD22-B10 ANSI/ESDA/JEDE JS-002 Latch-up Per Technology 5(0) 1 EIA/JESD22-B10 ANSI/ESDA/JEDE JS-002 Iterral Impedance Theta-JA on board Per Pin-Package N/A EIA/JESD22-B10 ANSI/ESDA/JEDE JS-002 Biased Humidity or 85°C / 65% / 1000 hours 45(0) 3 JESD22-A110(1) JSED22-A110(1) Biased Humidity or or 85°C / 65% / 2000 hours 77(0) 3 JESD22-A110(1) JSED22-A110(1) Chuiss 130°C / 65% / 192 hours or 110°C / 85% / 526 hours 77(-) 1 JESD22-A110(1) Temperature Cycle 45°C / 65% / 2000 hours 77(-) 3 JESD22-A110(1) Solderability Bake Preconditioning 22(0) 1 ANSI/J-STD-002 Fammability Bake Preconditioning 20(0)	Wire Bond Life	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules	
Base Production Base Production Sumits/voltage Production ANS//ESDA/JEDE JS-001 Sensitivity ANS//ESDA/JEDE Production	Electrical Characterization	TI Data Sheet	10	3	N/A	
SensitivityCDM per TI Data sheetEIA/JESD22-C101 ANS//ESDA/JEDE JS-002Latch-upPer Technology3(0)1EIA/JESD78Physical DimensionsTI Data Sheet5(0)1EIA/JESD78Physical DimensionsTI Data Sheet5(0)1EIA/JESD78Thermal ImpedanceTheta-JA on boardPer Pin-PackageN/AEIA/JESD2-B10Biase Life Test125°C / 1000 hours or equivalent45(0)3JESD22-A108(¹)Biased Humidity or85°C / 85% / 1000 hours77(0)3JESD22-A110(¹)Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A110(¹)Diased HAST130°C / 85% / 96 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)extended Biased HAST ⁽²⁾ 130°C / 85% / 192 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)or130°C / 85% / 192 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)or130°C / 85% / 192 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)or130°C / 85% / 192 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)or130°C / 85% / 192 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)or130°C / 85% / 192 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)or130°C / 85% / 192 hours or 110°C / 85% / 26877(0)3JESD22-A110(¹)Temperature Cycle65°C to +150°C non-biased for 500 cycles or or Method A - UL 94V-0 or Method B - EC standard 6		HBM per TI Data sheet	3 units/voltage	N/A	EIA/JESD22-A114 or ANSI/ESDA/JEDEC JS-001	
Physical DimensionsTI Data Sheet5001EIA/JESD22- B10Thermal ImpedanceTheta-JA on boardPer Pin-PackageN/AEIA/JESD1Bias Life Test125°C / 1000 hours or equivalent45(0)3JESD22-A108(1)Biased Humidity or85°C / 85% / 1000 hours $45(0)$ 3JESD22-A108(1)Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A110(1)Extended Biased Humidity ⁽²⁾ 85°C / 85% / 2000 hours $77(-)$ 1JESD22-A110(1)or130°C / 85% / 192 hours or 110°C / 85% / 52877(-)1JESD22-A110(1)Extended Biased HAST130°C / 85% / 192 hours or 110°C / 85% / 26477(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A118(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A118(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A118(1)SolderabilityBake Preconditioning22(0)1ANSI/J-STD-002FlammabilityBake Preconditioning22(0)1ANSI/J-STD-002FlammabilityPer wire size505001s x 30(0) bonds3JESD22-B116Bond ShearPer wire size50013ASTM F-459 or TM2Die ShearPer die size5(0)3TM 2019High Temp Stor		CDM per TI Data sheet			EIA/JESD22-C101 or ANSI/ESDA/JEDEC JS-002	
Thermal ImpedanceTheta-JA on boardPer Pin-PackageN/AEIA/JESD51Bias Life Test $125^{\circ}C / 1000$ hours or equivalent $45(0)$ 3 $JESD22-A108^{(1)}$ Biased Humidity or $85^{\circ}C / 85\% / 1000$ hours $45(0)$ 3 $JESD22-A101^{(1)}$ Biased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(0)$ 3 $JESD22-A110^{(1)}$ Extended Biased Humidity ⁽²⁾ $85^{\circ}C / 85\% / 2000$ hours $77(-)$ 1 $JESD22-A110^{(1)}$ or $130^{\circ}C / 85\% / 192$ hours or $110^{\circ}C / 85\% / 528$ $77(-)$ 1 $JESD22-A110^{(1)}$ Unbiased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(-)$ 3 $JESD22-A110^{(1)}$ Unbiased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(-)$ 3 $JESD22-A110^{(1)}$ Unbiased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(-)$ 3 $JESD22-A110^{(1)}$ Unbiased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(-)$ 3 $JESD22-A.118^{(1)}$ Unbiased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(-)$ 3 $JESD22-A.118^{(1)}$ Unbiased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(-)$ 3 $JESD22-A.118^{(1)}$ Unbiased HAST $130^{\circ}C / 85\% / 96$ hours or $110^{\circ}C / 85\% / 264$ $77(-)$ 3 $JESD22-A.118^{(1)}$ SolderabilityBake Preconditioning $22(-)$ 1 $ANSI/J-STD-022$ FlammabilityBake Preconditioning $20(-)$ 3 $JESD22-B116$	Latch-up	Per Technology	3(0)	1	EIA/JESD78	
Bias Life Test 125°C / 1000 hours or equivalent 45(0) 3 JESD22-A108 ⁽¹⁾ Biased Humidity or 85°C / 85% / 1000 hours 77(0) 3 JESD22-A110 ⁽¹⁾ Biased HAST 130°C / 85% / 96 hours or 110°C / 85% / 264 hours 77(0) 3 JESD22-A110 ⁽¹⁾ Extended Biased Humidity ⁽²⁾ or 85°C / 85% / 2000 hours or 110°C / 85% / 264 hours 77(-) 1 JESD22-A110 ⁽¹⁾ Extended Biased HAST ⁽²⁾ 130°C / 85% / 192 hours or 110°C / 85% / 264 hours 77(-) 1 JESD22-A110 ⁽¹⁾ Unbiased HAST 130°C / 85% / 96 hours or 110°C / 85% / 264 hours 77(0) 3 JESD22-A118 ⁽¹⁾ Temperature Cycle -65°C to +150°C non-biased for 500 cycles or equivalent 77(0) 3 JESD22-A110 ⁽¹⁾ Solderability Bake Preconditioning 22(0) 1 ANSI/J-STD-002 Flammability Method A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 1694 5(0) 1 JESD22-B116 Bond Shear Per wire size 5 units x 30(0) bonds 3 JESD22-B116 Bond Pull Strength Per die size 5(0) 3 ASTM F-459 or TM2 <td>Physical Dimensions</td> <td>TI Data Sheet</td> <td>5(0)</td> <td>1</td> <td>EIA/JESD22- B100</td>	Physical Dimensions	TI Data Sheet	5(0)	1	EIA/JESD22- B100	
Biased Humidity or Biased HASTB5°C / 85% / 1000 hours hours77(0)3JESD22-A10(1) JESD22-A110(1)Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)Extended Biased Humidity(2) or Extended Biased HAST(2)85°C / 85% / 2000 hours or 110°C / 85% / 528 hours77(-)1JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A110(1)SolderabilityBake Preconditioning22(0)1ANSI/J-STD-002 UL 94V-0 por Method A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 16945(0)1UL 94V-0 UL 94V-0 UL 1694Bond ShearPer wire size5 units x 30(0) bonds3JESD22-B116Bond Pull StrengthPer wire size5(0)3ASTM F-459 or TM2 DiondsDie ShearPer die size5(0)3	Thermal Impedance	Theta-JA on board	Per Pin-Package	N/A	EIA/JESD51	
Biased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A110(1)Extended Biased Humidity(2)85°C / 85% / 2000 hoursJESD22-A110(1)JESD22-A110(1)or130°C / 85% / 192 hours or 110°C / 85% / 52877(-)1JESD22-A110(1)Extended Biased HAST(2)130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 26477(0)3JESD22-A.118(1)Temperature Cycle-65°C to +150°C non-biased for 500 cycles or equivalent77(0)3JESD22-A.118(1)SolderabilityBake Preconditioning22(0)1ANSI/J-STD-002FlammabilityMethod A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 16945(0)1JESD22-B116Bond ShearPer wire size5 units x 30(0) bonds3JESD22-B116Bond Pull StrengthPer wire size5(0)3TM 2019High Temp Storage150°C / 1000 hours15(0)3JESD22-A103(1)	Bias Life Test	125°C / 1000 hours or equivalent	45(0)	3	JESD22-A108 ⁽¹⁾	
Biased HASTHoursJESD22-A110(1)Extended Biased Humidity(2) or85°C / 85% / 2000 hours77(-)1JESD22-A10(1)Extended Biased HAST(2)130°C / 85% / 192 hours or 110°C / 85% / 528 hours77(-)1JESD22-A110(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A118(1)Temperature Cycle-65°C to +150°C non-biased for 500 cycles or equivalent77(0)3JESD22-A104(1)SolderabilityBake Preconditioning22(0)1ANSI/JSTD-002FlammabilityMethod A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 1694500 mits x 30(0) bonds3JESD22-B116Bond ShearPer wire size5 units x 30(0) bonds3ASTM F-459 or TM2Die ShearPer die size5(0)3TM 2019High Temp Storage150°C / 1000 hours15(0)3JESD22-A103(1)	Biased Humidity or	85°C / 85% / 1000 hours	77(0)	3	JESD22-A101 ⁽¹⁾	
or130°C / 85% / 192 hours or 110°C / 85% / 52877(-)11JESD22-A110(1)Lubiased HAST (2)130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A.118(1)Unbiased HAST130°C / 85% / 96 hours or 110°C / 85% / 264 hours77(0)3JESD22-A.118(1)Temperature Cycle-65°C to +150°C non-biased for 500 cycles or equivalent77(0)3JESD22-A.118(1)SolderabilityBake Preconditioning22(0)1ANSI/J-STD-002FlammabilityMethod A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 16945(0)1JESD22-B116Bond ShearPer wire size5 units x 30(0) bonds3JESD22-B116Bond Pull StrengthPer wire size5(0)3ASTM F-459 or TM2Die ShearPer die size5(0)3JESD22-A103(1)High Temp Storage150°C / 1000 hours15(0)3JESD22-A103(1)	Biased HAST				JESD22-A110 ⁽¹⁾	
Unbiased HAS1hours77(0)3JESD22-A.118(1)Temperature Cycle-65°C to +150°C non-biased for 500 cycles or equivalent77(0)3JESD22-A104(1)SolderabilityBake Preconditioning22(0)1ANSI/J-STD-002FlammabilityMethod A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 16945(0)1UL 94V-0 IEC standard 695-2 UL 1694Bond ShearPer wire size5 units x 30(0) bonds3JESD22-B116Bond Pull StrengthPer wire size5(0)3ASTM F-459 or TM2 Die ShearHigh Temp Storage150 °C / 1000 hours15(0)3JESD22-A103(1)	or	130°C / 85% / 192 hours or 110°C / 85% / 528	77(-)	1	JESD22-A101 ⁽¹⁾ JESD22-A110 ⁽¹⁾	
Temperature Cycleequivalent77(0)3JESD22-A104(7)SolderabilityBake Preconditioning22(0)1ANSI/J-STD-002Method A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 16945(0)1IEC standard 695-2 UL 1694Bond ShearPer wire size5 units x 30(0) 	Unbiased HAST		77(0)	3	JESD22-A.118 ⁽¹⁾	
FlammabilityMethod A - UL 94V-0 or Method B - IEC standard 695-2-2 or Method C - UL 16945(0)1UL 94V-0 IEC standard 695-2 UL 1694Bond ShearPer wire size5 units x 30(0) bonds3JESD22-B116Bond Pull StrengthPer wire size5 units x 30(0) bonds3ASTM F-459 or TM2Die ShearPer die size5(0)3TM 2019High Temp Storage150 °C / 1000 hours15(0)3JESD22-A103 ⁽¹⁾	Temperature Cycle		77(0)	3	JESD22-A104 ⁽¹⁾	
Flammabilityor Method B - IEC standard 695-2-2 or Method C - UL 16945(0)1IEC standard 695-2 UL 1694Bond ShearPer wire size5 units x 30(0) bonds3JESD22-B116Bond Pull StrengthPer wire size5 units x 30(0) bonds3ASTM F-459 or TM2Die ShearPer die size5(0)3TM 2019High Temp Storage150 °C / 1000 hours15(0)3JESD22-A103 ⁽¹⁾	Solderability	Bake Preconditioning	22(0)	1	ANSI/J-STD-002	
Bond SnearPer wire sizebonds3JESD22-B116Bond Pull StrengthPer wire size5 units x 30(0) bonds3ASTM F-459 or TM2Die ShearPer die size5(0)3TM 2019High Temp Storage150 °C / 1000 hours15(0)3JESD22-A103 ⁽¹⁾	Flammability	or Method B - IEC standard 695-2-2	5(0)	1	IEC standard 695-2-2	
Bond Pull StrengthPer wire sizebonds3ASTM F-459 of TM2Die ShearPer die size5(0)3TM 2019High Temp Storage150 °C / 1000 hours15(0)3JESD22-A103 ⁽¹⁾	Bond Shear	Per wire size		3	JESD22-B116	
High Temp Storage 150 °C / 1000 hours 15(0) 3 JESD22-A103 ⁽¹⁾	Bond Pull Strength	Per wire size	• • • •	3	ASTM F-459 or TM2011	
	Die Shear	Per die size	5(0)	3	TM 2019	
Moisture Sensitivity Surface Mount Only 12 1 J-STD-020 ⁽¹⁾	High Temp Storage	150 °C / 1000 hours	15(0)	3	JESD22-A103 ⁽¹⁾	
	Moisture Sensitivity	Surface Mount Only	12	1	J-STD-020 ⁽¹⁾	

(1) Precondition performed per JEDEC Std. 22, Method A112/A113.

(2) For information only.

TEXAS INSTRUMENTS www.ti.com

Technology Family FIT / MTBF Data

Mean Time Between Fails (MTBF) and Failures in Time (FIT) rates are device reliability statistics calculated based on data collected from TI's internal reliability testing (life test).

TI's DPPM/FIT/MTBF Estimator Search Tool reports the generic data based on technology groupings and shows conditions under which the rates were derived. All terms used in the tool and definitions can be found on the TI reliability terminology page. Failure rates are summarized by technology and mapped to the associated material part numbers. The failure rates are highly dependent on the number of units tested, therefore, it is not recommended to compare failure rates.

TI DPPM/FIT/MTBF Estimator Search Tool webpage link:

www.ti.com/quality/docs/estimator.tsp

Device Family Qualification Data

TI's Qualification Summary Search Tool reports generic qualification data representative of the material sets, processes, and manufacturing sites used by the device family and may not include all of the testing performed for a specific EP device. Please see the Enhanced Products New Device Qualification Matrix above for the full suite of qualification testing performed to release Enhanced Product devices.

TI Qualification Summary Search webpage link:

www.ti.com/qualificationsummary/qualsumm/home

Ongoing Reliability Monitoring

TI periodically monitors the reliability of its products, wafer fab processes, and package technologies, through its Ongoing Reliability Monitor (ORM) program. The ORM program involves collecting environmental reliability stress data on representative sets of devices, processes and packages. The results from the ORM program are updated quarterly in this report.

TI Ongoing Reliability Monitoring Search webpage link:

www.ti.com/orm/home?actionId=2801.html

For additional information or technical support please contact the Texas Instruments Customer Support Center. For more information on TI Enhanced Products, click here.

3

Important Limitations on Use of Data Exceeding Specified Limits

TI is providing this data for your convenience. However, we want to make clear the significant limitations of its usefulness as an indicator of how devices may perform in various applications.

THIS DATA IS PROVIDED "AS IS" WITHOUT ANY EXPRESS OR IMPLIED WARRANTY OF ANY KIND INCLUDING WARRANTIES OF MERCHANTABILITY, NONINFRINGEMENT OF INTELLECTUAL PROPERTY, OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT SHALL TI OR ITS SUPPLIERS BE LIABLE FOR ANY DAMAGES WHATSOEVER (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, LOSS OF INFORMATION) ARISING OUT OF THE USE OF OR INABILITY TO USE THE INFORMATION, EVEN IF TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Your use of this data, and all consequences of such use, is solely your responsibility. You must perform sufficient engineering and additional qualification testing in order to properly evaluate your application and determine whether a candidate device is suitable for use in that application.

TI semiconductor components are specifically designed and manufactured to be used within the electrical, thermal, mechanical and other parameters set forth in TI's product data sheets. Quality and reliability data provided by Texas Instruments, such as MTBF and fit rate data, is intended to be an estimate of product performance based upon history only. It does not imply that any performance levels reflected in such data can be met if the product is operated outside the conditions expressly stated in the latest published data sheet for a device.

Plastic encapsulated TI semiconductor devices are neither designed nor warranted as suitable for use in military applications and/or military environments.

THIS INFORMATION SHOULD NOT BE USED TO ASSIST IN THE PRACTICE OF "UPRATING" OR "UPSCREENING" DEVICES FOR USE IN MILITARY OR OTHER CRITICAL APPLICATIONS. There are significant limitations of this information as an indicator of how commercial, off-the-shelf (COTS) devices may perform in such applications or environments, and about the hazards of using COTS devices in such applications. TI strongly believes that semiconductor components should never be used outside their specified tolerance levels as up-screening can lead directly to system or component failure. Such failures may present distinct risks to end-users and to third parties. TI cannot accept any responsibility for component or system failures that occur due to the misuse of its products, including misuse that may result from the practice of up-screening.

Any use of TI components beyond their rated limits voids all warranty responsibility of TI with respect to such devices, and also voids all responsibility of TI with respect to any applications assistance, product design, software performance or services of any kind that were or may have been performed in connection with the sale of any such devices. Further, resale of TI's products or services with statements different from or beyond the parameters stated by TI for that product or service in official TI data books or data sheets, or without the warnings or instructions provided by TI, voids all express and any implied warranties for the associated TI product or service, and is an unfair and deceptive business practice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated