Application Brief

Optimizing Industrial Robot CPU Boards with Logic and Voltage Translation

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Functional Block Diagram

For the purpose of this report, a simplified robot CPU board block diagram is used to illustrate the logic and translation use cases, see Figure 1. Each red block has an associated use-case document. Links are provided in Table 1 and Table 2. For a more complete block diagram, see the *Robot CPU Board Products and Reference Design* pages.

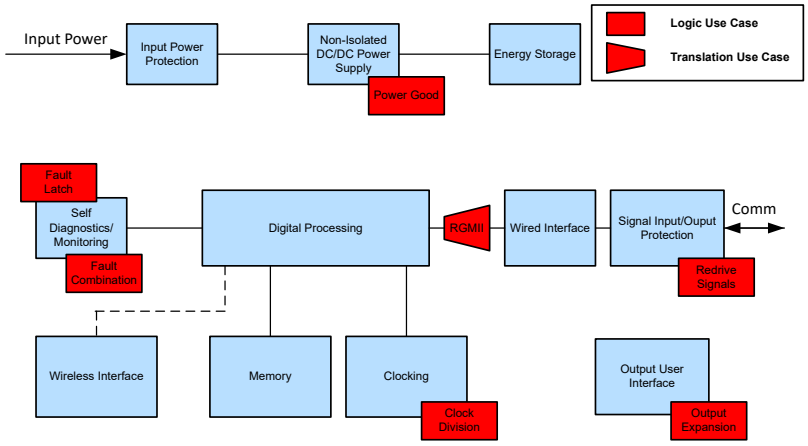

Figure 1. Simplified Block Diagram for Robot CPU Boards

Logic and Translation Use Cases

Each use case is linked to a separate short document that provides additional details including a block diagram, design tips, and part recommendations. The nearest block and use-case identifiers are listed to match up exactly to the use cases shown in the provided Simplified Block Diagram for Robot CPU Boards.

Table 1. Logic Use Cases

Nearest Block	Use-Case Identifier	Use Case
Self-Diagnostics/Monitoring	Fault Latch	*Catch a Digital Pulse* *Multiple Fault Monitoring*
	Fault Combination	*Use Fewer Inputs to Monitor Error Signals*
Clocking	Clock Division	*Dividing a Clock*
Non Isolated DC/DC Power Supply	Power Good	*Combine Power Good Signals*
Signal Input/Output Protection	Redrive Signals	*Redrive Digital Signals*
Output User Interface	Output Expansion	*Drive Indicator LEDs*

Table 2. Translation Use Cases

Nearest Block	Use-Case Identifier	Use Case
Wired Interface	RGMII	*Translate Voltages for RGMII*

Dividing a Clock

It is common to see clocks be used in industrial robot CPU boards however not all devices are able to use the clock at its fastest. For devices to be able to operate, the user can divide the clock by using D-type flip-flops(DFF). Using DFFs to divide your clock frequency will result in values of $\frac{clock}{2^n}$ where n is the number of DFFs connected in series. This is shown in Figure 2.

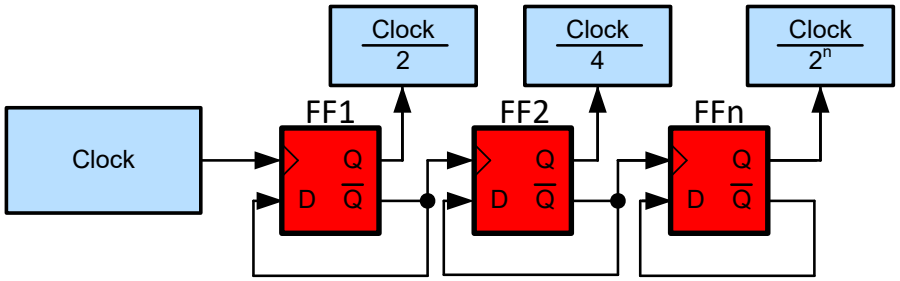

Figure 2. Example of Dividing a Clock

Design Considerations

- Effect can be accomplished using a counter
- Latched devices start in an unknown state [FAQ] What is the default output of a latched device? (Flip-Flop, latch, register)
- Depending on propagation delays the clock will not only be delayed but also behind by a few nanoseconds.
- [FAQ] How do I Calculate Power Consumption for my CMOS Logic Device?
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*

Table 3. Recommended Parts

Part Number	Automotive Qualified	Operating Voltage Range	Features
SN74AUP1G74		0.8 V to 3.6 V	AUP family logic devices are extremely low power, and fast; I_{CC} < 0.9 µA; t_{pd} 5 - 10 ns
			Clear and preset
SN74AUP1G80		0.8 V to 3.6 V	AUP family logic devices are extremely low power, and fast; I_{CC} < 0.9 µA; t_{pd} 5 - 10 ns Only inverted Q output
SN74AUC1G74		0.8 V to 2.7 V	Extremely high speed at 1.8 V; t_{pd} < 2.4 ns
SN74LVC1G374		1.65 V to 5.5 V	High drive strength 32 mA 3-State outputs Over-voltage inputs
SN74LVC1G374-Q1	✓		
SN74LVC1G74			High drive strength 32 mA Push-Pull outputs Over voltage tolerant inputs
SN74LVC2G74-Q1	✓		
SN74HCS393		2 V to 6 V	Counter Up to 8 divisions

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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