Application Report
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Optimizing Design of Electronic Meters With Logic and Translation Use Cases

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ABSTRACT

Electronic meters integrate numerous common subsystems whether they measure electricity, heat, gas, or water. Though the electronic meters, also known as smart meters, differ in what they measure, they share similar digital interfacing challenges, such as communicating with different wired and wireless interfaces. All of the use cases shown in the *Block Diagram* and *Logic and Translation Use Cases* sections of this document are commonly seen in electronic meter designs.

Logic gates, voltage translators, and other logic devices are utilized for many purposes throughout modern electronic systems. This document provides example solutions for common design challenges that can be solved using logic and translation. Not all of the solutions here appear in every system; however, all solutions shown are commonly used and effective.

There are dozens of logic families available from Texas Instruments, and it can be difficult to select the right one for the application. Electronic meters vary in features, but the key design parameters remain the same making it easier to identify an appropriate family for this application. See *Section 4* for help finding the right logic family for the use case.

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Trademarks

1 Block Diagram

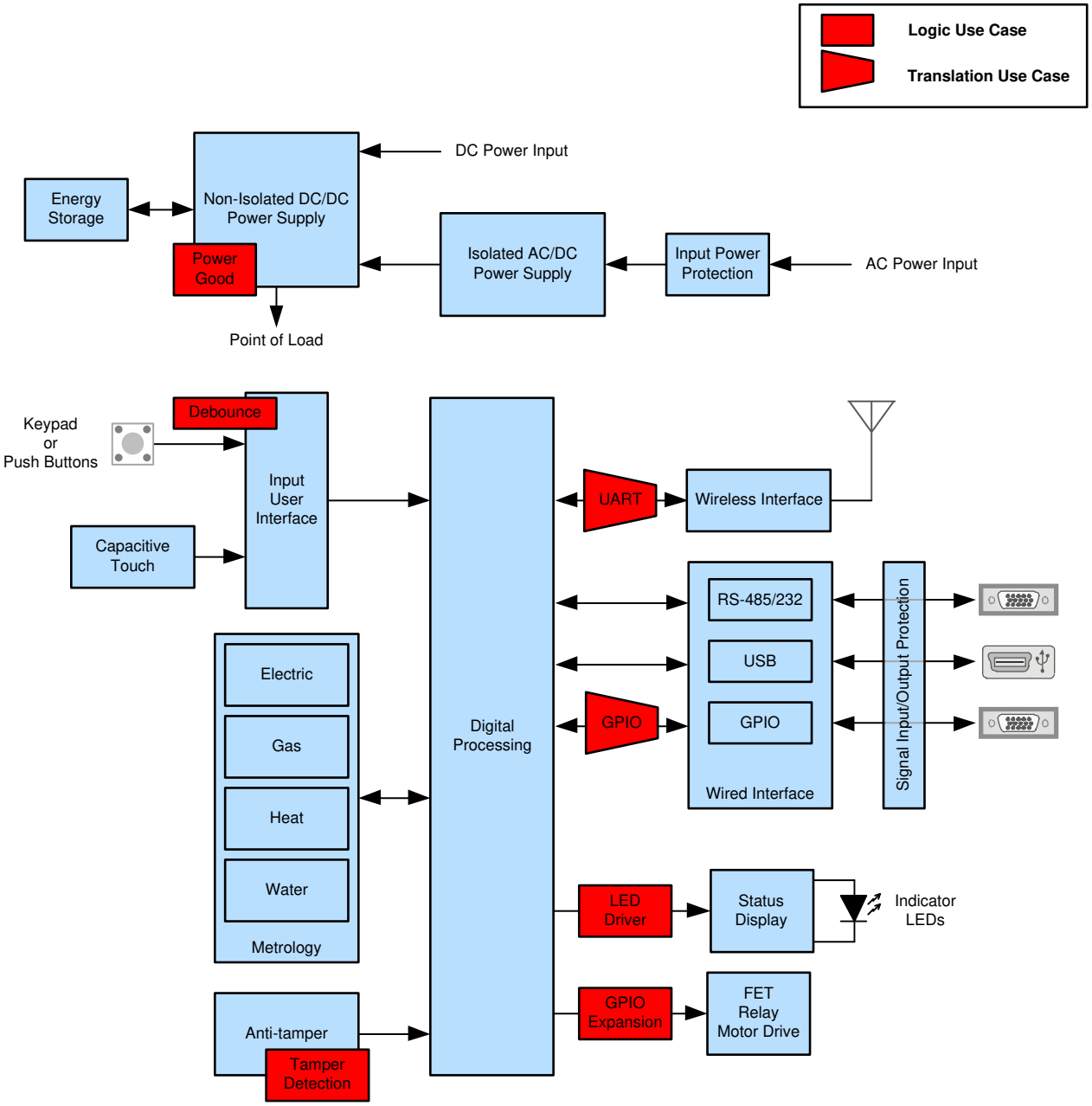

Figure 1. Simplified Block Diagram for Electronic Meters

For the purpose of this report, a simplified electronic meter system block diagram is used to illustrate the logic and translation use cases, see Figure 1. For a more complete view, see the interactive online end equipment reference diagrams for smart meters.

2 Optimizing Communication with Wireless Interfaces

It is common for smart meters to utilize wireless interfaces such as Wi-Fi®, ZigBee®, or Bluetooth® to connect to a local network. In many designs, the simplest method to achieve this is to utilize pre-built and pre-approved modules. These modules often have limited voltage operation ranges, and to support their usage, voltage-level shifters are typically required between the extremely low-power processor, often operating as low as 1.2 V, and the wireless module, commonly operating at 3.3 V.

The most common communication protocol used between the processor and wireless interface is universal asynchronous receiver/transmitter (UART).

2.1 UART Voltage Translation

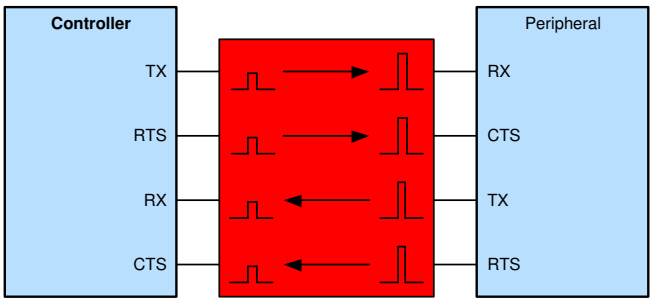

Figure 2. Using Voltage Translation With the UART 4-Wire Communication Bus

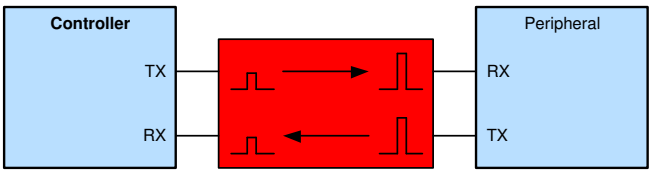

Figure 3. Using Voltage Translation With the UART 2-Wire Communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Provide protection from disconnected peripherals
- Find the right voltage level translator through the *online parametric search tool*.

3 Logic and Translation Use Cases

3.1 Logic Use Cases

3.1.1 Drive Indicator LEDs

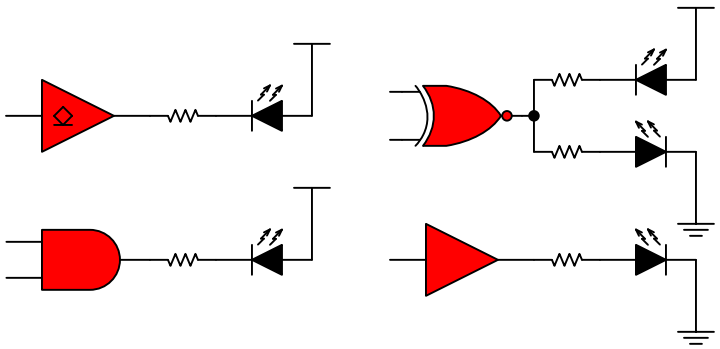

Figure 4. Using Logic as Indicator LED Driver Application Examples

- Add system indicators without controller interaction required
- Most logic gates can drive low-current indicator LEDs (1 to 25 mA)
- Logic functions add configurability
- Disable indicator LEDs as desired
- Find the right logic solutions through the *online parametric search tool*

3.1.2 Power Sequencing: Combine Power Good Signals

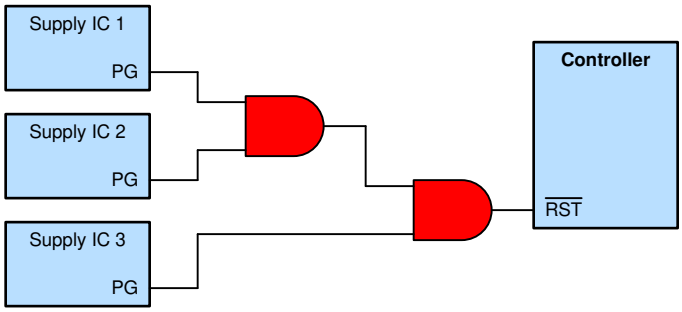

Figure 5. Using Logic to Combine Multiple Power-Good Signals

- Combine power good signals to drive an active low reset
- Add power indicator LEDs without software or system controller interaction
- See more about this use case in the *Logic Minute* video *Combining Power Good Signals*
- Find the right AND gate through the *online parametric search tool*.

3.1.3 Debounce Switches and Buttons

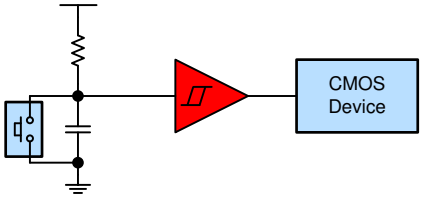

Figure 6. Using Logic to Prevent Multiple Triggers of a CMOS Input Due to Switch Bounce

- Prevents multiple triggers of CMOS inputs due to switch bounce
- Works when the system controller is asleep
- Works without a system controller
- Reduces controller code complexity, no software debounce required
- See more about this use case in the *Logic Minute* video *Debounce a Switch*
- Find the right Schmitt-trigger buffer through the *online parametric search tool*

3.1.4 Tamper Detection: Latching Alarm Circuit with Reset

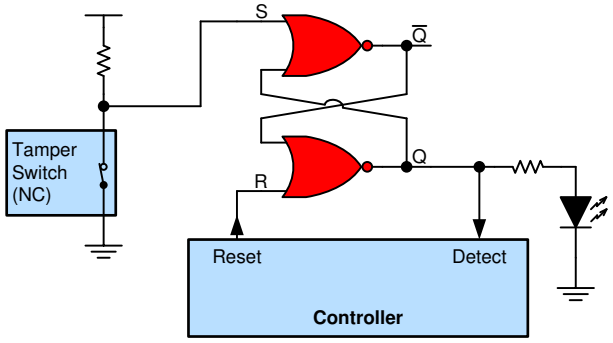

Figure 7. Using Logic to Monitor a Normally Closed (NC) Tamper Switch

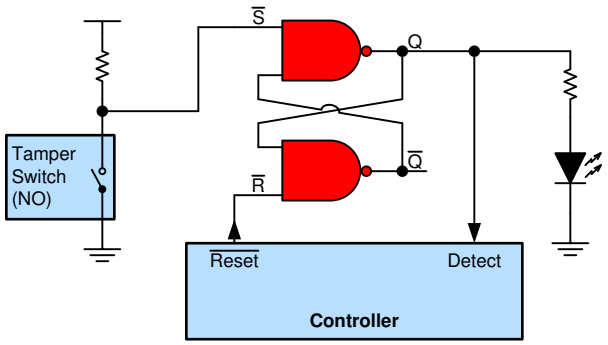

Figure 8. Using Logic to Monitor a Normally Open (NO) Tamper Switch

- Flags any tampering
- Extremely low power
- Works while the controller sleeps
- Can be used without a controller
- See more about this use case in the *Logic Minute* video *Using an S-R Latch in Alarm Circuitry*
- Find the right NOR or NAND gate through the *online parametric search tool*

3.1.5 Increase Number of Controller Inputs

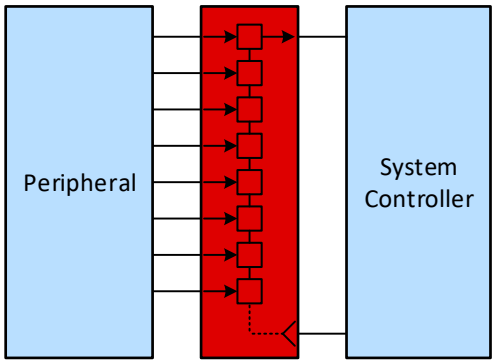

Figure 9. Using Shift-Register to Serialize Parallel Data and Conserve Controller I/O's

- Input eight bits of parallel data to the System Controller with as few as two I/Os
- Daisy chain shift registers to produce large numbers of inputs
- Input up to 180 Mbps of serial data with a parallel-in serial-out shift register
- Find the right Shift Register through the *online parametric search tool*

3.1.6 Increase Number of Controller Outputs

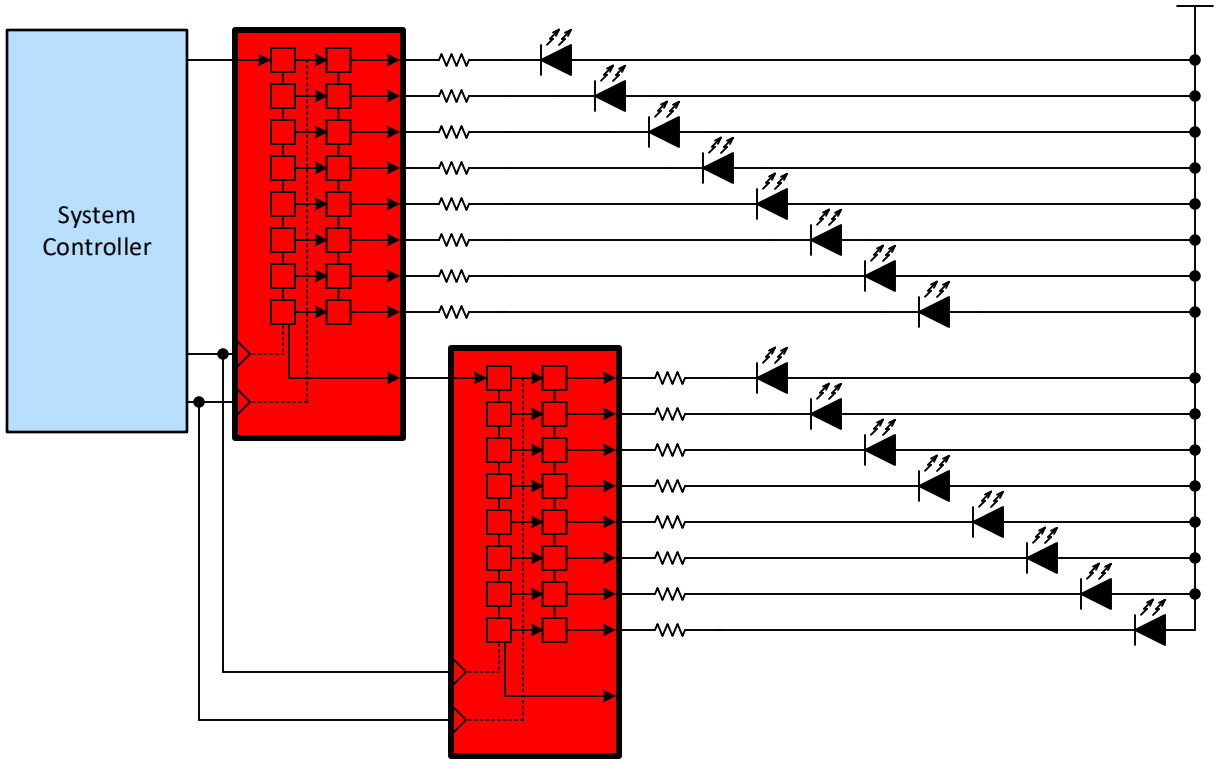

Figure 10. Using Two Shift Registers to Control 16 LEDs with Three Signals (Data, Shift Clock, and Output Register Clock)

- Turn as few as two outputs into eight outputs with one serial-in parallel-out shift register
- Daisy chain shift registers to produce large numbers of outputs
- Drive low-current (< 8 mA) LEDs directly
- Find the right Shift Register through the *online parametric search tool*

3.2 Voltage Translation Use Cases

3.2.1 GPIO Communication

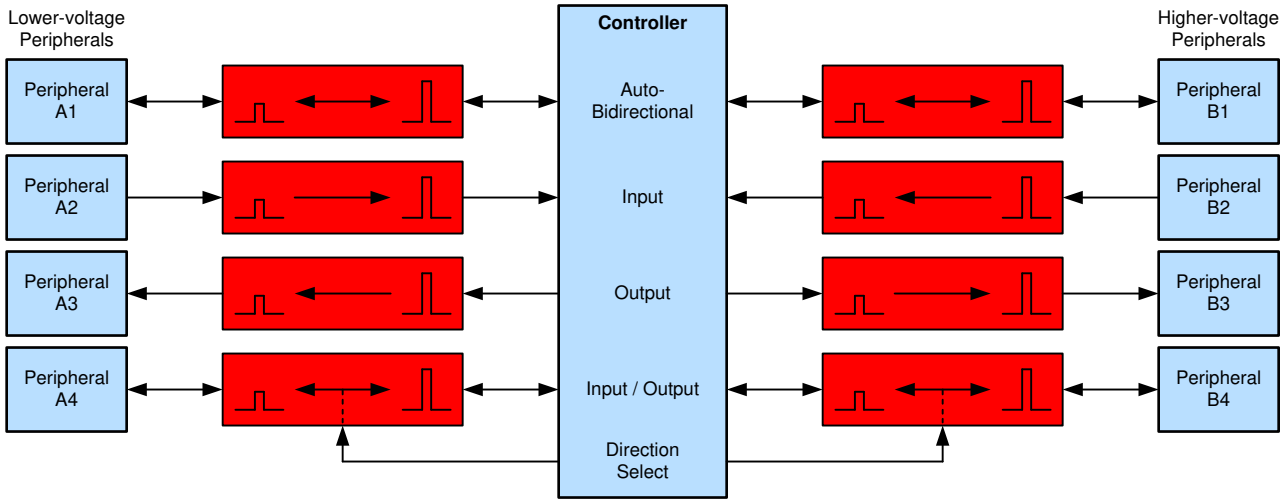

Figure 11. Using Voltage Translation With GPIO Communications

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Provides protection from disconnected peripherals
- Find the right voltage level translator through the *online parametric search tool*

4 Recommended Logic and Translation Families for Electronic Meters

4.1 AUP: Advanced Ultra-low-Power CMOS Logic and Translation

Key Features: SN74**AUPxG**xxxx

- Low static- and dynamic-power consumption
- Wide V_{CC} operating range: 0.8 to 3.6 V
- Input hysteresis allows for slow input transition rate
- Best in class for speed-power optimization
- I_{off} specification for partial power down support
- Packaging options:
  - DSBGA
  - SC70
  - SM8
  - SON
  - SOT, SOT-23
  - UQFN
  - US8
  - X2SON

Key Features: SN74**AUPxT**xxxx

- Low static- and dynamic-power consumption
- 1.65-V to 3.6-V translation range
- Best in class for speed-power optimization
- I_{off} specification for partial power down support

Find the right AUP family logic and voltage level translation devices through the *online parametric search tool*.

4.2 AXC: Advanced eXtremely Low-Voltage CMOS Translation

Key Features

- Up and down translation across 0.65 V to 3.6 V
- Designed with glitch suppression circuitry to improve power sequencing performance
- Maximum quiescent current (I_{CCA} + I_{CCB}) as low as 6 µA (85°C maximum) and 14 µA (125°C maximum)
- Up to 500-Mbps support when translating from 1.8 V to 3.3 V
- V_{CC} isolation feature – If either V_{CC} input is below 100 mV, all I/Os outputs are disabled and become high impedance
- I_{off} supports partial-power-down mode operation
- Operating temperature: –40°C to 125°C
- Packaging Options:
  - SC70
  - SM8
  - SON
  - SOT, SOT-23
  - UQFN
  - US8
  - X2SON

Find the right AXC family voltage level translation devices through the *online parametric search tool*.

4.3 LVC: Low-Voltage CMOS Logic and Translation

Key Features: SN74**LVC**xxxx

- Huge portfolio of logic functions
- LVC: 4+ channels per package
- Overvoltage tolerant inputs allow unidirectional down-translation with any function
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation.
- Packaging options:
  - SOIC
  - TSSOP
  - VQFN
  - SOP
  - SSOP

Key Features: SN74**LVCxG**xxxx

- Put one, two, or three channels of any logic function right where they are needed
- Configurable gates available ('57, '58, '97, '98, '99 functions)
- Overvoltage tolerant inputs allow unidirectional down-translation with any gate or buffer
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation
- Packaging options:
  - SOT-23
  - SC70
  - X2SON
  - SOT-5X3
  - SON
  - DSBGA

Key Features: SN74**LVCxT**xxxx

- LVCxT: Up and down translation across 1.65 V to 5.5 V
- 1, 2, 8, or 16 channels per device
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation

Find the right LVC family logic and voltage level translation devices through the *online parametric search tool*.

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