Texas Instruments

Migration From 3.3-V to 2.5-V Power Supplies for Logic Devices

Application Report

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TEXAS INSTRUMENTS

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Introduction

Powering systems at the 5-V level has been a standard practice for approximately 30 years. Power consumption is always a concern in system design and, because reducing the supply voltage yields an exponential decrease in power consumption, lower supply voltages are commonly used. Thus, a transition from the common 5-V power-supply level to the 3.3-V level is occurring. Furthermore, the next voltage level for which specified switching levels have been defined is 2.5 V. During this transition, parts of a system may be designed for a lower supply voltage while other parts may not. This raises concerns of input-voltage tolerance, interfacing or translating, and level shifting. This application report explores the possibilities for migrating to 3.3-V and 2.5-V power supplies and discusses the implications.

Customers are successfully using a wide range of low-voltage, 3.3-V logic devices. These devices are within Texas Instruments (TI™) advanced low-voltage CMOS (ALVC), crossbar technology (CBT), crossbar technology with integrated diode (CBTD), low-voltage crossbar technology (CBTLV) and low-voltage CMOS “A” revision (LVC-A) logic families. Additionally, TI plans to release a level shifter that generates valid 3.3-V and 2.5-V signals.

The transition from 5-V to 3.3-V logic began with core logic converting first to the lower power-supply level. Although memory is still primarily at the 5-V level, it is being converted to 3.3 V, and this conversion will continue. The same method of migration is expected for 3.3 V to 2.5 V, with memory logic following core logic by several years.

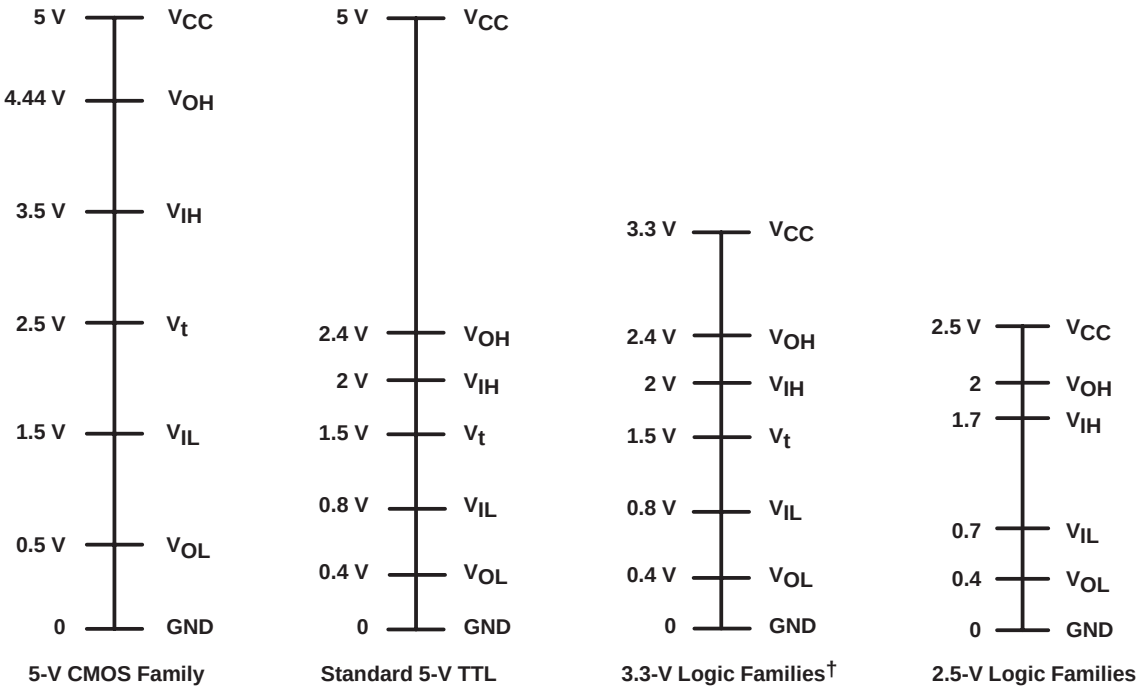
The main topics in this application report are:

- Background
- Technology
- Features and Uniqueness of Devices
- Typical Design Applications
- Laboratory Testing
- Results
- SPICE/IBIS Models
- Package Information
- Frequently Asked Questions
- Conclusion
- Glossary
- Bibliography

Background

The transition from one power-supply level to a lower one is driven primarily by a desire to reduce power consumption. For approximately the last 30 years, 5-V power supplies have been the standard for both core and memory logic. However, core logic has begun to migrate to 3.3-V power-supply levels, and memory has followed. The next commonly accepted power-supply level is 2.5 V and designers are beginning to incorporate it in their systems. This sets the stage for 1.8-V logic, for which a standard has not been established.

For each power-supply level, a standard exists for defining commonly agreed-upon levels of input and output voltages. Figure 1 shows the appropriate switching levels for 5-V, 3.3-V, and 2.5-V V_{CC} families.



† In accordance with JEDEC Standard 8-A for LV interface levels

Figure 1. Switching Levels for 5-V, 3.3-V, and 2.5-V V_{CC} Families

Technology

Table 1 lists the logic families TI produces that operate at 3.3-V V_{CC}. The process, the power-supply level for which the device was designed and optimized, and whether the device can operate at 3.3-V and 2.5-V V_{CC} levels are included.

Table 1. Logic Family Technology Summary

LOGIC FAMILY	PROCESS	OPTIMIZED POWER SUPPLY LEVEL	OPERATIONAL AT V_{CC} = 3.3 V	OPERATIONAL AT V_{CC} = 2.5 V
AHC	CMOS	5 V	Yes	Yes
ALVC	CMOS	3.3 V	Yes	Yes
CBT	CMOS†	5 V	Yes	Yes
CBTD	CMOS	5 V	Yes	Yes
CBTLV	CMOS	3.3 V	Yes	Yes
LVC-A	CMOS	3.3 V	Yes	Yes

† The CBT16232, CBT16233, and CBT16390 devices are BiCMOS.

In Table 1, CMOS process indicates that the devices contain solely CMOS circuitry. The BiCMOS process indicates that a combination of bipolar and CMOS transistors may be implemented in the circuitry.

Features and Uniqueness of Devices

When discussing interactions between different power-supply levels, the distinction between input-voltage tolerance, interfacing or translating, and level shifting is important. Input-voltage tolerance applies when a device with a lower power supply can withstand the presence of a higher voltage without being damaged. For example, a 3.3-V device drives a 2.5-V device without harming the receiver. Under this concept, there is no implication about the device being able to produce a signal compatible with the higher power-supply level. Interfacing or translating implies that a device can generate valid input and output voltage levels, even though a single power-supply level is being used. A device is a level shifter when it implements two power supplies and can produce signals that conform to the switching requirements of both the lower-voltage power supply and the higher-voltage power supply.

All devices in the families listed in Table 1 operate and function correctly when powered at 3.3-V and 2.5-V V_{CC}. The following paragraphs address how the devices interact when they are operated at one power-supply level and are exposed to signals from a device operated at a different power-supply level.

Figure 1 illustrates that a 3.3-V device can adequately drive a 2.5-V device. $V_{OL(3.3\text{-V logic})}$ (0.4 V) is less than $V_{IL(2.5\text{-V logic})}$ (0.7 V), which allows a 300-mV noise margin. Similarly, $V_{OH(3.3\text{-V logic})}$ (2.4 V) is greater than $V_{IH(2.5\text{-V logic})}$ (1.7 V), which allows for a 700-mV noise margin. Table 2 summarizes the compatibility between 3.3-V and 2.5-V devices when both are powered at 3.3-V V_{CC}.

Table 2. 3.3-V to 2.5-V Compatibility When V_{CC} = 3.3 V

LOGIC FAMILY	2.5-V TOLERANT	2.5-V SWITCHING LEVELS GENERATED
AHC	Yes	Yes
ALVC	Yes	Yes
CBT†	Yes	Yes
CBTD†	Yes	Yes
CBTLV†	Yes	Yes
LVC-A	Yes	Yes

† CBT, CBTD, and CBTLV families are limited by the input voltage.

A 2.5-V device cannot adequately drive a 3.3-V device. $V_{OL(2.5\text{-V logic})}$ (0.4 V) is less than $V_{IL(3.3\text{-V logic})}$ (0.8 V), which allows a 400-mV noise margin. However, $V_{OH(2.5\text{-V logic})}$ (2 V) is approximately equal to $V_{IH(3.3\text{-V logic})}$ (2 V), which theoretically allows no noise margin. Therefore, 2.5-V devices should not be used to drive 3.3-V devices. Table 3 summarizes the compatibility between 2.5-V and 3.3-V devices when both are powered at 2.5-V V_{CC}.

Table 3. 2.5-V to 3.3-V Compatibility When V_{CC} = 2.5 V

LOGIC FAMILY	3.3-V TOLERANT	3.3-V SWITCHING LEVELS GENERATED
AHC	Yes	No
ALVC	No	No
CBT	Yes	No
CBTD	Yes	No
CBTLV	Yes	No
LVC-A	Yes	No

Typical Design Applications

When migrating from 5-V power supplies to 3.3-V power supplies, migration from 3.3 V to 2.5 V is expected to occur in stages. Specifically, core logic will make the transition to 2.5 V, while memory and I/Os probably will lag. The configuration in Figure 2 likely will be commonplace.

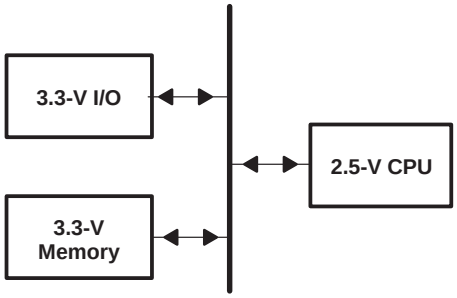


Figure 2. Typical Anticipated 3.3-V/2.5-V Architecture

The CPU operates at 2.5-V V_{CC} and must communicate with a 3.3-V V_{CC} memory and I/O. For all unidirectional data flow from the memory and I/O to the CPU, e.g., reading from memory and receiving input from the I/O, any device that is powered at 3.3-V V_{CC} is acceptable. However, for all communication and data transfer from the CPU to memory or the I/O, such as address buffering and printing, only a device with level-shifting capabilities that can generate true 3.3-V signals from a 2.5-V input should be used.

Laboratory Testing

To demonstrate the ability of TI devices to operate at both 3.3-V and 2.5-V V_{CC} levels, several devices were tested to determine typical propagation delay times. Because typical values were desired, V_{CC} was set to 3.3 V and 2.5 V, and the ambient temperature was 25°C. Tables 4 and 5 show the conditions under which the measurements were taken and the results obtained.

Results

Data in Tables 4 and 5 show that under the same conditions a device's propagation delay increases as V_{CC} is reduced and decreases as the capacitive load is decreased.

Table 4. Typical Propagation Delays When V_{CC} = 3.3 V

LOGIC FAMILY	DIRECTION	CAPACITIVE LOAD (pF)	t_{pd} OR t_{PLH}/t_{PHL} (TYPICAL)
AHC245	A <—> B	30	4.3/3.7 ns
		50	4.6/3.9 ns
AHC16245	A <—> B	30	4.3/3.7 ns
		50	6.8/5.6 ns
ALVC16245	A to B	30	1.4/1.7 ns
		50	1.8/2.2 ns
CBT	A <—> B	50	750 ps
CBTD	A <—> B	50	750 ps
CBTLV3245	A <—> B	50	600 ps
LVCH245A	A <—> B	50	2.7/3.1 ns
LVCH16245A	A to B	30	2.1/2.2 ns
		50	2.8/2.5 ns

Table 5. Typical Propagation Delays When V_{CC} = 2.5 V

LOGIC FAMILY	DIRECTION	CAPACITIVE LOAD (pF)	t_{pd} OR t_{PLH}/t_{PHL} (TYPICAL)
AHC245	A <—> B	30	5.6/4.6 ns
		50	6/5 ns
AHC16245	A <—> B	30	5.6/4.5 ns
		50	9.4/7.2 ns
ALVCH16245	A to B	30	2.4/2.5 ns
		50	3.6/2.8 ns
CBT	A <—> B	50	900 ps
CBTD	A <—> B	50	900 ps
CBTLV3245	A <—> B	30	500 ps
		50	700 ps
LVCH245A	A to B	50	3.1/3.6 ns
	B to A		3.1/3.5 ns
LVCH16245A	A to B	30	2.8/2.7 ns
		50	4.1/3.1 ns

SPICE/IBIS Models

SPICE and IBIS models are available for certain devices. Appendix A lists SPICE and IBIS models for given functions within a logic family.

The SPICE model is a level-13 model that consists of the input and output stages and can be obtained by contacting your local TI Sales Representative. The IBIS model consists of the input and output stages and can be obtained at the TI web site http://www.ti.com/sc/docs/asl/models/ibis.htm.

Package Information

The devices discussed in this application report are available in a variety of packages, including plastic dual-in-line package (PDIP), quarter-size outline package (QSOP), small-outline integrated circuit (SOIC), small-outline transistor (SOT), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP). TI's Logic Selection Guide, literature number SDYU001, lists devices and packages in which they are available.

Frequently Asked Questions

Question: How do I reconcile differences between the 3.3-V part of my system and the 2.5-V part?

Answer: When designing with multiple power-supply levels in a single system, ensure that the devices that are powered with the lower-voltage power supply are not damaged when interfacing with the part of the system that is powered by the higher-voltage power supply. This is accomplished by ensuring that all devices are voltage tolerant of the other devices. For the purposes of this application report, any 2.5-V device must be 3.3-V tolerant to ensure that no damage occurs to the 2.5-V device.

Question: With the CBT logic family, I could interface the 5-V part of my system with the 3.3-V part of my system by adding a diode between the external V_{CC} and the output-enable terminals. Can I use a similar method with the CBTLV family to interface between the 3.3-V part and 2.5-V part of my system?

Answer: To drive the CBTLV output levels fully to the rail, a PMOS transistor was added to the circuitry. This PMOS and its associated circuitry prevent the CBTLV family of devices from level translating between 3.3 V and 2.5 V. However, the CBT family is capable of performing this function. Please see item 1 in the bibliography.

Question: How do I get a copy of the SPICE and IBIS models?

Answer: The SPICE models can be obtained by contacting your local TI Sales Representative. The IBIS models can be obtained at http://www.ti.com/sc/docs/asl/models/ibis.htm.

Conclusion

As systems migrate from 3.3-V to 2.5-V power supplies, issues of input-voltage tolerance, interfacing or translating, and level shifting must be addressed. A 3.3-V device can drive a 2.5-V device, but a 2.5-V device cannot drive a 3.3-V device due to switching-level incompatabilities. TI offers a variety of logic families that are capable of operating at 3.3-V and 2.5-V V_{CC} levels.

Glossary

AHC	Advanced High-Speed CMOS
ALVC	Advanced Low-Voltage CMOS
CBT	Crossbar Technology
CBTLV	Low-Voltage Crossbar Technology
CPU	Central Processing Unit
IBIS	I/O Buffer Information Specification
I/O	Input/Output
LVC-A	Low-Voltage CMOS “A” Revision
LVTTL	Low-Voltage Transistor-Transistor Logic
PDIP	Plastic Dual-In-line Package
QSOP	Quarter-Size Outline Package
SOIC	Small-Outline Integrated Circuit
SOT	Small-Outline Transistor
SPICE	Simulation Program With Integrated-Circuit Emphasis
SSOP	Shrink Small-Outline Package
TI	Texas Instruments
TSSOP	Thin Shrink Small-Outline Package
TVSOP	Thin Very Small-Outline Package

Bibliography

1. 3.3-V to 2.5-V Translation with Texas Instruments Crossbar Technology, literature number SCDA004
2. Advanced Bus Interface SPICE I/O Models, 1995, literature number SCBD004A
3. AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book, 1996, literature number SCLD004
4. CBT Bus Switches, Crossbar Technology Data Book, 1996, literature number SCDD001A
5. Logic Selection Guide, literature number SDYU001 (revised quarterly)
6. Low-Voltage CMOS Logic Data Book, 1997, literature number SCBD152
7. Low-Voltage Logic Data Book, 1996, literature number SCBD003B
8. Semiconductor Group Package Outlines Reference Guide, literature number SSYU001

Appendix A

Available SPICE and IBIS Models

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’00	S	NA	NA	S/I
’02	S	NA	NA	S/I
’04	S	NA	NA	S/I
’08	S	NA	NA	S/I
’10	NA	NA	NA	S/I
’14	S	NA	NA	S/I
’32	——	NA	NA	S/I
’74	——	NA	NA	S/I
’86	——	NA	NA	S/I
’112	NA	NA	NA	S/I
’125	S	NA	NA	S/I
’126	S	NA	NA	S
’137	NA	NA	NA	S/I
’138	——	NA	NA	S/I
’139	——	NA	NA	S
’157	——	NA	NA	S/I
’158	NA	NA	NA	S
’240	——	NA	NA	S
’241	NA	NA	NA	S
’244	——	NA	NA	S/I
’245	——	NA	NA	S
’257	NA	NA	NA	S/I
’258	NA	NA	NA	S
’373	——	NA	NA	S
’374	——	NA	NA	S/I
’540	——	NA	NA	S
’541	——	NA	NA	S
’543	NA	NA	NA	S/I
’544	NA	NA	NA	S
’573	——	NA	NA	S
’574	——	NA	NA	S
’646	NA	NA	NA	S/I
’652	NA	NA	NA	S/I
’821	NA	NA	NA	S
’823	NA	NA	NA	S
’827	NA	NA	NA	S
’828	NA	NA	NA	S

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’841	NA	NA	NA	S
’843	NA	NA	NA	S
’861	NA	NA	NA	S
’863	NA	NA	NA	S
’2952	NA	NA	NA	S/I
’16233	NA	NA	S	NA
’16240	——	S	NA	S/I
’162240	NA	S	NA	NA
’16241	NA	NA	NA	S
’16244	——	S/I	NA	S/I
’162244	NA	S/I	NA	S/I
’16245	——	S/I	NA	S/I
’162245	NA	S	NA	——
’16260	NA	S	NA	NA
’162260	NA	S	NA	NA
’162268	NA	S	NA	NA
’16269	NA	S	NA	NA
’162269	NA	——	NA	NA
’16270	NA	S	NA	NA
’16271	NA	S	NA	NA
’16272	NA	S	NA	NA
’16280	NA	S	NA	NA
’162280	NA	——	NA	NA
’16282	NA	S	NA	NA
’162282	NA	——	NA	NA
’16334	NA	S/I	NA	NA
’162334	NA	S/I	NA	NA
’16344	NA	S	NA	NA
’162344	NA	S	NA	NA
’16373	——	S	NA	S/I
’162373	NA	S	NA	NA
’16374	——	S/I	NA	S/I
’162374	NA	S	NA	NA
’16409	NA	S	NA	NA
’162409	NA	——	NA	NA
’16500	NA	S	NA	NA
’16501	NA	S	NA	NA

† S = SPICE model exists; I = IBIS model exists; NA = Not applicable, indicating that the device does not exist for that particular family; —— = neither SPICE nor IBIS model exists.

Available SPICE and IBIS Models (Continued)

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’16524	NA	——	NA	NA
’16525	NA	——	NA	NA
’16540	——	S	NA	S/I
’162540	NA	S	NA	NA
’16541	——	S	NA	S/I
’162541	NA	S	NA	NA
’16543	NA	S	NA	S/I
’16600	NA	S	NA	NA
’16601	NA	S	NA	NA
’162601	NA	S/I	NA	NA
’16646	NA	S	NA	S/I
’16652	NA	S	NA	S/I
’16721	NA	S/I	NA	NA
’162721	NA	S/I	NA	NA
’16820	NA	S	NA	NA
’162820	NA	S/I	NA	NA
’16821	NA	S/I	NA	NA
’16823	NA	S/I	NA	NA
’16825	NA	S	NA	NA

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’16827	NA	S/I	NA	NA
’162827	NA	S/I	NA	NA
’16828	NA	S	NA	NA
’16830	NA	S/I	NA	NA
’162830	NA	——	NA	NA
’16831	NA	——	NA	NA
’162831	NA	——	NA	NA
’16832	NA	——	NA	NA
’162832	NA	——	NA	NA
’16835	NA	S/I	NA	NA
’162835	NA	S/I	NA	NA
’16836	NA	S/I	NA	NA
’162836	NA	S/I	NA	NA
’16841	NA	S	NA	NA
’162841	NA	——	NA	NA
’16843	NA	S	NA	NA
’16863	NA	——	NA	NA
’16901	NA	S	NA	NA
’16952	NA	S	NA	S/I

† S = SPICE model exists; I = IBIS model exists; NA = Not applicable, indicating that the device does not exist for that particular family; —— = neither SPICE nor IBIS model exists.