Application Report
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CDCE62005 Phase Noise Performance and Jitter Cleaning Ability

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ABSTRACT

This application report presents phase noise data taken on the Texas Instruments' CDCE62005 jitter cleaner and synchronizer PLL. The phase noise performance of the CDCE62005 depends both on the phase noise of the reference clock and the CDCE62005 itself. This application report shows the phase noise performance at the most popular CDMA frequencies and helps the user to choose the right clocking solution for their particular applications. These test results confirm that the CDCE62005 can provide clocks better than –145dBc/Hz phase noise at 10-MHz offset from the carrier frequency. Low phase noise is a requirement for wireless applications as well as many other high-performance sampling systems. The report also reviews the open-loop VCO performance of the CDCE62005 device.

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1 Introduction

The CDCE62005 is a low phase noise, low jitter clock synthesizer and jitter cleaner with programmable outputs and inputs. It features a phase-locked loop (PLL) architecture with an on-chip voltage-controlled oscillator (VCO) and internal loop filter. An optional external low-pass loop filter is required to complete the PLL. Proper selection of the VCO frequency and loop bandwidth are critical to achieve the best performance from the CDCE62005.

This report includes phase noise plots of many of the most common frequencies used in wireless base station applications. In addition, the phase noise of the open loop VCO of the CDCE62005 is included for completeness. The phase noise of the 30.72-MHz reference and output phase noise of the CDCE62005 at various frequencies are also included. The RMS jitter was calculated from the phase noise plots measured over a 10-kHz to 20-MHz range using the Agilent E5052A™ phase noise analyzer.

1.1 Definitions

Timing budget— Defined by dynamic (jitter) and static errors (skew). Depending on the system architecture, only a subset of parameters from the datasheet affects the timing budget. Jitter is a timing distribution of the clock signal that expresses the edge deviation from the ideal occurrence. Jitter is composed of both deterministic and random (Gaussian) content.

Jitter— Any edge deviation from the ideal occurrence. The causes of jitter include: power-supply noise, thermal and mechanical noise from the input signal and other external sources, reflection, electromagnetic interference (EMI), and other random noise. Suggestions to reduce jitter include: power-supply bypassing (10 μF to 47 μF) to prevent voltage droop and ripple because of current surges; filtering each VCC pin (with a 0.1-μF, low effective series resistance [ESR] capacitor); using proper termination to remove reflections; using differential signaling as opposed to single-ended signaling; and minimizing noise coupling by isolating other high-frequency signals from the clock driver.

Phase noise— The short-term instability caused by frequency variation (phase) of a signal referenced to the carrier level and a function of the carrier offset (that is, relative noise level within a 1-Hz bandwidth). Integration of phase noise (PN) over a given frequency band yields phase jitter RMS.

Phase jitter— Phase jitter, or accumulated jitter, is the absolute deviation of a clock edge from its ideal position in timing. While period jitter only accounts for the variation between clock periods, phase jitter accumulates the error of each period and is therefore always larger. The wider the recording time window, the more frequency bandwidth becomes integrated into the total phase jitter. Phase jitter can also be measured by integrating phase noise over the frequency band of interest. Either way, the system designer must specify the minimum and maximum frequency for the integration.

For setup and hold time budget calculations, the peak-to-peak (PP) value of the phase jitter is important. Note that only the added phase noise by the clock driver is of interest to find the worst edge position between the master clock in the system and the subsystem. The absolute phase jitter of the master clock itself adds to all clock signals in the system, thus canceling its effect.

Period jitter— The deviation in cycle time of a signal with respect to an ideal period over a random sample of cycles. Period jitter is important because it includes the maximum and minimum frequencies, and it specifies the shortest clock period. It is important for the setup and hold time budgets. Calculations with period jitter are sufficient for subsystems that use clock and data signals derived from the same clock source. Period jitter can be measured with any oscilloscope.

Peak-to-peak period jitter— The total jitter range from minimum to maximum values of a clock signal. Peak-to-peak (PP) jitter increases indefinitely with recording time. Thus, PP jitter values are only meaningful if either the recording length or the relative bit error rate is known.

RMS period jitter— One standard deviation (1 σ) of the peak-to-peak jitter of a clock signal. RMS jitter is only valid for Gaussian (that is, normal) distribution. RMS jitter is independent of the sampling window, and therefore more suitable for comparing the performance of two or more devices where the sampling time window differs or is unknown.

Cycle-to-cycle period jitter— Also known as adjacent cycle jitter; the variation in cycle time of a signal between consecutive cycles over a random sample of successive cycle pairs. Cycle-to-cycle jitter is also a good value to calculate the setup and hold time budgets because it defines the minimum and maximum variations of the timing variation from ideal for the next clock edge.

Crosstalk— This characteristic is used to measure parasitic coupling between signals, and is the effect of capacitive coupling that causes a logic transition. Capacitive coupling is the transfer of energy between nearby switching integrated circuits. The coupling depends on factors such as the distance between the traces, the signal swing, the operating frequency, and the permissiveness of the silicon dioxide. Coupling can be improved by physically increasing the distance between traces. Power and ground planes also act as shields to minimize crosstalk.

2 Test Equipment and Setup

All measurements presented in this report were taken at a 3.3-V nominal power supply, room temperature, and PLL lock condition. The power supply was provided by a HP6624A™; a reference input of 30.72-MHz LVCMOS is provided by an HP8133 signal generator. Phase noise was measured using the Agilent E5052A signal source analyzer. The test setup shown in Figure 1 was used for all phase noise testing. Output dividers were set to /1, /2, /4, and /8 for overall phase noise measurements. An output divider of /4 was used for jitter cleaner tests where the 30.72-MHz LVCMOS input was fed into a NoiseCom noise generator box to increase the noise floor, and thus raise the input jitter. The RMS jitter was calculated from the phase noise plots measured over a 10-kHz to 20-MHz range. A loop filter bandwidth of 400 kHz was used for the total jitter tests, and a loop filter bandwidth of 100 Hz was used for the jitter cleaner tests. The filter topology of the former is shown in Figure 2; the filter topology of the latter is shown in Figure 3. For clean reference inputs (less than 1 ps, RMS jitter), large loop filter bandwidths were preferred; for dirty reference inputs (greater than 1ps, RMS jitter), smaller loop filter bandwidths were preferred. All HS-LVPECL outputs were properly terminated and tested for jitter.

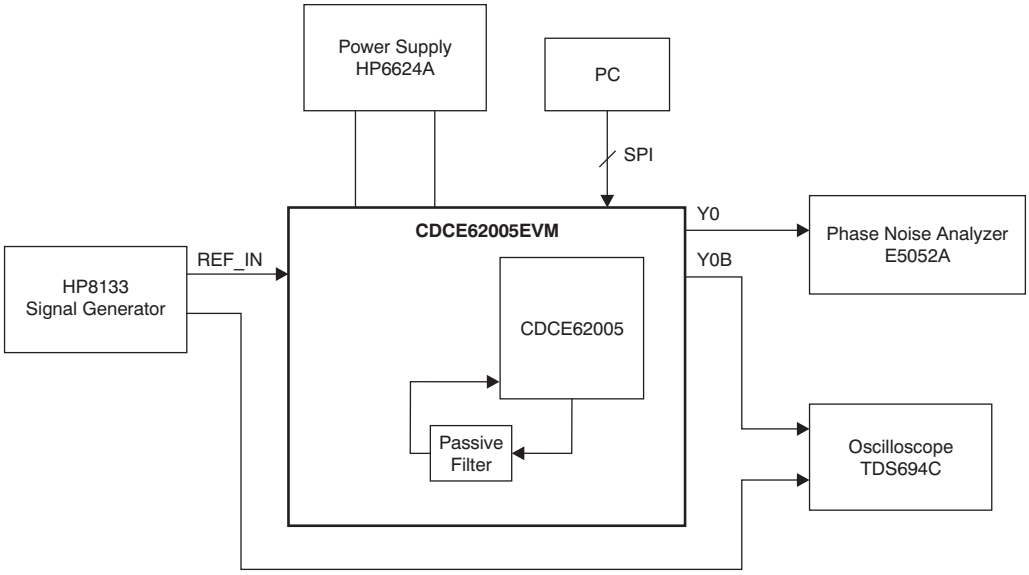


Figure 1. Phase Noise Measurement Test Setup

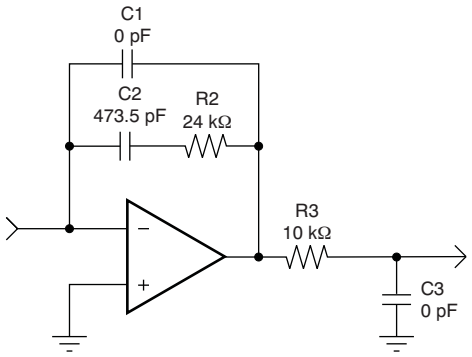
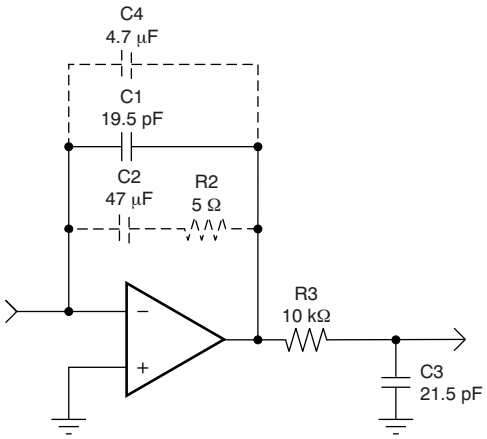


Figure 2. On-Chip Loop Filter Circuit for 400-kHz Loop Bandwidth



Note: Components shown with a dashed line are off-chip.

Figure 3. Partial On-Chip Loop Filter Circuit for 100-Hz Loop Bandwidth

3 Total Phase Noise Measurements

Section 3.1 shows a summary of total phase noise/jitter measurements on the CDCE62005 with the on-chip VCO set at 1966.08 MHz, a prescaler divider of 4, a feedback divider of 16, and for /1, /2, /4, and /8 output divider configurations for an HS-LVPECL output type. Section 3.2 shows the measurement results at different output frequencies and output types.

3.1 Phase Noise Measurement Summary

Table 1 summarizes the CDCE62005 total jitter measurements for several frequencies.

Table 1. CDCE62005 Total Jitter Summary

FREQUENCY (MHz)	OUTPUT TYPE	PHASE JITTER (fs, RMS) 10 kHz to 20 MHz
491.52	HS-LVPECL	401
245.76	HS-LVPECL	436
122.88	HS-LVPECL	479
61.44	HS-LVPECL	509

3.2 Phase Noise Measurement Results

Figure 4 through Figure 6 illustrate the phase noise measurement results for a range of output frequencies.

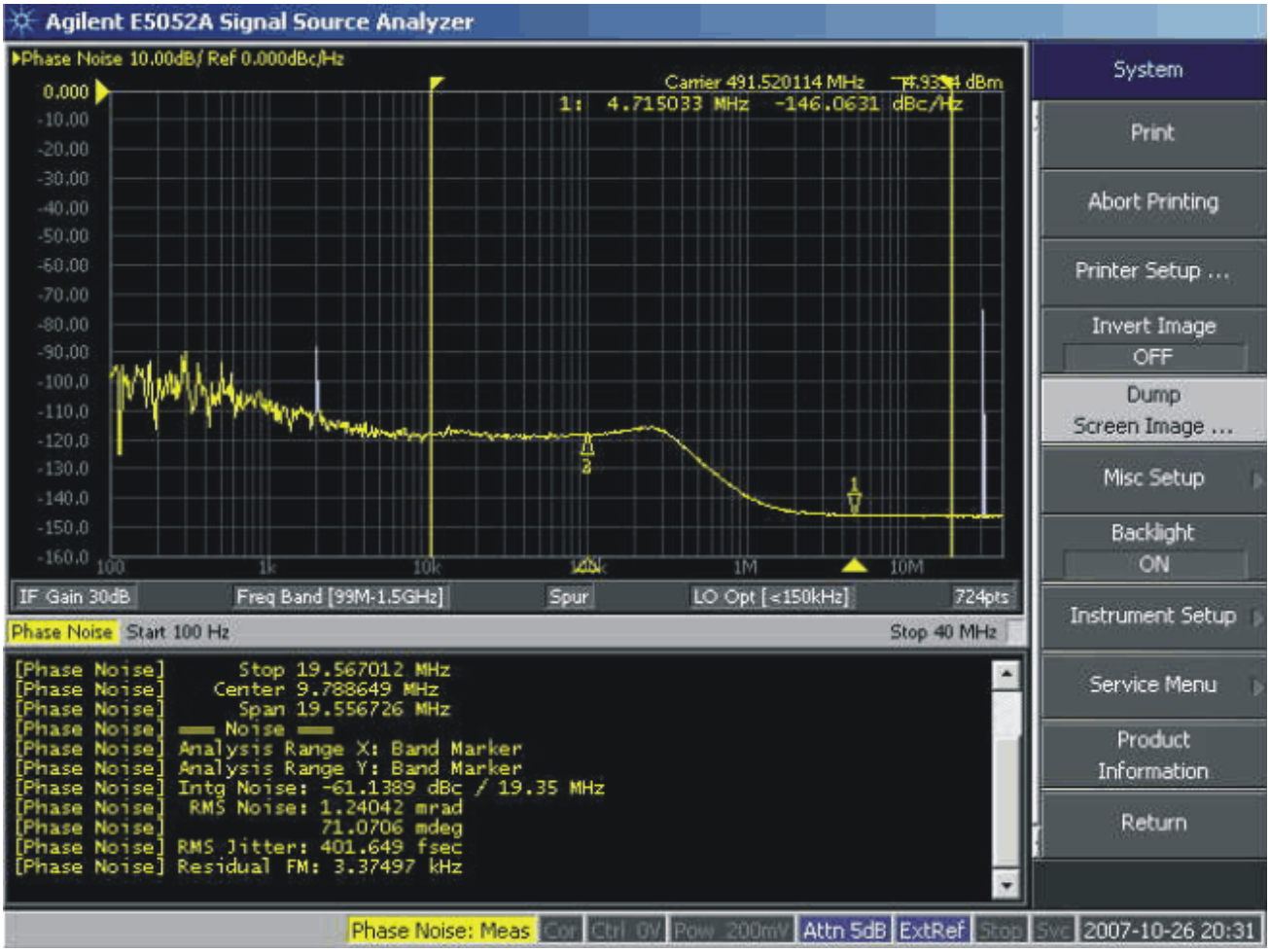


Figure 4. 491.52-MHz HS-LVPECL Output Phase Noise

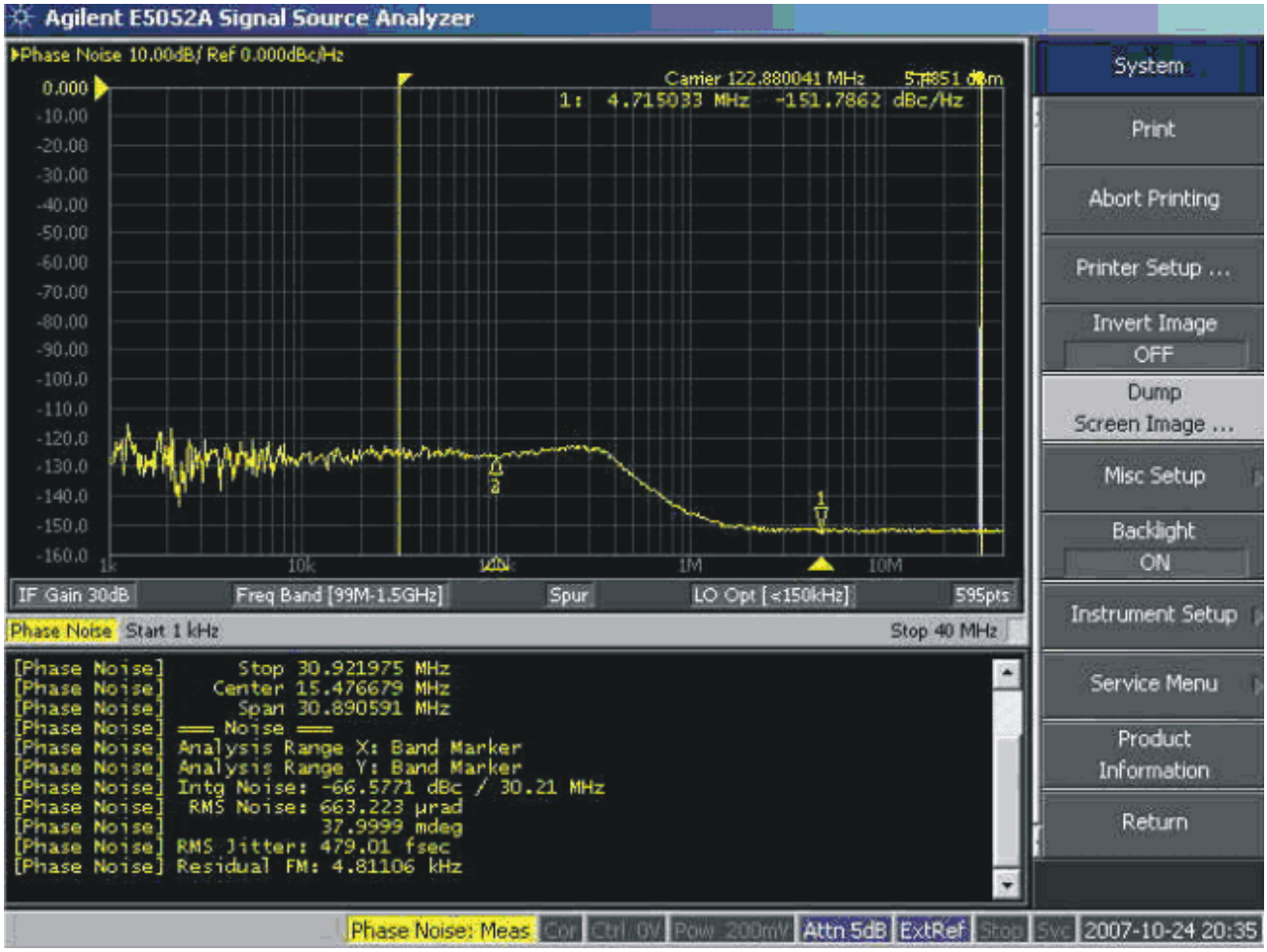


Figure 5. 122.88-MHz HS-LVPECL Output Phase Noise

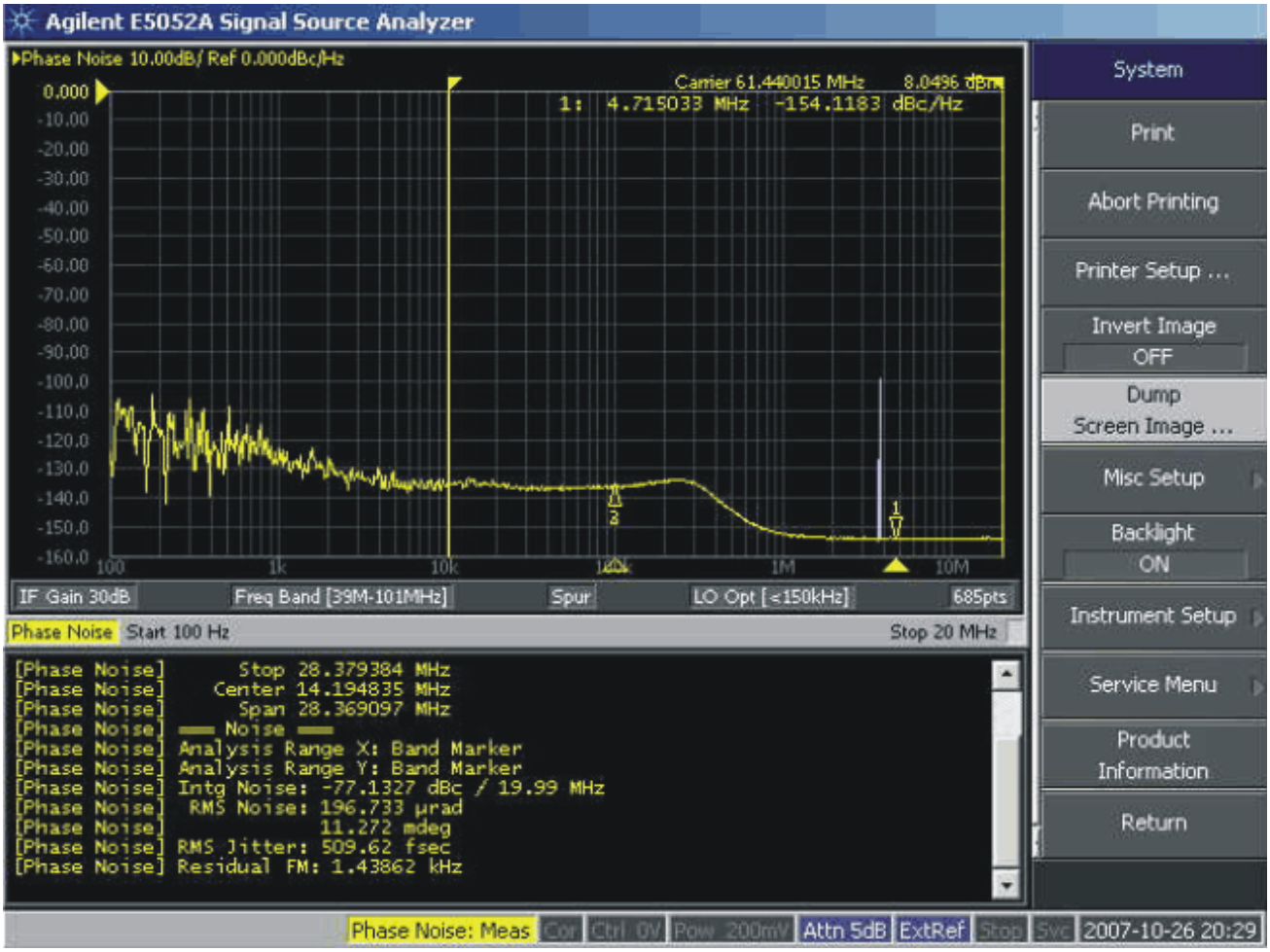


Figure 6. 61.44-MHz HS-LVPECL Output Phase Noise

4 Jitter Cleaner Measurements

Section 4.1 shows a summary of jitter cleaning ability of the CDCE62005 with a 122.88-MHz output frequency and HS-LVPECL output type. The input is a 30.72-MHz LVCMOS with varying phase jitter characteristics. Section 4.2 shows the measurement results for jitter cleaning ability for 50ps, RMS input jitter.

4.1 Jitter Cleaner Measurement Summary

The jitter cleaning ability of the CDCE62005 is shown in Table 2. Figure 7 illustrates the device input jitter versus output jitter cleaning ability.

Table 2. CDCE62005 Jitter Cleaning Ability Summary

IN PHASE JITTER (ps, RMS) 1 kHz to 5 MHz	OUTPUT TYPE	OUT PHASE JITTER (fs, RMS) 10 kHz to 20 MHz
1	HS-LVPECL	479
5	HS-LVPECL	544
10	HS-LVPECL	603
25	HS-LVPECL	658
50	HS-LVPECL	713

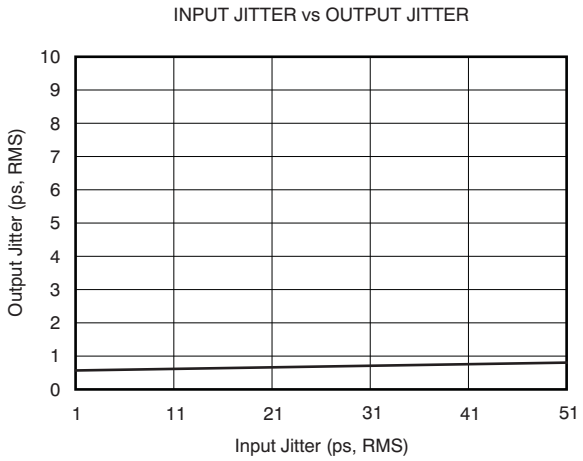


Figure 7. 122.88-MHz HS-LVPECL Output Jitter Cleaning Ability

4.2 Jitter Cleaner Measurement Results

Figure 8 and Figure 9 show the jitter cleaning performance results for 30.72-MHz LVCMOS input phase noise and 122.88-MHz HS-LVPECL output phase noise, respectively.

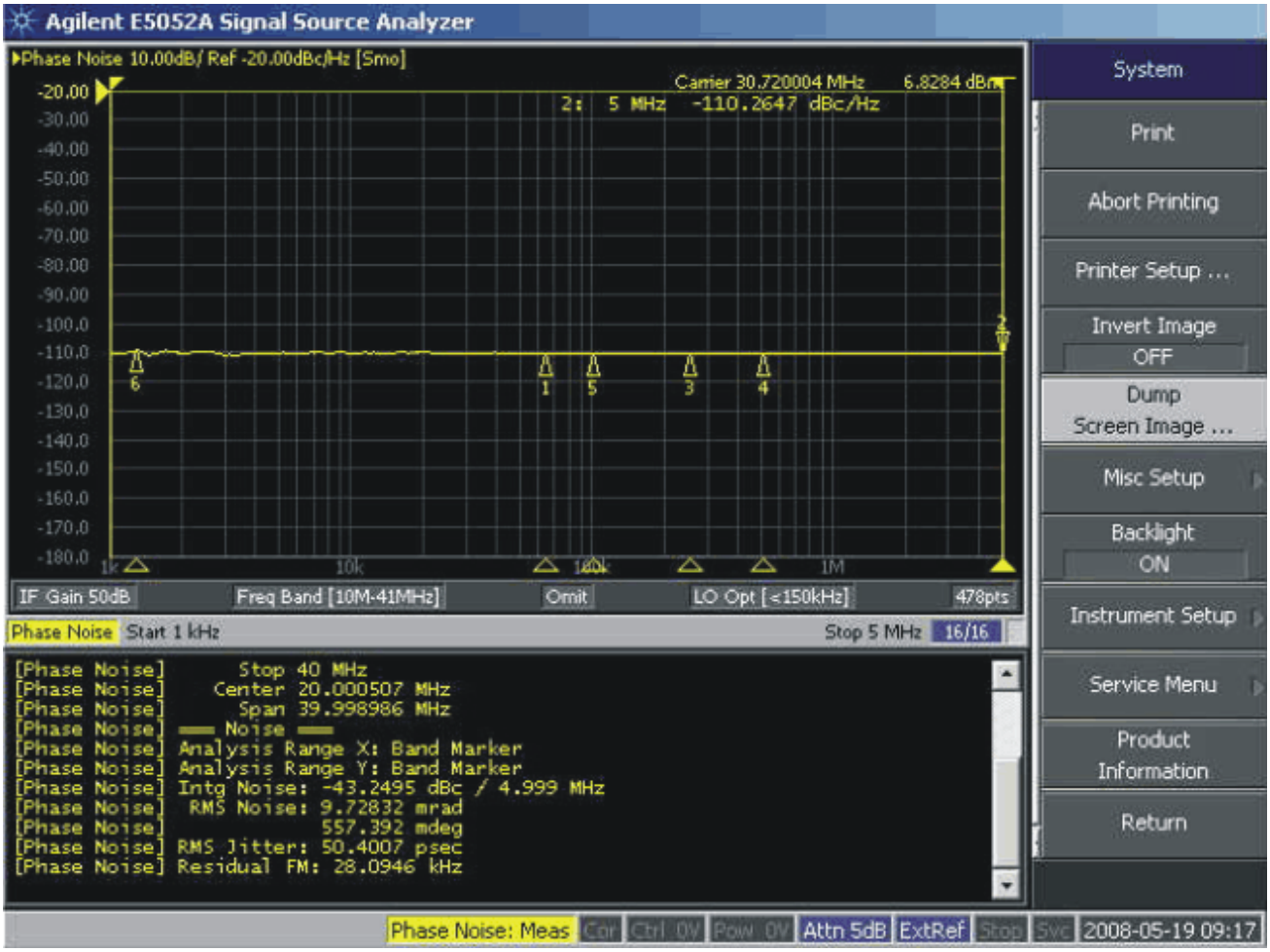


Figure 8. 30.72-MHz LVCMOS Input Phase Noise Profile (50 ps, RMS)

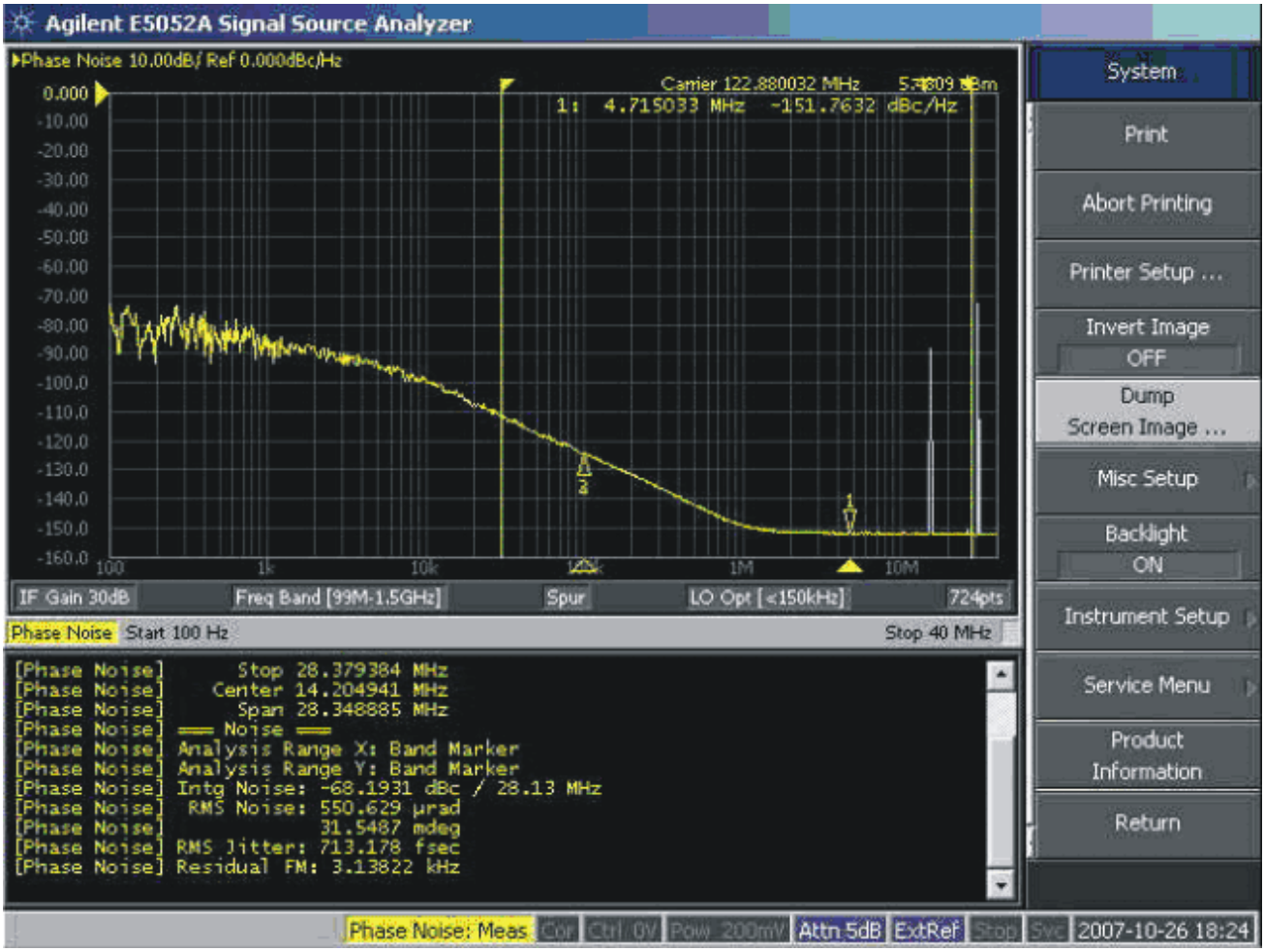


Figure 9. 122.88-MHz HS-LVPECL Output Phase Noise Profile (50 ps, RMS Input)

5 On-Chip Open-Loop VCO Phase Noise Measurements

Section 5.1 shows the measurement results of the open-loop VCO performance of both the on-chip VCOs present in the CDCE62005 under different test conditions.

5.1 Phase Noise Measurement Results

Figure 10 and Figure 11 show the open-loop phase npise measurements for the two VCOs with a prescaler divider of 3 and an output divider of 1.

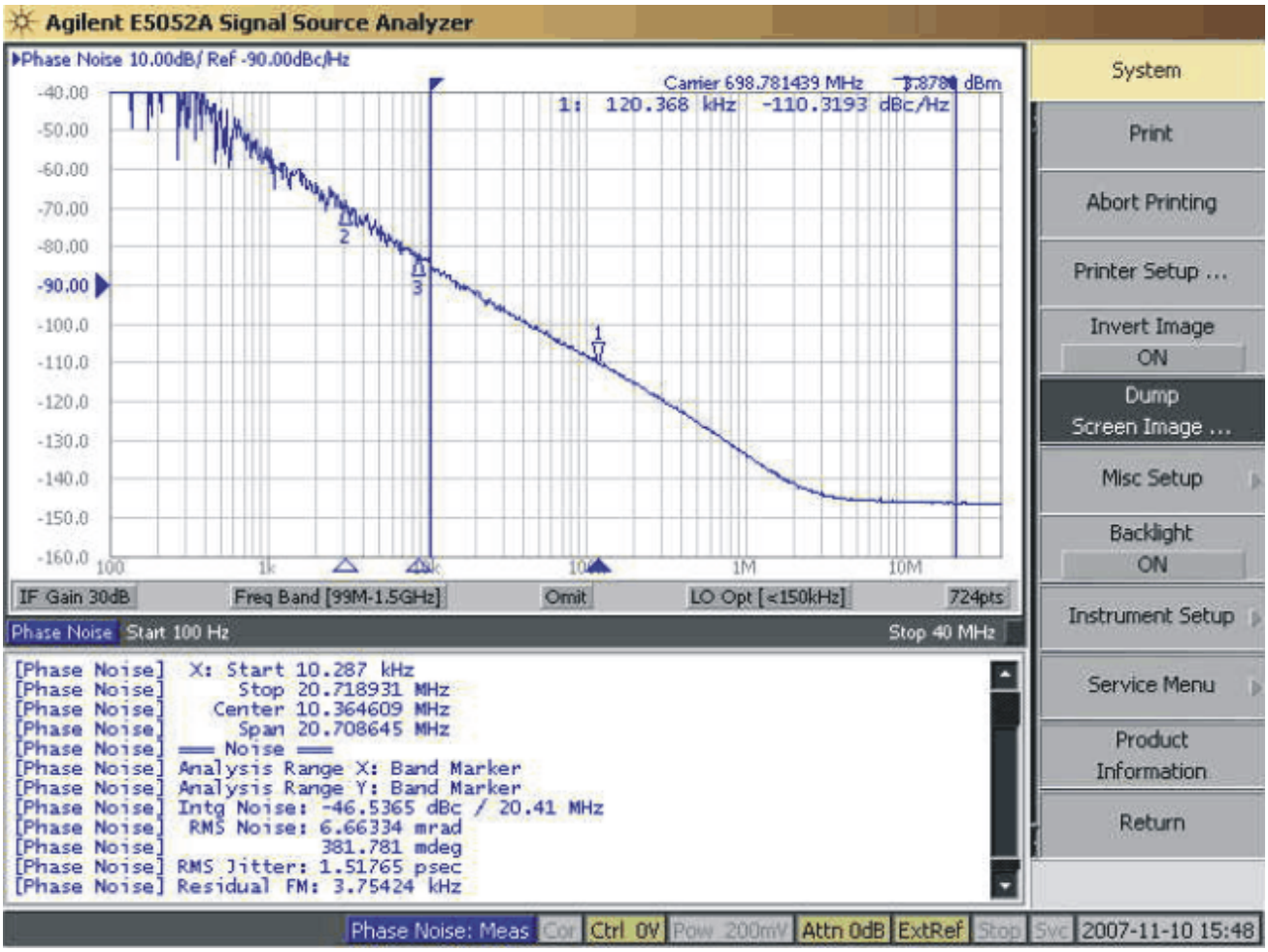


Figure 10. Open-Loop Phase Noise of On-Chip VCO1 (Prescaler Divider 3, Output Divider 1)

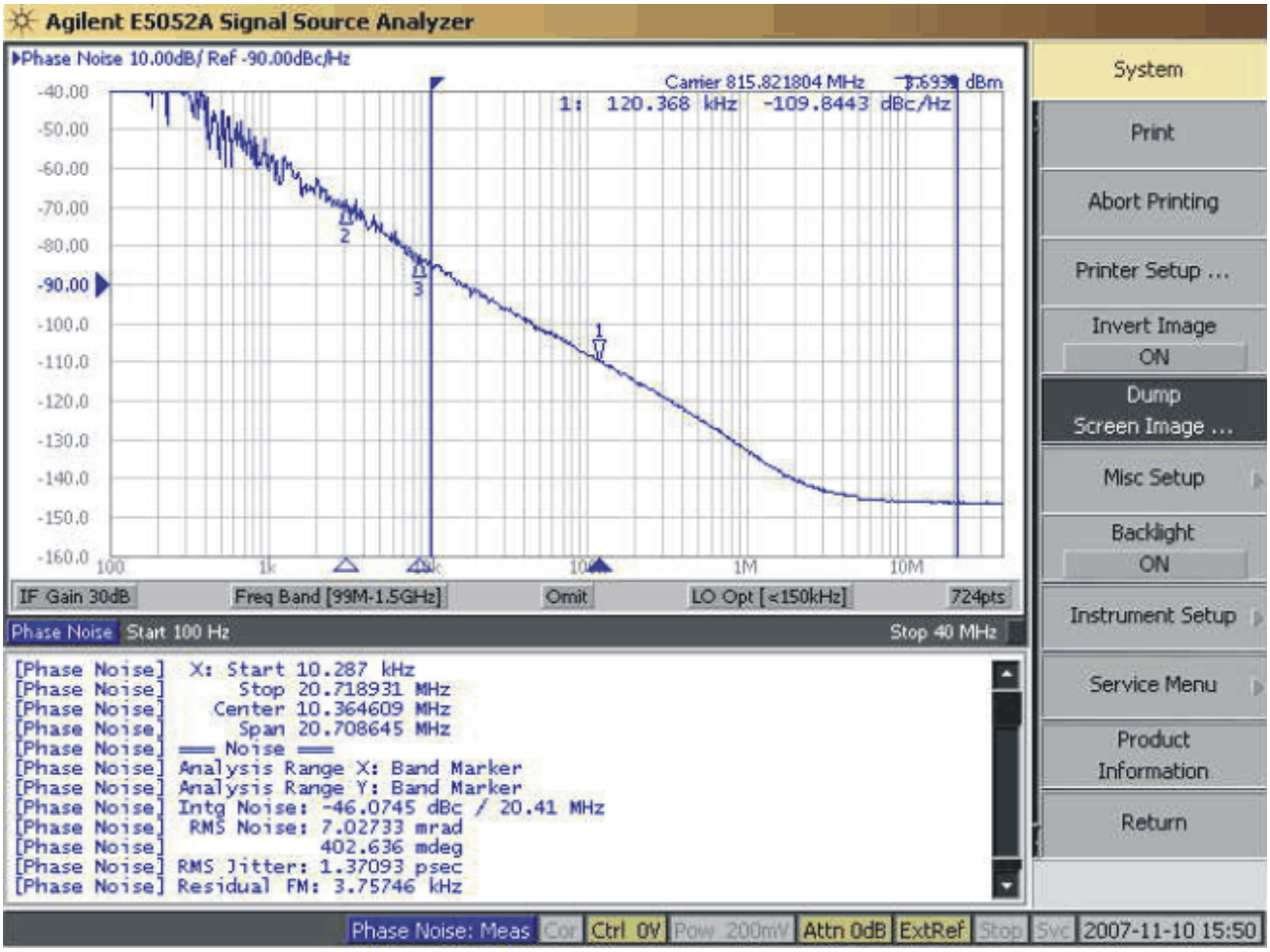


Figure 11. Open-Loop Phase Noise of On-Chip VCO2 (Prescaler Divider 3, Output Divider 1)

Figure 12 and Figure 13 show the open-loop phase npise measurements for the two VCOs with a prescaler divider of 2 and an output divider of 1.

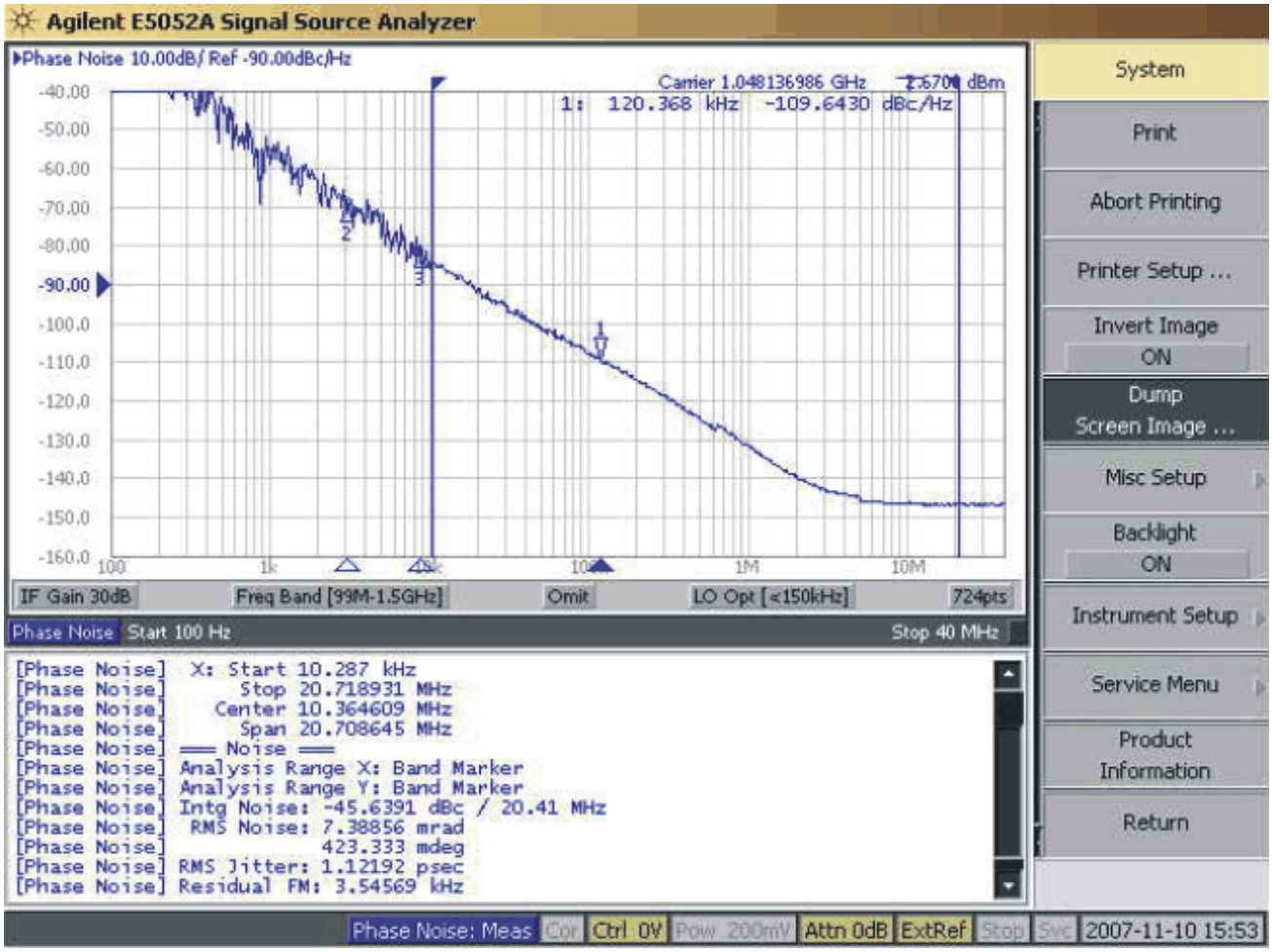


Figure 12. Open-Loop Phase Noise of On-Chip VCO1 (Prescaler Divider 2, Output Divider 1)

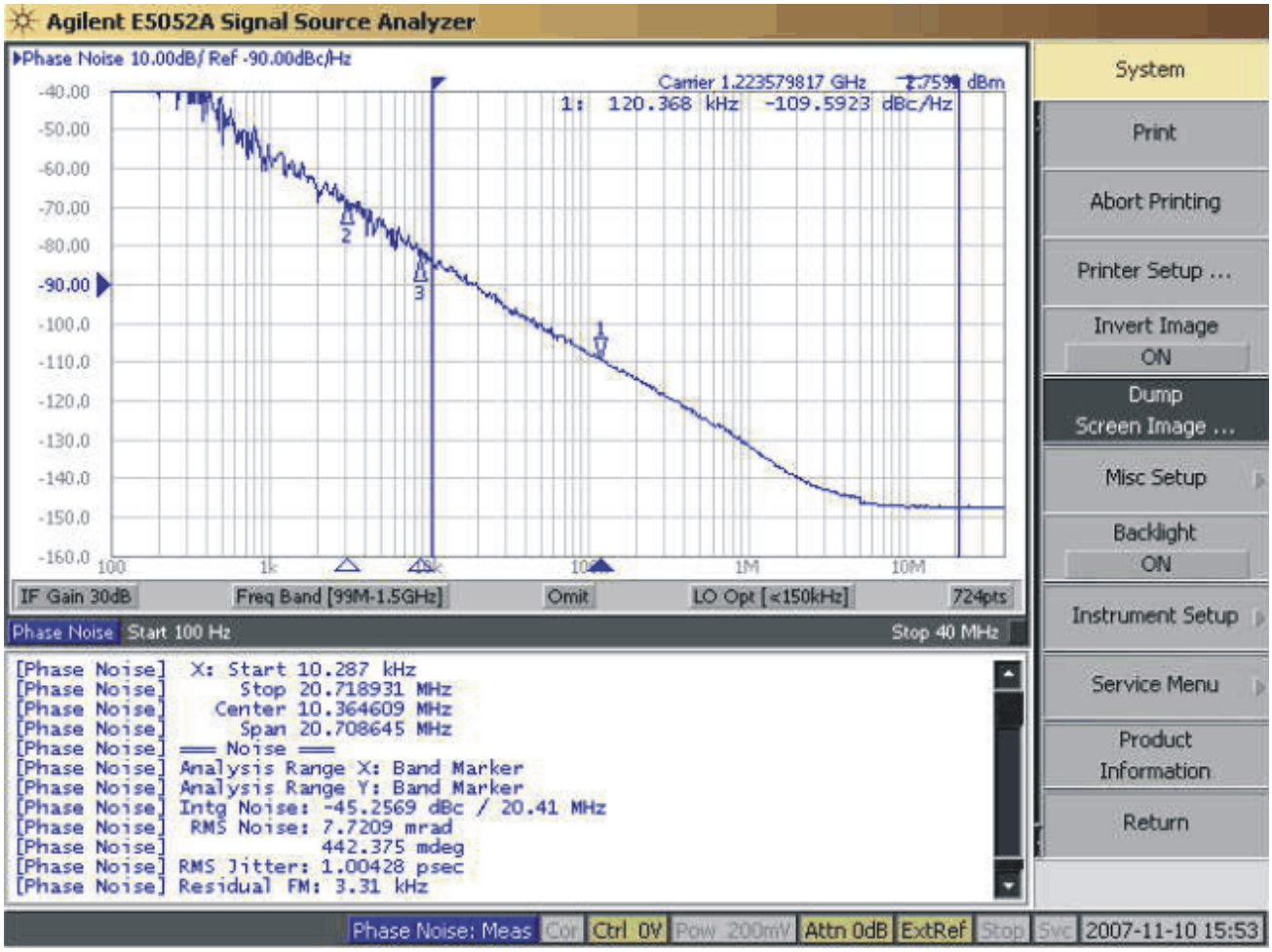


Figure 13. Open-Loop Phase Noise of On-Chip VCO2 (Prescaler Divider 2, Output Divider 1)

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