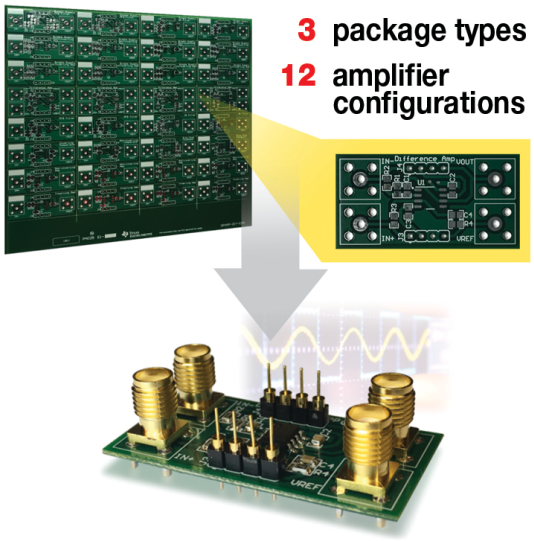
DIYAMP-SOT23-EVM



This user's guide contains support documentation for the DIYAMP-SOT23 evaluation module (EVM). Included is a description of how to set up and configure the EVM, printed circuit board (PCB) layout, schematic, and bill of materials (BOM) of the DIYAMP-SOT23-EVM.

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1 Introduction

The DIYAMP-SOT23-EVM is an EVM developed to give users the ability to easily evaluate their design concepts. This break-apart EVM has several popular op-amp configurations including: amplifiers, filters, and stability compensation configurations for both single and dual supply. The EVM is designed for 0805 and 0603 package size surface mount components enabling easy prototyping. This board gives the user the ability to build anything from a simple amplifier to complex signal chains by combining different configurations.

For more information about power supply voltages and input/output limitations, consult TI Precision Labs – Op Amps videos.

1.1 DIYAMP-SOT23-EVM Kit Contents

Table 1 details the contents included in the DIYAMP-SOT23-EVM kit.

Table 1. DIYAMP-SOT23-EVM Kit Contents

Item	Description	Quantity
DIYAMP-SOT23-EVM	PCB	1
Header Strip	100 mil (2.54 mm) spacing, 32 position, through hole	2

1.2 EVM Features

This EVM supports the following features:

- Multiple circuit configurations
- Dual- and single-supply configurations
- Breadboard compatible
- Schematic provided in silk screen on the PCB
- Multiple connector options for input and output connections: SMA, test point, and wires.

1.3 List of Circuits on the EVM

- Single-supply multiple feedback (MFB) filter
- Single-supply Sallen-Key filter
- Single-supply non-inverting amplifier
- Single-supply inverting amplifier
- Difference amplifier
- Dual-supply multiple feedback (MFB) filter
- Dual-supply Sallen-Key filter
- R_{iso} with dual feedback
- Non-Inverting Comparator
- Inverting Comparator
- Dual-supply non-inverting amplifier
- Dual-supply inverting amplifier

2 Hardware Setup

Assembly of the DIYAMP-SOT23-EVM involves identifying and breaking out the desired circuit configuration from the EVM, soldering components, header pins, and inputs and outputs connections. This section presents the details of these procedures.

2.1 EVM Circuit Locations

Figure 1 and Table 2 map the location of each circuit configuration on the EVM. Figure 1 labels each circuit configuration with a letter ranging from A to L. Table 2 matches the circuit configuration to a letter in Figure 1 and also provides the name of each individual circuit written in silk screen on the EVM.

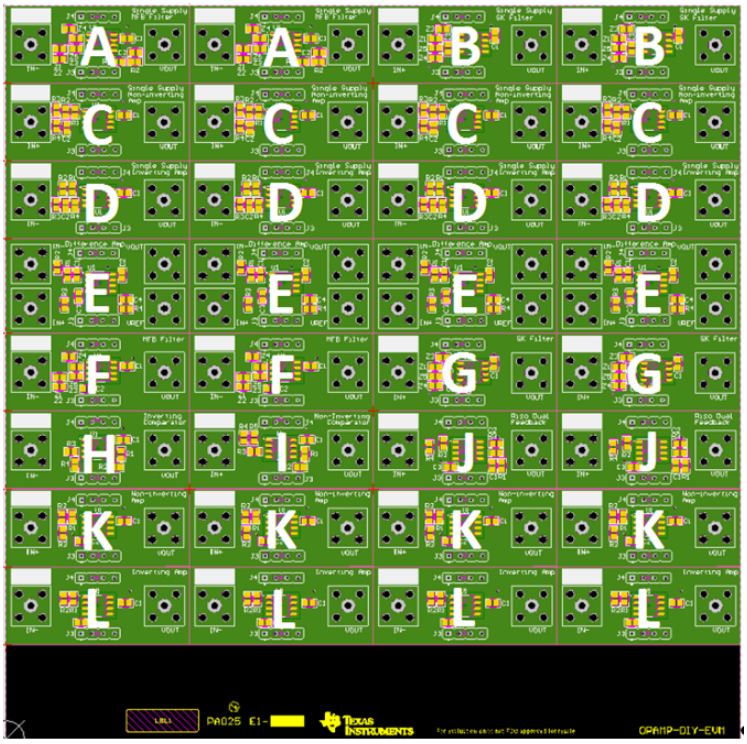

Figure 1. Location of Circuit Configurations

Table 2. Location of Circuit Legend

Circuit Name	Silk Screen Label	Letter in Figure 1
Single-supply multiple feedback filter	Single-Supply MFB Filter	A
Single-supply Sallen Key filter	Single-Supply SK Filter	B
Single-supply non-inverting amplifier	Single-Supply Non-Inverting Amp	C
Single-supply inverting amplifier	Single-Supply Inverting Amp	D
Difference amplifier	Difference Amp	E
Dual-supply multiple feedback filter	MFB Filter	F
Dual-supply Sallen Key filter	SK Filter	G
Inverting comparator	Inverting Comparator	H
Non-inverting comparator	Non-Inverting Comparator	I
R_{iso} with dual feedback	Riso Dual Feedback	J
Dual-supply non-inverting amplifier	Non-Inverting Amp	K
Dual-supply inverting amplifier	Inverting Amp	L

2.2 EVM Assembly Instructions

This section has step-by-step instructions on how to assemble a circuit configuration from the EVM.

Step 1. Choose the desired circuit configuration. See Section 2.1 for the location of each circuit configuration.

Step 2. Gently flex the PCB panel at the score lines to separate the desired circuit configuration from the EVM.

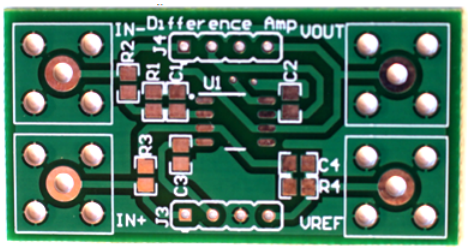

Figure 2. Detach Desired Circuit Configuration

Step 3. Solder device and surface mount passive components to the separated PCB.

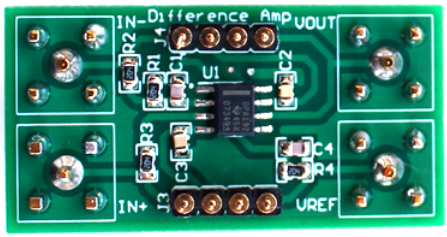

Figure 3. Detach Configuration With Attached IC and Passive Components

Step 4. Use long-nose pliers to break header strips, provided in the EVM kit, into 4-position lengths.

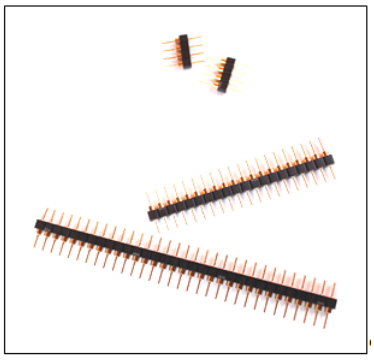

Figure 4. Terminal Strip (TS-132-G-AA) Broken Into 4-Pin Lengths

Step 5. Insert header strips into a spare DIP socket as shown in Figure 5.

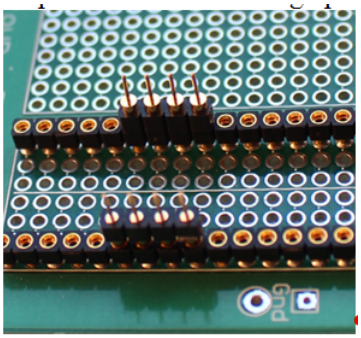

Figure 5. 4-Pin Length Terminal Strips Inserted in DIP Socket

Step 6. Position separated PCB over pins and solder the connections. Carefully remove from the DIP socket.

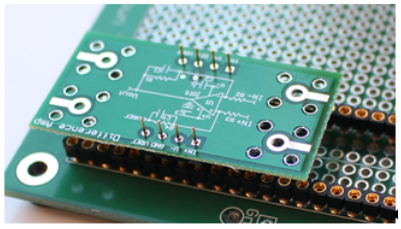

Figure 6. Detached Board Configuration Position Over Terminal Pins

Step 7. Attach SMA connectors, test points, or wires to the input and output of the separated PCB.

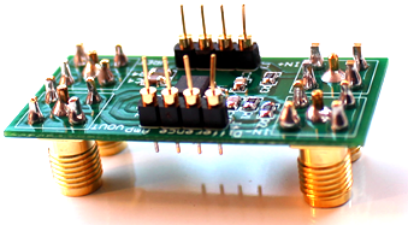

Figure 7. Fully-Assembled Circuit Configuration From DIYAMP-SOT23-EVM

3 Schematic and PCB Layout

This section provides the schematic and PCB layout of each circuit configuration provided on the EVM.

3.1 Schematic PCB Drawing

Each circuit board has a silk screen of its schematic for easy reference.

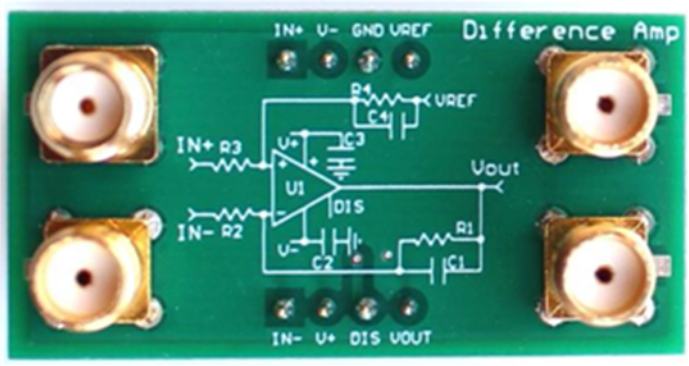

Figure 8. Silk Screen Circuit Schematic

3.2 Single-Supply, Multiple Feedback Filter

Figure 9 shows the schematic for the single-supply, multiple feedback (MFB) filter circuit configuration.

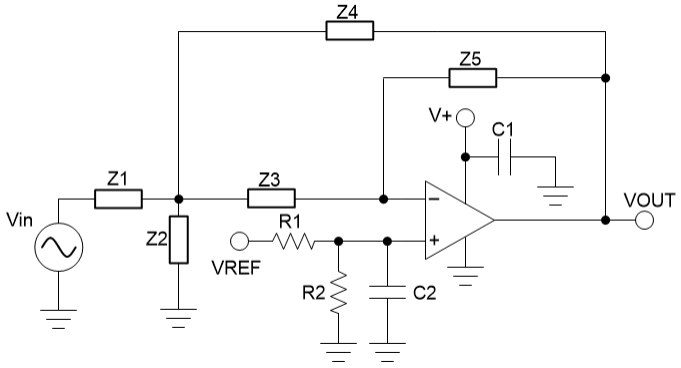

Figure 9. Single-Supply, Multiple Feedback Filter Schematic

The MFB topology (sometimes called infinite gain or Rauch) is often preferred, due to low sensitivity to component variations. The MFB topology creates an inverting second-order stage. This inversion may, or may not, be a concern in the filter application.

The single-supply, MFB filter circuit can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection of Z1 through Z5. Table 3 displays the type of passive component that should be chosen for Z1 through Z5 for each filter configuration.

Table 3. MFB Filter Type Component Selection

Pass-Band Filter Type	Type of Component (Z1)	Type of Component (Z2)	Type of Component (Z3)	Type of Component (Z4)	Type of Component (Z5)
Low Pass	R1	C2	R3	R4	C5
High Pass	C1	R2	C3	C4	R5
Band Pass	R1	R2	C3	C4	R5

For additional guidance in designing a filter, download FilterPro™ active filter design software.

Capacitor C2 provides the option to filter noise that may be introduced from the Vref input. calculates the cutoff frequency due to C2.

$$f_{c\_Vref} = \frac{1}{2\pi \times R_1 \,//\, R_2 \times C_2} \quad (1)$$

The PCB layout of the top layer of the single-supply, MFB filter configuration is displayed in Figure 10.

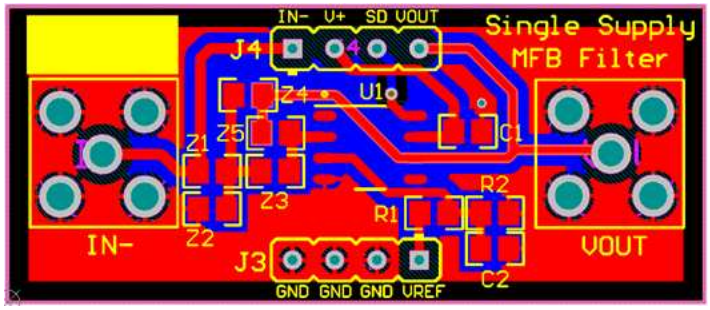

Figure 10. Single-Supply, MFB Filter Top Layer

The PCB layout of the bottom layer of the single-supply, MFB filter configuration is displayed in Figure 11.

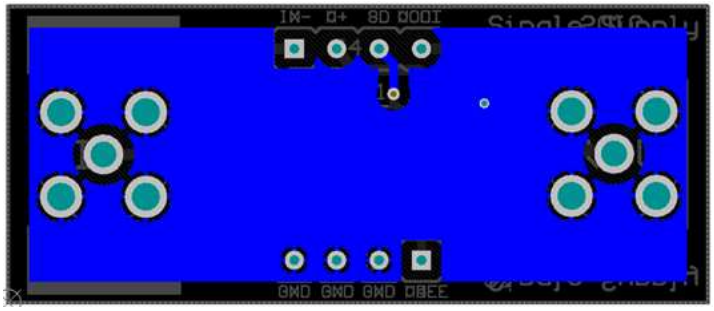

Figure 11. Single-Supply, MFB Filter Bottom Layer

3.3 Single-Supply, Sallen-Key Filter

Figure 12 shows the schematic for the single-supply, Sallen-Key filter circuit configuration.

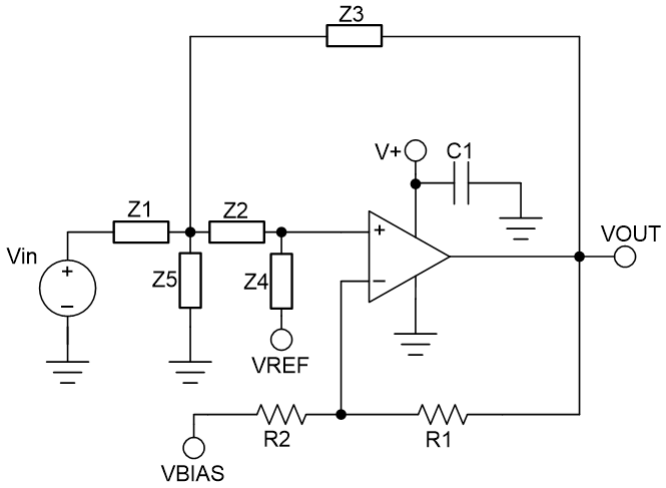

Figure 12. Single-Supply, Sallen-Key Filter Schematic

Sallen-Key is one of the most commonly applied active filter topologies. The Sallen-Key is a non-inverting, voltage-controlled, voltage-source (VCVS) able to attain larger Qs with a stable response than other filter topologies. Because Sallen-Key is non-inverting, it might be preferable over the MFB topology.

The single-supply, Sallen-Key filter can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection of Z1 through Z5. Table 4 displays the type of passive component that should be chosen for Z1 through Z5 for each filter configuration.

Table 4. Sallen-Key Filter Component Type Selection

Pass-Band Filter Type	Type of Component (Z1)	Type of Component (Z2)	Type of Component (Z3)	Type of Component (Z4)	Type of Component (Z5)
Low Pass	R1	R2	C3	C4	Not populated
High Pass	C1	C2	R3	R4	Not populated
Band Pass	R1	C2	R3	R4	C5

For additional guidance in designing a filter, download the FilterPro active filter design software.

The PCB layout of the top layer of the single-supply, Sallen-Key filter circuit configuration is displayed in Figure 13.

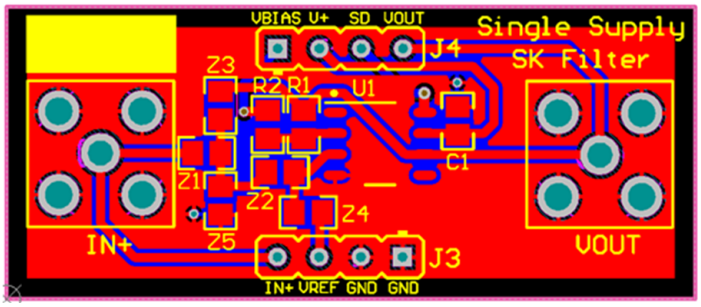

Figure 13. Single-Supply, Sallen-Key Filter Top Layer

The PCB layout of the bottom layer of the single-supply, Sallen-Key filter configuration is displayed in Figure 14.

Figure 14. Single-Supply, Sallen-Key Filter Bottom Layer

3.4 Single-Supply, Non-Inverting Amplifier

Figure 15 shows the schematic for the single-supply, non-inverting amplifier circuit configuration.

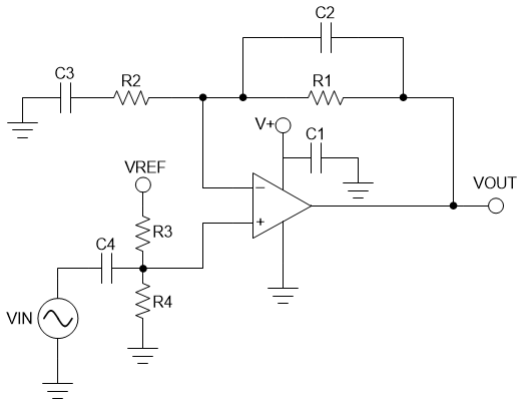

Figure 15. Single-Supply, Non-Inverting Amplifier Schematic

The non-inverting op-amp configuration takes an input signal that is applied directly to the high impedance, non-inverting input terminal and outputs a signal that is the same polarity as the input signal. The load resistance for this topology is the sum of R1 and R2. The values of the resistors in the feedback network will determine the amount of gain to amplify the input signal.

There are multiple ways to configure the single-supply, non-inverting amplifier. The following cases show three primary use case configurations for this circuit.

Case 1: Standard non-inverting circuit

This circuit board can be configured into a standard non-inverting circuit by shorting C3 and C4 with a 0-Ω resistor and leaving R3 and R4 unpopulated.

Equation 2 displays the transfer function for the standard single-supply, non-inverting amplifier circuit configuration.

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{in}$$

where

- C3 is shorted with a 0-Ω resistor
- C4 is shorted with a 0-Ω resistor
- R3 is unpopulated
- R4 is unpopulated (2)

Capacitor C2 provides the option to filter the output. The cutoff frequency of the filter can be calculated using Equation 3.

$$f_c = \frac{1}{2\pi \times R_1 \times C_2} \quad (3)$$

Case 2: AC coupled, single-supply, non-inverting circuit

This circuit board can be configured into an AC coupled non-inverting circuit by populating C3 and C4 with capacitors and populating R3 or R4 with resistors. R3 and R4 are used to set the DC output in the following two ways:

Option 1: VREF is directly applied to the input IN+

- R3 is populated with the desired biasing resistor
- R4 is unpopulated

Option 2: VREF is divided down and applied to the input IN+

- R3 and R4 are populated with resistors, see Equation 4

$$V_{IN+} = \left(\frac{R_4}{R_3 + R_4}\right) V_{ref} \quad (4)$$

The AC response of the input signal is high-passed through C4, R3 + R4. The op-amp noise-gain is unity-gain until the gain begins to rise at the zero frequency defined in Equation 5.

$$F_{ZERO} = \frac{1}{2\pi \times C_3 (R_1 + R_2)} \quad (5)$$

The gain flattens off to the same gain defined in Equation 2 at the frequency defined in Equation 6.

$$F_{pole} = \frac{1}{2\pi \times C_3 \times R_2} \quad (6)$$

For more information on the AC coupled non-inverting circuit, see e2e.ti.com.

Case 3: Non-inverting signal scaling circuit

This circuit board can be configured into a non-inverting signal scaling circuit by shorting C3 with a 0-Ω resistor and populating C4 with a resistor. This forms a 3-resistor divider with R3 and R4 on the input to scale or shift the input signal level. The op amp is typically configured as a unity-gain buffer.

Step 1. Choose a value for the resistor installed in place of C4

Step 2. Compute R3

$$R_3 = \frac{\left(1 + \frac{R_1}{R_2}\right) C_4 \times V_{ref}}{V_{offset}} \quad (7)$$

Step 3. Compute R2

$$R_2 = \frac{-V_{offset} \times C_4 \times R_3}{V_{offset} \times R_3 + V_{offset} \times C_4 - V_{ref} \times C_4} \quad (8)$$

For more information on the AC coupled non-inverting circuit, see e2e.ti.com.

The PCB layout of the top layer of the single-supply, non-inverting circuit configuration is displayed in Figure 16.

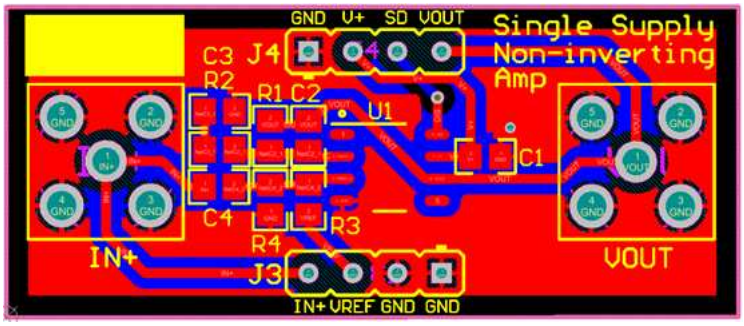

Figure 16. Single-Supply, Non-Inverting Amplifier Top Layer

The PCB layout of the bottom layer of the single-supply, non-inverting circuit configuration is displayed in Figure 17.

Figure 17. Single-Supply, Non-Inverting Amplifier Bottom Layer

3.5 Single-Supply, Inverting Amplifier

Figure 18 shows the schematic for the single-supply, inverting amplifier circuit configuration.

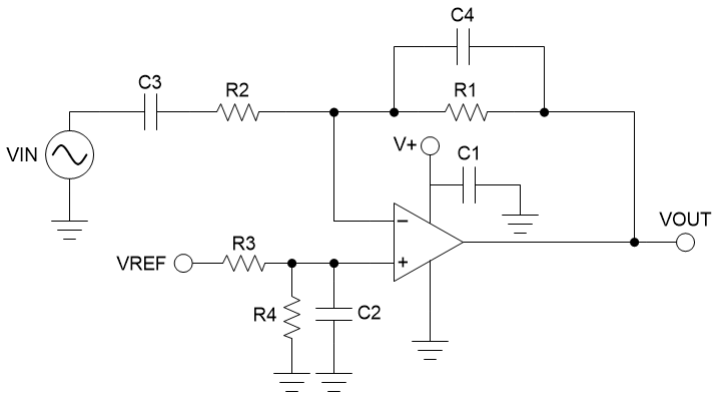

Figure 18. Single-Supply, Inverting Amplifier Schematic

The inverting op-amp configuration takes an input signal that is applied directly to the inverting input terminal and outputs a signal that is the opposite polarity as the input signal. The benefit of this topology is that it avoids common mode limitations. The load resistance for this topology is equal to R2. The values of the resistors in the feedback network will determine the amount of gain to amplify the input signal.

The single-supply, inverting amplifier circuit provides the option to AC couple the input, filter the output, and bias the output of the amplifier to a desired value.

Equation 9 displays the dc transfer function of the single-supply, inverting amplifier circuit configuration.

$$V_{out} = \left(-\frac{R_1}{R_2}\right) V_{in} + \left(1 + \frac{R_1}{R_2}\right)\left(\frac{R_4}{R_3 + R_4}\right) V_{ref} \quad (9)$$

where

- C3 is shorted with a 0-Ω resistor

Capacitor C3 provides the option to AC couple the input of the single-supply, inverting amplifier by creating a high-pass filter. Equation 10 displays the dc transfer function of the single-supply, inverting amplifier circuit configuration.

$$V_{out} = \left(\frac{R_4}{R_3 + R_4}\right) V_{ref} \quad (10)$$

where

- The input is AC coupled with C3

The cutoff frequency of the high-pass filter can be calculated using Equation 11.

$$f_{c\_highpass} = \frac{1}{2\pi \times C_3 \times R_2} \quad (11)$$

Equation 12 displays the transfer function when the frequency of the input signal is above the cutoff frequency calculated in Equation 11.

$$V_{out} = \left(-\frac{R_1}{R_2}\right) V_{in} + \left(\frac{R_4}{R_3 + R_4}\right) V_{ref} \quad (12)$$

Capacitor C2 filters noise that may be introduced from the Vref input. Equation 13 calculates the cutoff frequency due to C2.

$$f_{c\_Vref} = \frac{1}{2\pi \times R_3 \,//\, R_4 \times C_2} \quad (13)$$

Capacitor C4 provides the option to filter the output. The cutoff frequency of the filter can be calculated using Equation 14.

$$f_{c\_Vout} = \frac{1}{2\pi \times R_1 \times C_4} \quad (14)$$

The PCB layout of the top layer of the single-supply, inverting amplifier circuit configuration is displayed in Figure 19.

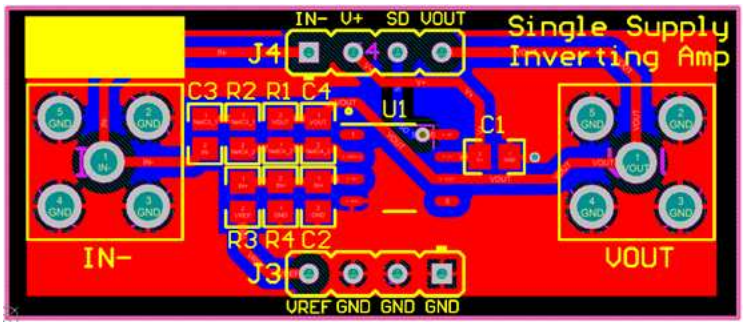

Figure 19. Single-Supply, Inverting Amplifier Top Layer

The PCB layout of the bottom layer of the single-supply, inverting amplifier circuit configuration is displayed in Figure 20.

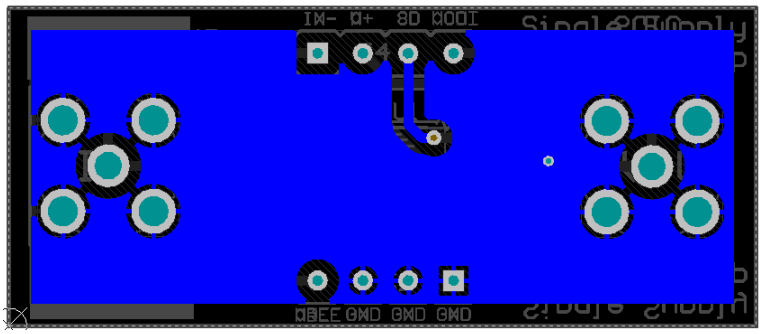

Figure 20. Single-Supply, Inverting Amplifier Bottom Layer

3.6 Difference Amplifier

Figure 21 shows the schematic for the difference amplifier circuit configuration.

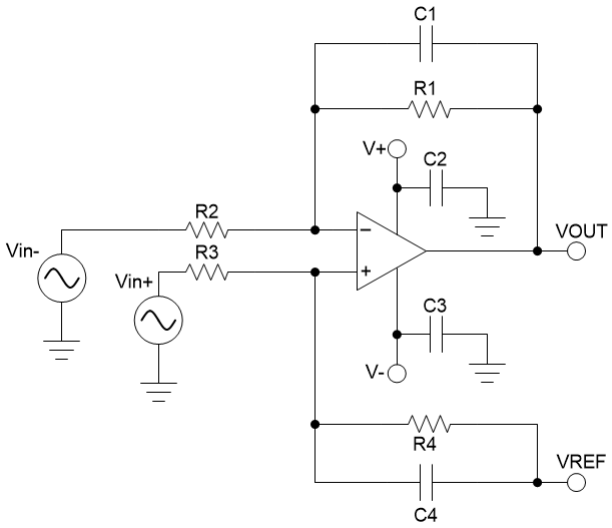

Figure 21. Difference Amplifier Schematic

The difference amplifier utilizes both inverting and non-inverting inputs and produces an output that is equal to the difference between the inputs. The gain of the difference amplifier is dependent on the ratio of the resistor values selected.

Equation 15 displays the transfer function of the difference amplifier circuit configuration.

$$V_{out} = \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_1}{R_2}\right) V_{IN+} + \left(\frac{R_3}{R_3 + R_4}\right)\left(1 + \frac{R_1}{R_2}\right) V_{ref} + \frac{R_1}{R_2} V_{IN-} \quad (15)$$

If $R_1 = R_4$ and $R_2 = R_3$, Equation 15 can be simplified to Equation 16.

$$V_{out} = \frac{R_1}{R_2}\left(V_{IN+} - V_{IN-}\right) + V_{ref} \quad (16)$$

Capacitors C1 and C4 provide the option to filter the output of the amplifier. The cutoff frequency of the filter can be calculated using Equation 17.

$$f_c = \frac{1}{2\pi \times R_1 \times C_1} \quad (17)$$

where

- $R_1 = R_4$, $R_2 = R_3$, and $C_1 = C_4$

The PCB layout of the top layer of the difference amplifier circuit configuration is displayed in Figure 22.

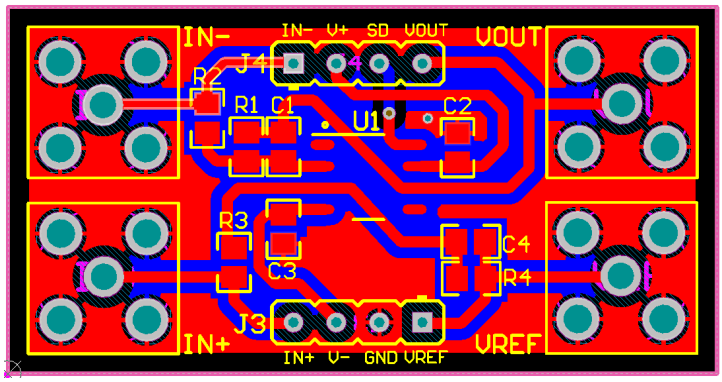

Figure 22. Difference Amplifier Top Layer

The PCB layout of the bottom layer of the difference amplifier circuit configuration is displayed in Figure 23.

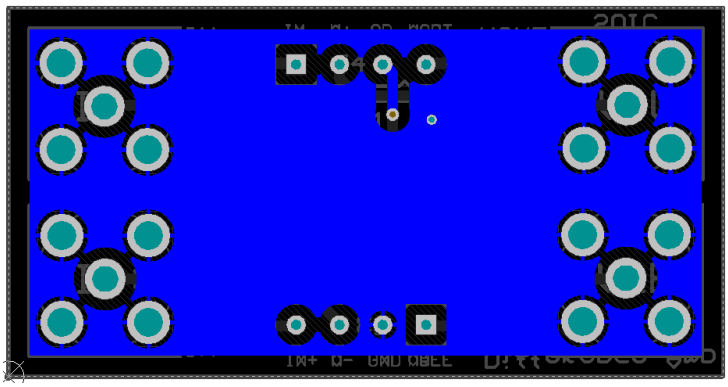

Figure 23. Difference Amplifier Bottom Layer

3.7 Dual-Supply, Multiple Feedback Filter

Figure 24 shows the schematic for the dual-supply, multiple feedback filter circuit configuration.

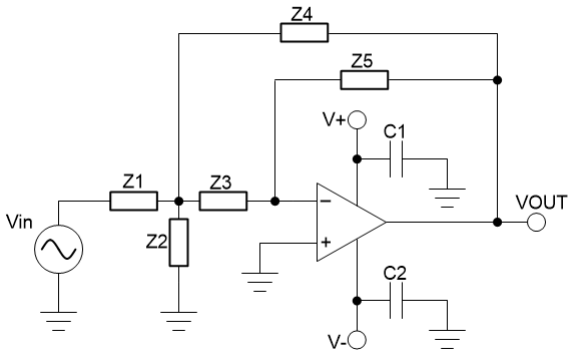

Figure 24. Dual-Supply, Multiple Feedback Filter Schematic

The MFB topology (sometimes called infinite gain or Rauch) is often preferred due to low sensitivity to component variations. The MFB topology creates an inverting second-order stage. This inversion may, or may not, be a concern in the filter application.

The dual-supply, MFB filter circuit can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection of Z1 through Z5. Table 5 displays the type of passive component that should be chosen for Z1 through Z5 for each filter configuration.

Table 5. MFB Filter Type Component Selection

Pass-Band Filter Type	Type of Component (Z1)	Type of Component (Z2)	Type of Component (Z3)	Type of Component (Z4)	Type of Component (Z5)
Low Pass	R1	C2	R3	R4	C5
High Pass	C1	R2	C3	C4	R5
Band Pass	R1	R2	C3	C4	R5

For additional guidance in designing a filter, download the FilterPro active filter design software.

The PCB layout of the top layer of the dual-supply, multiple feedback filter circuit configuration is displayed in Figure 25.

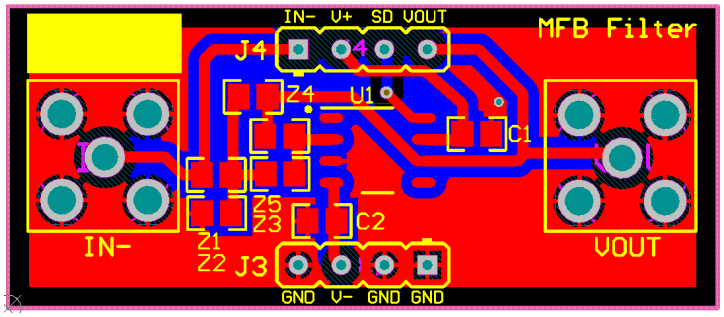

Figure 25. Dual-Supply, Multiple Feedback Filter Top Layer

The PCB layout of the bottom layer of the dual-supply, multiple feedback filter circuit configuration is displayed in Figure 26.

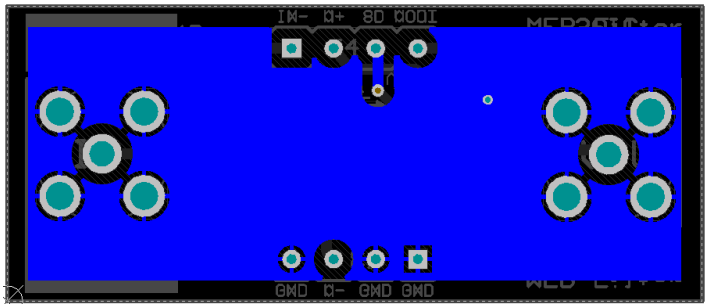

Figure 26. Dual-Supply, Multiple Feedback Bottom Layer

3.8 Dual-Supply, Sallen-Key Filter

Figure 27 shows the schematic for the dual-supply, Sallen-Key Filter circuit configuration.

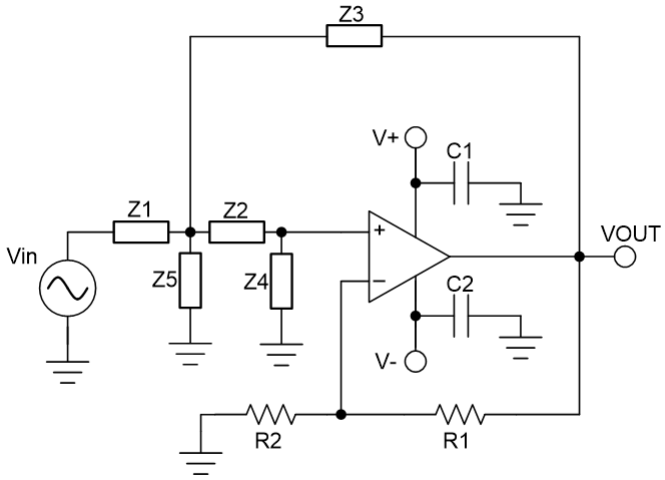

Figure 27. Dual-Supply, Sallen-Key Filter Schematic

Sallen-Key is one of the most commonly applied active filter topologies. The Sallen-Key is a non-inverting, voltage-controlled, voltage-source (VCVS) able to attain larger Qs with a stable response than other filter topologies. Because Sallen-Key is non-inverting, it might be preferable over the MFB topology.

For this EVM, the Sallen-key filter can be configured for unity-gain by populating R1 with a short and leaving R2 open. Gain can be added by adding the appropriate resistors to R2 and R1 as explained in FilterPro.

The dual-supply, Sallen-Key filter can be configured as a low-pass filter, high-pass filter, or band-pass filter based on the component selection of Z1 through Z5. Table 6 displays the type of passive component that should be chosen for Z1 through Z5 for each filter configuration.

Table 6. Sallen-Key Filter Component Type Selection

Pass-Band Filter Type	Type of Component (Z1)	Type of Component (Z2)	Type of Component (Z3)	Type of Component (Z4)	Type of Component (Z5)
Low Pass	R1	R2	C3	C4	Not populated
High Pass	C1	C2	R3	R4	Not populated
Band Pass	R1	C2	R3	R4	C5

For additional guidance in designing a filter, download the FilterPro active filter design software.

The PCB layout of the top layer of the dual-supply, Sallen-Key filter circuit configuration is displayed in Figure 28.

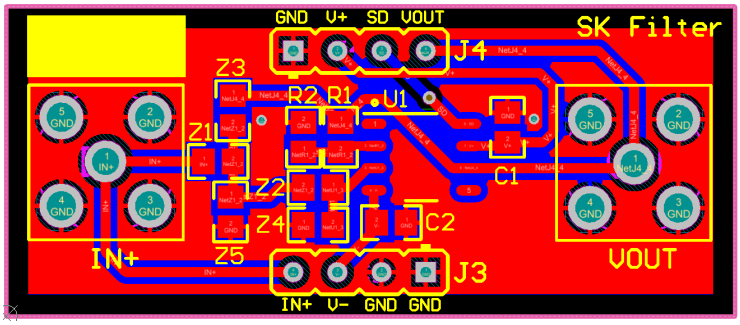

Figure 28. Dual-Supply, Sallen-Key Top Layer

The PCB layout of the bottom layer of the dual-supply, Sallen-Key filter circuit configuration is displayed in Figure 29.

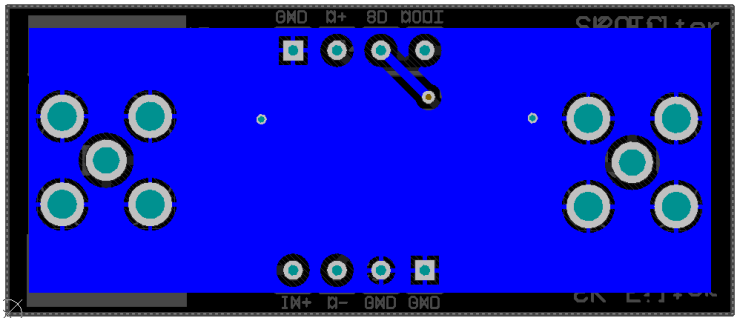

Figure 29. Dual-Supply, Sallen-Key Bottom Layer

3.9 Inverting Comparator

Figure 30 shows the schematic for the inverting comparator circuit configuration.

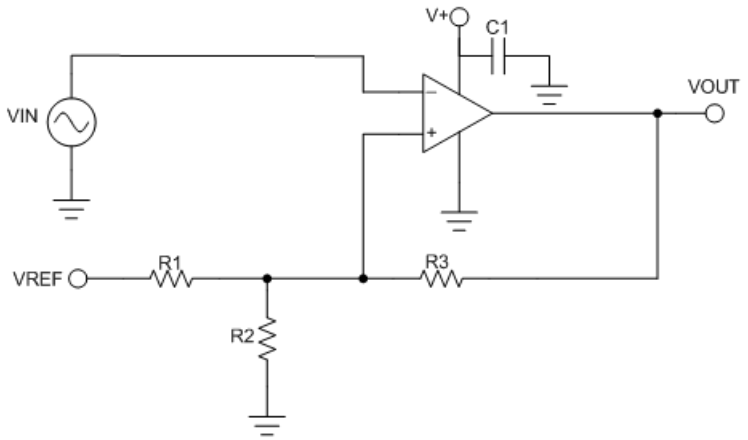

Figure 30. Inverting Comparator Schematic

It is important to note that this circuit layout is meant for SOT23 package op amps or push-pull output type comparators. This configuration uses a voltage divider R1 and R2 to set up the threshold voltage when no hysteresis is added. The comparator will compare the input signal (Vin) to the threshold voltage (Vth).

$$V_{th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{ref} \quad (18)$$

where

- R3 is unpopulated

The comparator input signal is applied to the inverting input, so the output will have an inverted polarity. When Vin > Vth, the output will drive to the negative supply (GND or logic low). When Vin < Vth, the output will drive to the positive supply (V+ or logic high).

R3 can be populated to implement hysteresis which uses two different threshold voltages to avoid the multiple transitions. The input signal must exceed the upper threshold (VH) to transition low or below the lower threshold (VL) to transition high. Equation 19 and Equation 20 will calculate the value of R2 and R3 for the two desired thresholds.

$$R_3 = \left(\frac{V_L}{V_H - V_L} \right) R_1 \quad (19)$$

$$R_2 = \left(\frac{V_L}{V_+ - V_H} \right) R_1 \quad (20)$$

The PCB layout of the top layer of the inverting comparator circuit configuration is displayed in Figure 31.

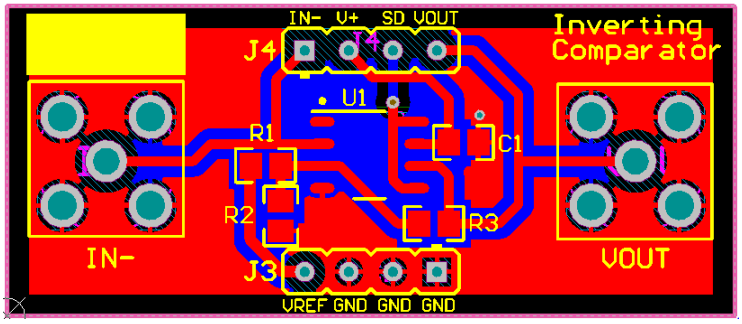

Figure 31. Inverting Comparator Top Layer

The PCB layout of the bottom layer of the inverting comparator circuit configuration is displayed in Figure 32.

Figure 32. Inverting Comparator Bottom Layer

3.10 Non-Inverting Comparator

Figure 33 shows the schematic for the non-inverting comparator circuit configuration.

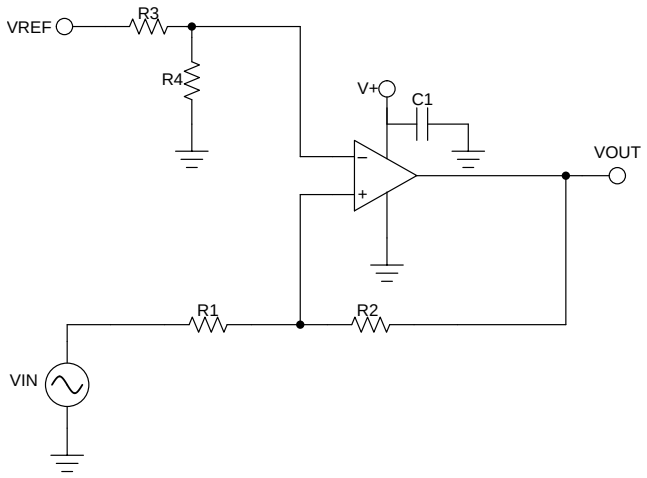

Figure 33. Non-Inverting Comparator Schematic

It is important to note that this circuit layout is meant for SOT23 package op amp or push-pull output type comparators. This configuration uses a voltage divider R3 and R4 to set up the threshold voltage. The comparator will compare the input signal (Vin) to the threshold voltage (Vth).

$$V_{th} = \left(\frac{R_4}{R_3 + R_4} \right) V_{ref} \tag{21}$$

The comparator input signal is applied to the non-inverting input, so the output will have a non-inverted polarity. When Vin > Vth, the output will drive to the positive supply (V+ or logic high). When Vin < Vth, the output will drive to the negative supply (GND or logic low).

R2 can be populated to implement hysteresis which uses two different threshold voltages to avoid the multiple transitions. The input signal must exceed the upper threshold (VH) to transition high or below the lower threshold (VL) to transition low. Equation 22 and Equation 23 will calculate the value of R1 and R2 for the two desired thresholds.

$$R_1 = \frac{(V_h - V_{th})}{V_{th}} R_2 \tag{22}$$

$$R_2 = \frac{(V_{th} + V_+)}{(V_l - V_{th})} R_1 \tag{23}$$

The PCB layout of the top layer of the non-inverting comparator circuit configuration is displayed in Figure 34.

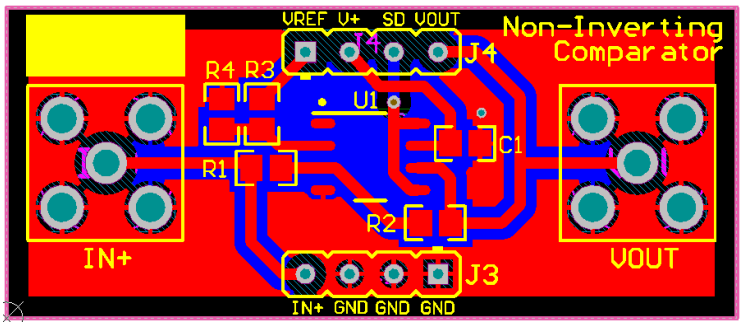

Figure 34. Non-inverting Comparator Top Layer

The PCB layout of the top layer of the non-inverting comparator circuit configuration is displayed in Figure 35.

Figure 35. Non-Inverting Comparator Bottom Layer

3.11 R_{iso} With Dual Feedback

Figure 36 shows the schematic for the R_{iso} with dual-feedback circuit configuration.

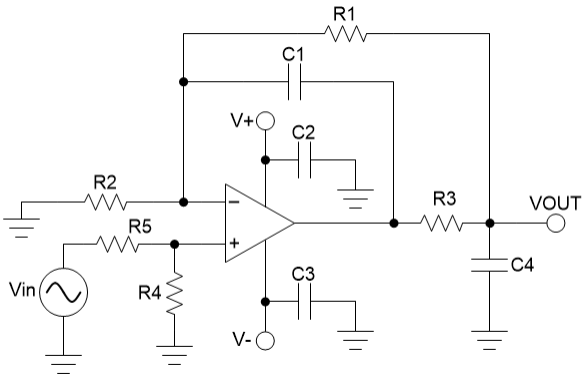

Figure 36. R_{iso} with Dual-Feedback Schematic

The dc gain of the R_{iso} with dual-feedback circuit configuration can be calculated using Equation 24.

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right)\left(\frac{R_4}{R_4 + R_5}\right)V_{in} \quad (24)$$

In situations where stability is affected by capacitive loads, the R_{iso} dual-feedback configuration has the ability to stabilize the circuit by compensating the contribution of the capacitive load to circuit instability. This capacitive load compensation technique uses an isolation resistor that compensates the circuit by adding a zero to cancel the pole from the output impedance and capacitive load. Refer to the *TI Precision Labs - Op Amps: Stability 5* video for detailed information on this technique.

The design steps for the R_{iso} method follow:

1. Use TINA-TI™ to find the zero frequency, f_{ZERO}, where A_{OL_Loaded} = 20 dB (example shown in Figure 37).

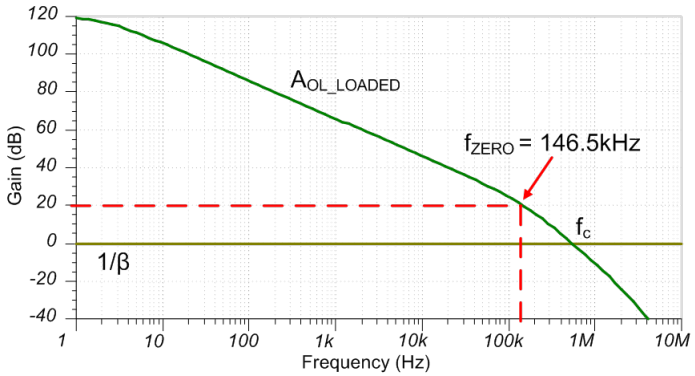

Figure 37. Example of f_{ZERO}, Where A_{OL_Loaded} = 20 dB

2. Calculate R_{iso} to set the zero at f_{ZERO} – this will yield between 60° and 90° of phase margin

$$R_{iso} = \frac{1}{2\pi \times f_{ZERO} \times C_{Load}} \quad (25)$$

where

- R_{iso} = R3
- C_{Load} = C4

While the R_{iso} circuit is both simple to implement and design, it has a big disadvantage in precision circuits. The voltage drop from R_{iso} is dependent on the output current or output load, and may be significant compared to the desired signal.

The second capacitive load compensation technique uses the R_{iso} with dual-feedback stability compensation method. The R_{iso} dual-feedback circuit solves the voltage drop disadvantage of the previously stated R_{iso}. Refer to the *TI Precision Labs - Op Amps: Stability 6* video for detailed information on this technique.

Design steps for the R_{iso} method follow:

1. R_{iso} using Method 1: R_{iso} techniques
2. Set R1: $R_1 \geq (R_{iso} \times 100)$
3. Set C_1: $\frac{6R_{iso} \times C_{Load}}{R_1} \leq C_1 \leq \frac{10R_{iso} \times C_{Load}}{R_1}$

Using this range ensures that the two feedback paths, R_2 and C_3, will never create a resonance that would cause instability. Smaller values of C3 will result in faster settling time at the expense of overshoot for certain load ranges. While the R_{iso} dual-feedback circuit solves the dc accuracy issue with the R_{iso} circuit, it has some disadvantages as well. The disadvantage of this method is that the circuit is not as tolerant to changes in the output capacitance and can quickly become unstable. Therefore, the R_{iso} dual-feedback circuit is best for situations where the output capacitance is known and will not vary significantly. This method generally results in a slower settling time than the R_{iso} circuit as well.

The PCB layout of the top layer of the R_{iso} dual-feedback amplifier circuit configuration is displayed in Figure 38

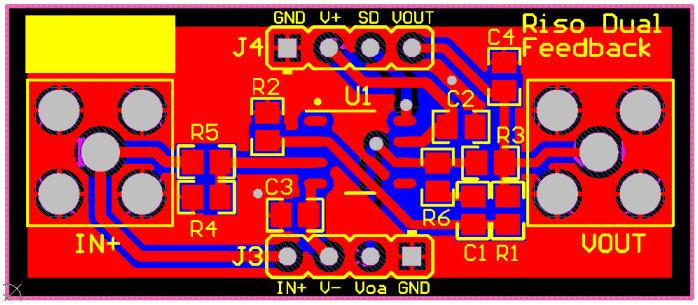

Figure 38. R_{iso} Dual-Feedback Top Layer

The PCB layout of the bottom layer of the R_{iso} dual-feedback amplifier circuit configuration is displayed in Figure 39.

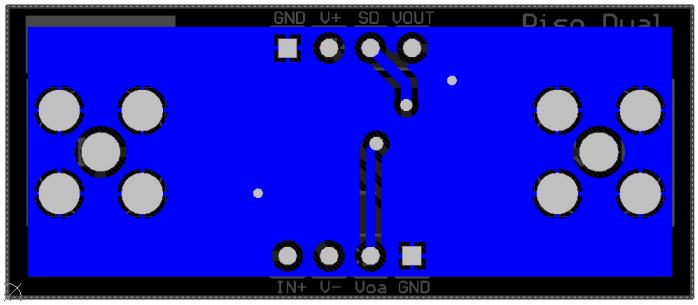

Figure 39. R_{iso} Dual-Feedback Bottom Layer

3.12 Dual-Supply, Non-Inverting Amplifier

Figure 40 shows the schematic for the dual-supply, non-inverting amplifier circuit configuration.

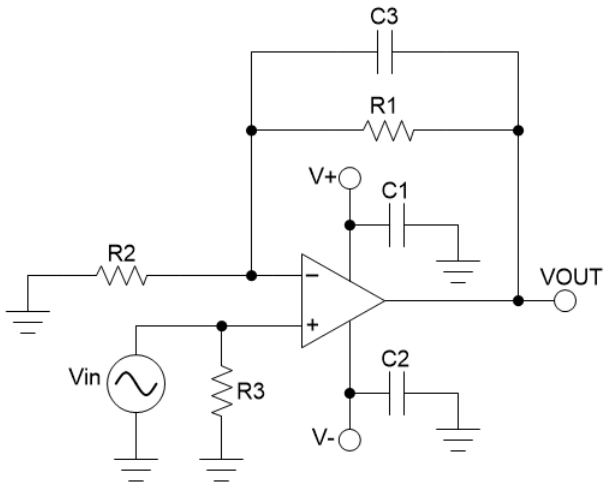

Figure 40. Dual-Supply, Non-Inverting Amplifier Schematic

The non-inverting op-amp configuration takes an input signal that is applied directly to the high impedance non-inverting input terminal and outputs a signal that is the same polarity as the input signal. The load resistance for this topology is the sum of R1 and R2. The values of the resistors in the feedback network will determine the amount of gain to amplify the input signal.

Equation 26 displays the transfer function of the dual-supply, non-inverting amplifier circuit configuration shown in Figure 40.

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{in} \tag{26}$$

Capacitor C3 provides the option to filter the output. The cutoff frequency of the filter can be calculated using Equation 27.

$$f_c = \frac{1}{2\pi \times R_1 \times C_3} \tag{27}$$

The PCB layout of the top layer of the dual-supply, non-inverting amplifier circuit configuration is displayed in Figure 41

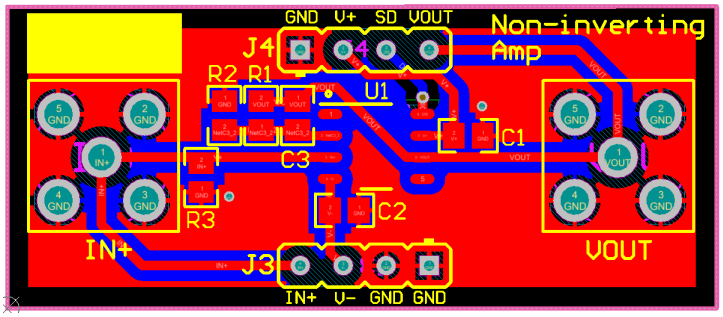

Figure 41. Dual-Supply, Non-Inverting Amplifier Top Layer

The PCB layout of the bottom layer of the dual-supply, non-inverting amplifier circuit configuration is displayed in Figure 42.

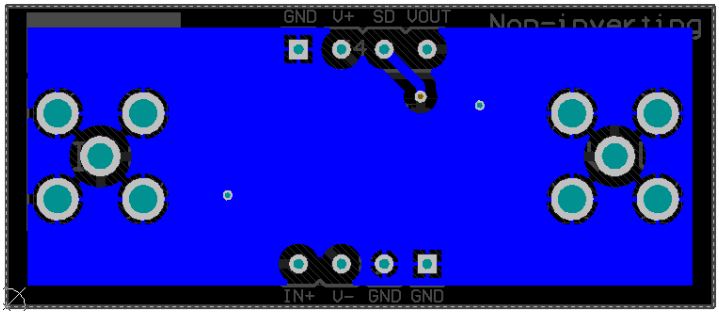

Figure 42. Dual-Supply, Non-Inverting Amplifier Bottom Layer

3.13 Dual-Supply, Inverting Amplifier

Figure 43 shows the schematic for the dual-supply, inverting amplifier circuit configuration.

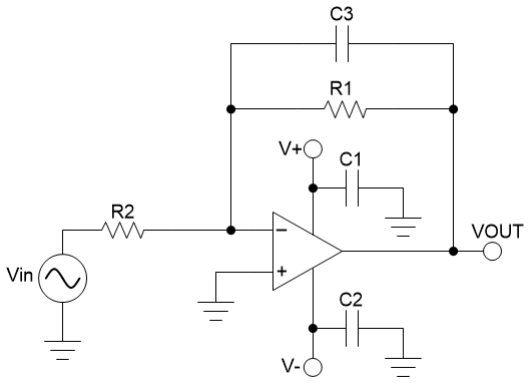

Figure 43. Dual-Supply, Inverting Amplifier Schematic

The inverting op-amp configuration takes an input signal that is applied directly to the inverting input terminal and outputs a signal that is the opposite polarity as the input signal. The benefit of this topology is that it avoids common mode limitations. The load resistance for this topology is equal to R2. The values of the resistors in the feedback network will determine the amount of gain to amplify the input signal.

Equation 28 displays the transfer function for the dual-supply, inverting amplifier circuit configuration shown in Figure 43.

$$V_{out} = -\frac{R_1}{R_2} V_{in} \tag{28}$$

Capacitor C3 provides the option to filter the output. The cutoff frequency of the filter can be calculated using Equation 29.

$$f_c = \frac{1}{2\pi \times R_1 \times C_3} \tag{29}$$

The PCB layout of the top layer of the dual-supply, inverting amplifier circuit configuration is displayed in Figure 44.

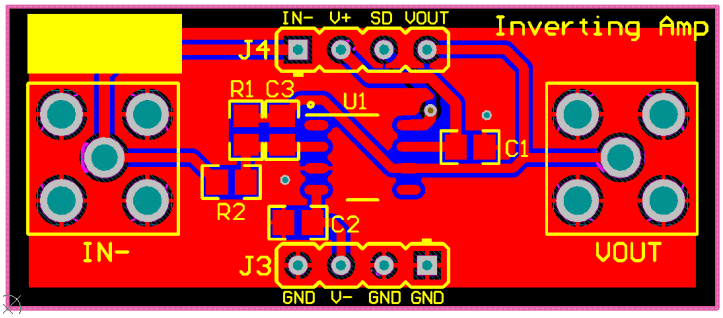

Figure 44. Dual-Supply, Inverting Amplifier Top Layer

The PCB layout of the bottom layer of the dual-supply, inverting amplifier circuit configuration is displayed in Figure 45.

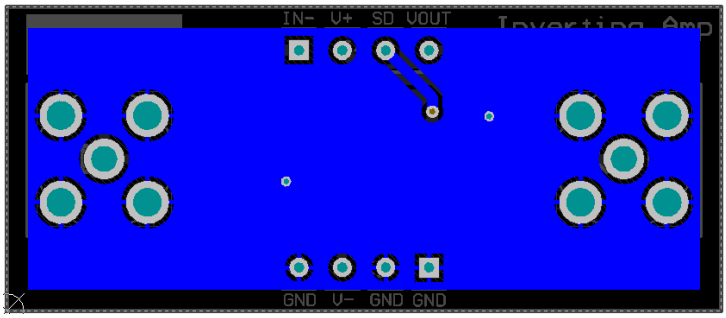

Figure 45. Dual-Supply, Inverting Amplifier Bottom Layer

4 Connections

This section provides a description for each connection available on the EVM.

4.1 Inputs and Outputs

The input/output connection slots were designed to fit the following connections: vertical SMA, horizontal SMA, wires, or through-hole test points. Examples of these four connectors are shown in this section.

The SMA recommended for this board is TE Connectivity part number 5-1814400-1.

Figure 46 shows SMA vertical connectors attached to both the input and output terminal.

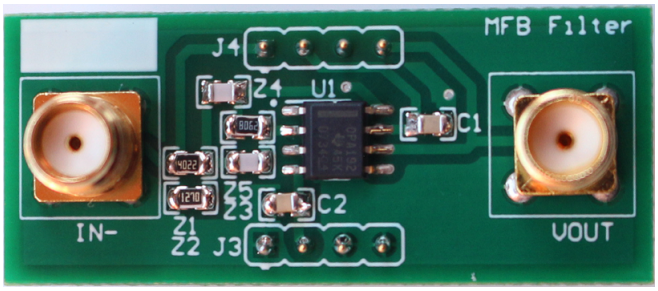

Figure 46. SMA Vertical Connectors

Figure 47 shows SMA horizontal connectors attached to the input signal terminal.

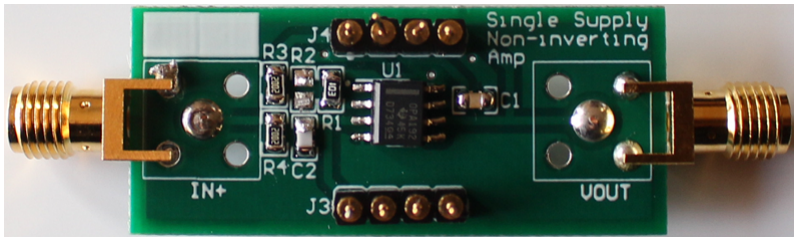

Figure 47. SMA Horizontal Connectors

Figure 48 shows a wire attached to the input and output terminal.

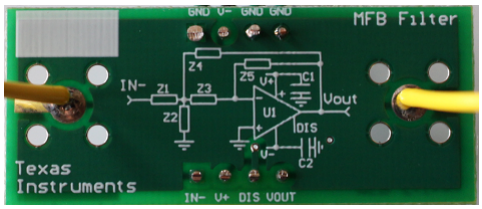

Figure 48. Wire Connections

Figure 49 shows a through-hole test point connector attached to the output and Vref terminal.

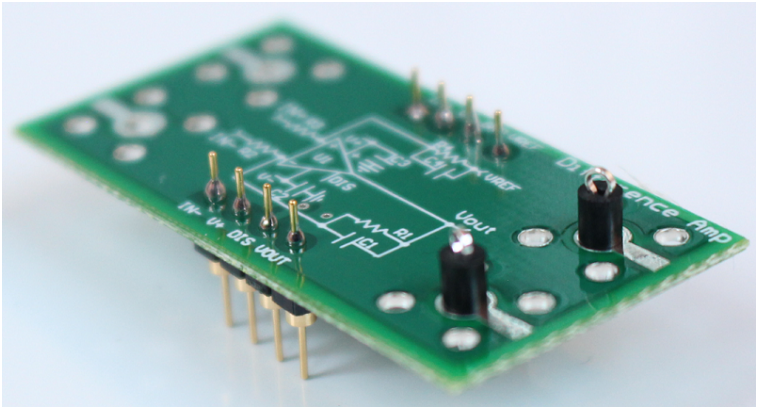

Figure 49. Through-Hole Test Points

The input and output connections can also be accessed from the header strip. The input connections are labeled IN+ and IN- for the non-inverting and inverting inputs, respectively. The output connection is labeled VOUT. An example highlighting the input and output is shown in Figure 50.

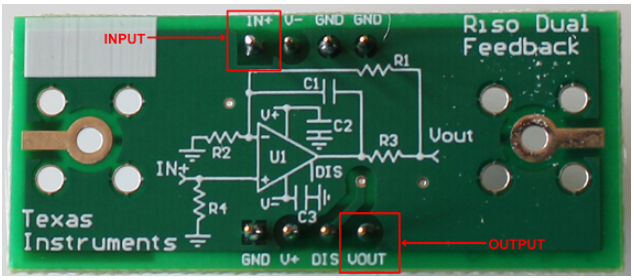

Figure 50. Input and Output Pins in Terminal Area

4.2 Power

This EVM features both dual- and single-supply, op-amp configurations. Power can only be applied using the header pins located at the top and bottom of the PCB. The positive supply is labeled V+, the negative supply is labeled V–, and ground is labeled GND. As an alternative, wire can be used in place of the included terminals strips to power the board directly. Figure 51 shows an all-wire assembly for a multiple feedback filter configuration.

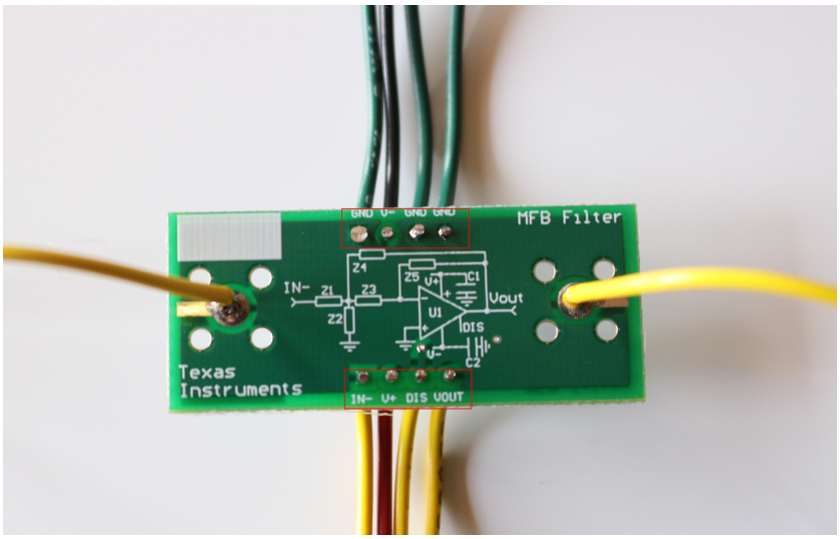

Figure 51. Wire Alternative for Terminal Area

4.3 Enable and Disable Feature

The DIYAMP-SOT23-EVM provides a means to test the shutdown feature for op-amp devices equipped with a shutdown pin. The access to the shutdown pin, labeled SD, is located on the terminal area.

5 Bill of Materials and Reference

5.1 Bill of Materials

Table 7 lists the bill of materials.

Table 7. Bill of Materials

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed-Circuit Board		PA031	Any
TS1, TS2	2		Header, 2.54mm,32x1,Gold,TH		TS-132-G-AA	Samtec

5.2 Reference

1. *Comparator with Hysteresis Reference Design* (TIDU020)
2. TI Precision Labs Training https://training.ti.com/ti-precision-labs-op-amps
3. *Analysis of the Sallen-Key Architecture* (SLOA024)
4. *AC Coupled, Single-Supply, Inverting and Non-inverting Amplifier Reference Design* (TIDU871)
5. FilterPro Design Tool

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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