Application Note

The Davies Sinusoidal Generator

Steven Dunbar, PE *Analog Field Applications*

ABSTRACT

Good quality sinusoidal waveforms can be deceptively difficult to generate. Traditional continuous-time circuits such as the Wien bridge oscillator are simple in principle, but require much additional non-linear circuitry for good performance. It is also becoming difficult to source the components (such as incandescent light bulbs and JFETs) to build the old continuous-time designs. Discrete time solutions usually require expensive precision digital-to-analog converters (DAC) and significant digital logic and firmware that can be too burdensome for many applications. This application note discusses how to use simple Medium Scale Integrated (MSI) logic along with resistors and amplifiers to generate waveforms having well-defined frequency and amplitude, while also providing relatively good harmonic distortion performance.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Good quality sinusoidal waveforms are often required for test and measurement and audio applications, but generating them with accurate frequency, amplitude, and low harmonic distortion is more difficult than can be expected. Sinusoidal generator circuits broadly fall into two classes: continuous-time and discrete-time solutions. Continuous time circuits such as the Wien bridge or phase-shift oscillators are fundamentally simple, but often require challenging non-linear circuitry to stabilize amplitude, are difficult to tune electronically, and have poor frequency stability. Without feedback control of amplitude, total harmonic distortion below about 1% is difficult to achieve, and amplitude stability can still be problematic over temperature and unit-to-unit variation.

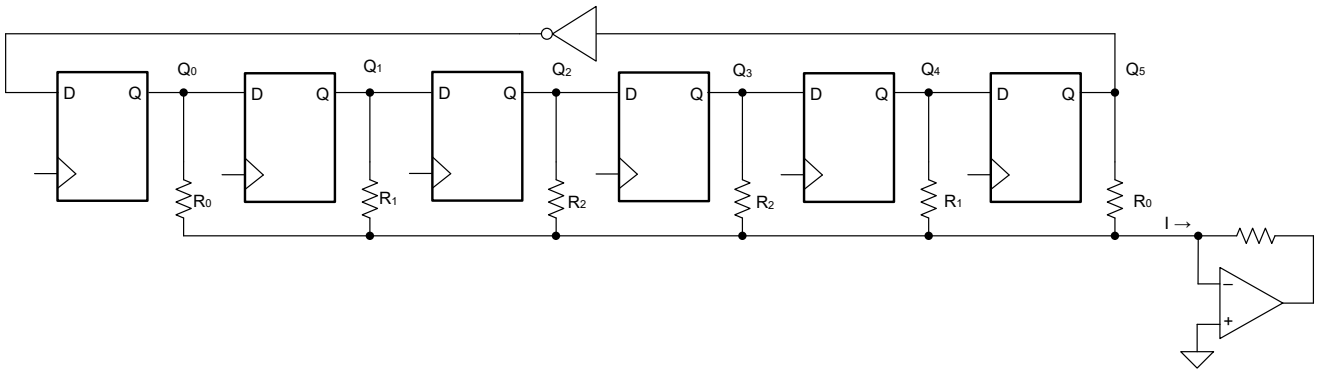
Discrete time circuits based on DACs are now common and can also synthesize non-sinusoidal waveforms. Driving these DACs usually requires substantial digital hardware such as programmable gate arrays or processors, along with the firmware to configure the DAC and clock waveform data through it. Depending on the DAC and reconstruction filter chosen, excellent performance can be achieved but at the expense of this complex digital logic.

In 1969, Tony Davies published an IEEE paper[1] documenting how to create sinusoids using a discrete-time approach from a Johnson counter[3] and weighted resistors summing up to an output similar to a finite impulse response filter. Davies' analysis is z-domain based; an approach now used for most modern digital signal processing problems. Referring to this earlier work, in 1976 Don Lancaster demonstrated[2] an implementation using 4000-series MSI logic for a simple generator having reasonably good results but with the potential for much better performance by further scaling up the circuit.

This approach is tailored specifically for sinusoids and requires only a simple Johnson counter and a symmetric array of weighted resistors (Figure 2-1) to create a stepped-sinusoid output akin to a discrete time DAC-based device. The stepped-sinusoid is easily filtered to remove residual harmonics for the final output, and frequency can be stepped very quickly. This approach solves the problems associated with continuous time circuits but without the need for substantial logic or programmable devices and their related firmware, or DACs. Using modern and economical MSI components such as the HCS logic series from Texas Instruments, sinusoids up through 10's of MHz can be created. Frequency and amplitude stability are limited only by the precisions of the time base and reference voltage used, and Total Harmonic Distortion (THD) performance can be improved as needed by using a larger shift register or additional harmonic filtering to meet the applicable specifications. This paper re-examines this approach and provides additional guidance on how to choose the resistor network to optimize THD using the standard EIA component values available. Simulation is used to verify results.

2 The Davies Generator

Figure 2-1 shows a simplified configuration of a 6-bit Johnson counter and related resistors to form a stepped-sinusoid output. Careful selection of the resistor values maps each state of the Johnson counter onto a point of the cosine function. As the Johnson counter is clocked through the states, a stepped sinusoid appears at the amplifier output. Extending the length of the shift register or using additional harmonic filtering (not shown) improves harmonic distortion performance.



Output harmonic filter not shown.

Figure 2-1. A 6-bit Johnson Counter and Resistors Form a Davies Sinusoidal Generator

A Johnson counter is a type of ring counter commonly used for state machines or clock division and must be properly reset at power up. Using a common clock, for each clock pulse the bit pattern shifts right with the output of the rightmost flip-flop inverted (or the output used if available) and fed back to the input of the shift register. This counter can be clocked relatively fast since the only propagation delay involved is from CLK to Q or $\overline{Q}$, whichever is slower.

Table 2-1 shows the repeating bit pattern of a 6-bit Johnson counter as the counter evolves over 12 clock cycles starting from a reset state. Twelve clock pulses sequence a 6-bit counter through all desired states.

Table 2-1. Bit Pattern of a 6-bit Johnson Counter While Clocked Through States

CLK	Q0	Q1	Q2	Q3	Q4	Q5
Reset	**0**	**0**	**0**	**0**	**0**	**0**
↑	1	0	0	0	0	0
↑	1	1	0	0	0	0
↑	1	1	1	0	0	0
↑	1	1	1	1	0	0
↑	1	1	1	1	1	0
↑	1	1	1	1	1	1
↑	0	1	1	1	1	1
↑	0	0	1	1	1	1
↑	0	0	0	1	1	1
↑	0	0	0	0	1	1
↑	0	0	0	0	0	1
↑	0	0	0	0	0	0

A counter of length N completes a full count cycle every 2 × N clock edges so the sinusoidal output frequency is determined with Equation 1.

$$F_{out} = \frac{F_{CLK}}{2N} \quad (1)$$

This counter only uses a fraction of the possible states available from the flip-flops. See Appendix B for important details regarding unused flip-flop states and how to avoid them.

Referring back to Figure 2-1, each resistor contributes a weighted current into the virtual ground node at the op amp, summing to I *I I*. Note how the resistor values are used in *pairs* (for an even length register). For symmetry reasons, assume the outputs of the flip-flops are represented by ±1-V logic levels (rather than binary 1 or 0) so each pair of R_i resistors contributes $+\frac{2V}{R_i}$, $-\frac{2V}{R_i}$, or 0 current toward I depending on the state of the counter. For a counter of even length, the ideal normalized resistor values are computed as Equation 2.

$$R_i = \frac{1\ \Omega}{\sin\left(\frac{\pi}{2N}\right)} \times \frac{1}{\sin\left(\frac{\pi}{2N}(2i+1)\right)} \; for\ 0 \le i \le \frac{N}{2} - 1 \tag{2}$$

For an odd length register (use Equation 3).

$$R_i = \frac{1\ \Omega}{sin\left(\frac{\pi}{2N}\right)} \times \frac{1}{sin\left(\frac{\pi}{2N}(2i+1)\right)} \; for\ 0 \le i \le \frac{N-1}{2} - 1 \tag{3}$$

The middle resistor is shown in Equation 4.

$$R\frac{N-1}{2} = \frac{1\ \Omega}{cos\left(\pi\frac{N-1}{2N}\right)} \tag{4}$$

See Appendix A for derivations of Equation 2 through Equation 4. Table 2-2 summarizes these values for registers up to length 16. Given the standard MSI devices available, of particular interest are register lengths 4, 6, 8, and 16. Any even-length register can also produce quadrature output. For applications requiring three-phase output, register lengths 6, 9, and 12 are useful. Registers of lengths 6 and 12 can produce both three-phase and quadrature output. Notice the parallel combination of all resistors in a given array is 1 Ω.

Table 2-2. Normalized Resistor Array Values for a Davies Generator Having Various Shift Register Lengths

Length	Ideal $R_i = 1/G_i$, Normalized to 1 Ω							
N	R_0	R_1	R_2	R_3	R_4	R_5	R_6	R_7
1	1.000							
2	2.000							
3	4.000	2.000						
4	6.828	2.828						
5	10.472	4.000	3.236					
6	14.928	5.464	4.000					
7	20.196	7.208	4.988	4.494				
8	26.274	9.226	6.165	5.226				
9	33.163	11.518	7.518	6.128	5.759			
10	40.863	14.081	9.040	7.174	6.472			
11	49.374	16.915	10.730	8.353	7.323	7.027		
12	58.695	20.020	12.585	9.657	8.293	7.727		
13	68.827	23.396	14.604	11.084	9.369	8.545	8.296	
14	79.770	27.042	16.787	12.631	10.548	9.462	8.988	
15	91.523	30.959	19.134	14.297	11.825	10.472	9.780	9.567
16	104.087	35.146	21.643	16.082	13.198	11.568	10.661	10.252

3 Optimizing Standard Resistance Values for THD Performance

The ideal resistances of Table 2-2 usually cannot be implemented directly with standard EIA-series values. Any deviation from an ideal value results in a systematic output error that deteriorates THD performance. This is similar to THD degradation when using a DAC having imperfect integral non-linearity (INL) characteristics. The values in Table 2-2 show that the resistors in the center of the shift register, having the smallest values, contribute the most current and the output is most sensitive to errors in these values.

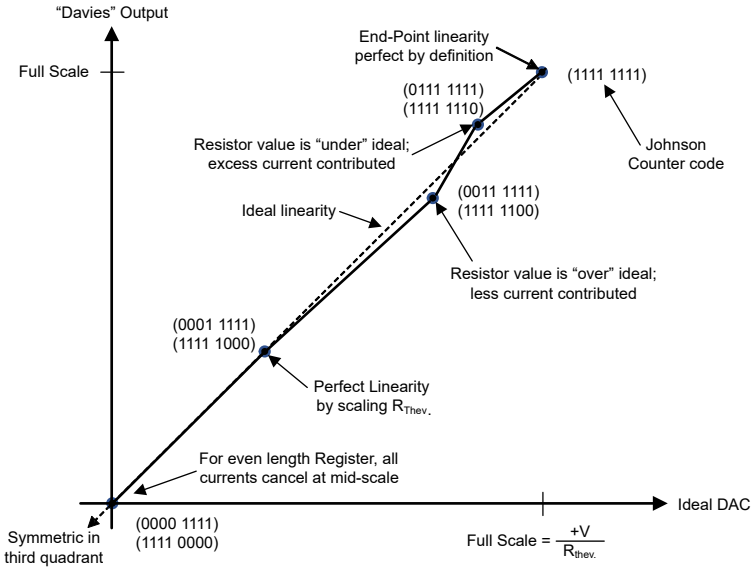
Resistance error consists of systematic and random components. Systematic error is created foremost by selecting a non-ideal value and secondarily by the non-zero output resistance of the flip-flops. Random error is primarily due to variation related to tolerance, but recall all resistors in even-length registers and most in odd-length registers are used in pairs. This is fortunate because resistors are commonly fabricated in the same lot and taken from the same reel during manufacturing to be well-correlated (though this is not always the case) and can result in better-than-expected current cancellation at the output node. For this reason, if a resistor needs replacement always replace both the resistor and the mate of the resistor with well-matched parts.

Since the middle-most resistor pair ($R\frac{N}{2}-1$ for even-length registers) carries the heaviest weight, choose this value first to coincide with a standard value by scaling the overall output Thevenin resistance slightly. The remaining resistors are calculated using this revised value working from the middle outward following an algorithm to minimize accumulated error.

For example, suppose an 8-bit shift register is used and a Thevenin output resistance of about 600 Ω is desired. From Table 2-1, the ideal middle resistor pair value is 5.226 × 600 Ω ≈ 3136 Ω. The nearest EIA-E96 (1%) value is 3.16 kΩ. By scaling the overall Thevenin resistance to 604.6 Ω, the systematic error contribution of these middle resistors is eliminated with < 1% system-level impact.

This revised Thevenin value is now used to calculate the remaining values using the following *over-under* (or *under-over*) algorithm to minimize accumulating errors. Continuing the example working outward from the middle, the next pair value is 6.165 × 604.6 Ω ≈ 3727 Ω. The nearest E96 value is 3.74 kΩ (+0.35%). Since this value is *over* the ideal value, the next resistor is chosen *under* the ideal to compensate. Moving outward again, the next resistor value is 9.226 × 604.6 Ω ≈ 5578 Ω. The nearest E96 value that is *under* (since the previous was *over*) is 5.49 kΩ (–1.58%). The outermost pair is then 26.274 × 604.6 Ω ≈ 15.885 kΩ, and the nearest E96 value that is *over* is 16.2 kΩ (+1.98%). The final Thevenin output resistance using these E96 values is ≈ 604.1 Ω; within 1% of the original design goal and improves linearity as best possible throughout the states of the counter using standard values.

This *over-under* selection of values skews the harmonic content contributed by resistor selection away from lower-order harmonics and toward higher orders that are easier to eliminate with filtering. Figure 3-1 shows how this algorithm helps maintain linearity through the various states of the Johnson counter as compared to an ideal DAC line.



Not to scale. Does not include random resistor variation.

Figure 3-1. Deviation From Absolute Linearity Due to Selecting Standard-Series Values Using *Over-Under* Algorithm

The prior example ignores flip-flop output resistance effects, but an enhanced example that compensates for this is found in Section 4.

4 Simulation Examples

Using the values from Section 3 and assuming no random resistor variation, the following TINA-TI SPICE simulation of Figure 4-1 based on the SN74HCS164 shift register demonstrates the upper limit of THD performance while using a realistic model of the shift register but neglecting the output resistance. Using 0-V, +5-V logic levels as shown results in a common-mode DC offset of 2.5 V in the output. Depending on the application, subsequent circuit stages can require AC coupling or some other method to remove the offset if it is undesirable. The additional 1-kHz square-wave source shown is used as a reference to sanity-check the simulated THD estimates since the Fourier series is well known. The scaled mid-supply common-mode voltage, VCM, provides the virtual ground that the op amp of Figure 2-1 otherwise provides.

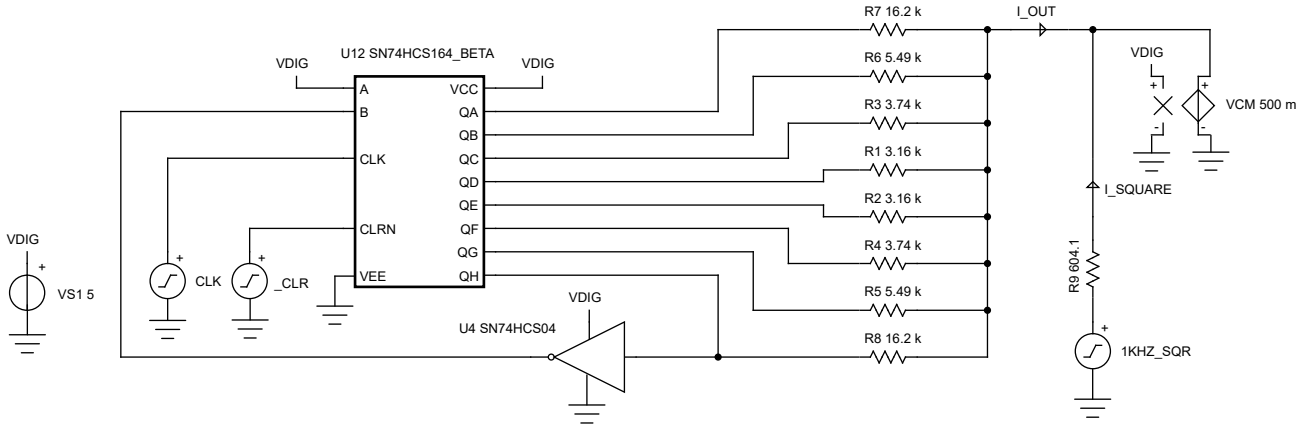
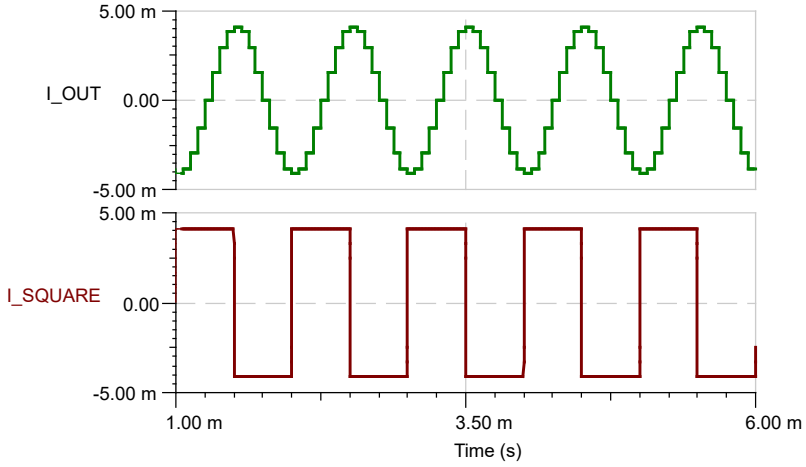


Figure 4-1. Simulation Schematic of MSI Logic Based "Davies" Generator With Square Wave Reference Source for THD Comparison

Clocking the circuit at 16 kHz results in an 8 × oversampled 1-kHz stepped-sinusoidal current into the virtual ground node, along with the reference square wave current.



Transient Simulation Results of Figure 4-1.

Figure 4-2. Transient Simulation Results Previous Image Showing Stepped Sinusoid and Square Wave Reference Waveforms

From within the TINA-TI diagram window, each curve is selected and a Fourier analysis estimates THD. As a sampled data system, only harmonics in the first Nyquist zone are considered and higher Nyquist zones ignored. This indicates that even without harmonic filtering < 0.17% THD is achieved, see Figure 4-3 and Figure 4-4.

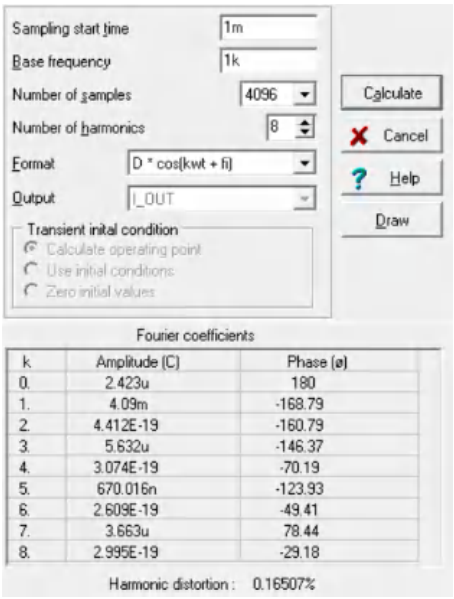


Figure 4-3. Simulated THD Results of Stepped Sinusoid Compared to Reference Square Wave

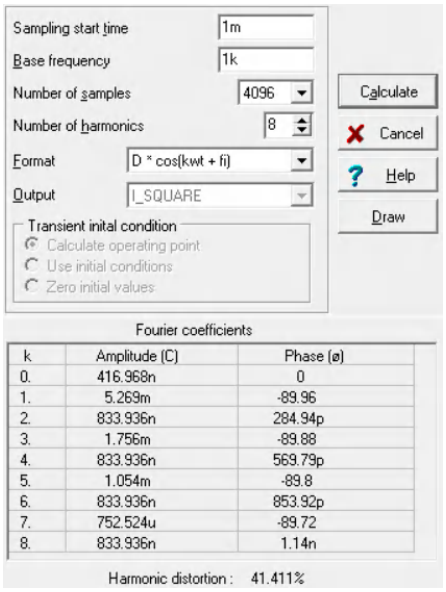


Figure 4-4. Simulated THD Results of Stepped Sinusoid Which Shows > 47-dB Improvement in 3rd Harmonic Suppression

The Fourier expansion of an ideal square wave is $y(t) = \frac{4}{\pi}\left(sin(\omega t) + \frac{1}{3}sin(3\omega t) + \frac{1}{5}sin(5\omega t) + \cdots\right)$ where $\omega = 2\pi f_O$. From this expansion it is clear the ratio of the 3rd harmonic to the fundamental is 1/3 (–9.54 dB) and verified in simulation in Figure 4-4. This indicates the TINA-TI THD computation appears correct. The 3rd harmonic of the stepped sinusoid is –57.2 dB relative to the fundamental, a > 47-dB improvement over the square wave.

5 Compensating for Shift Register Output Resistance

The *SN74HCS164 8-Bit Parallel-Out Serial Shift Registers With Schmitt-Trigger Inputs* data sheet provides insight into the output resistance of the flip-flops, with the output driver specifications shown in Figure 5-1.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

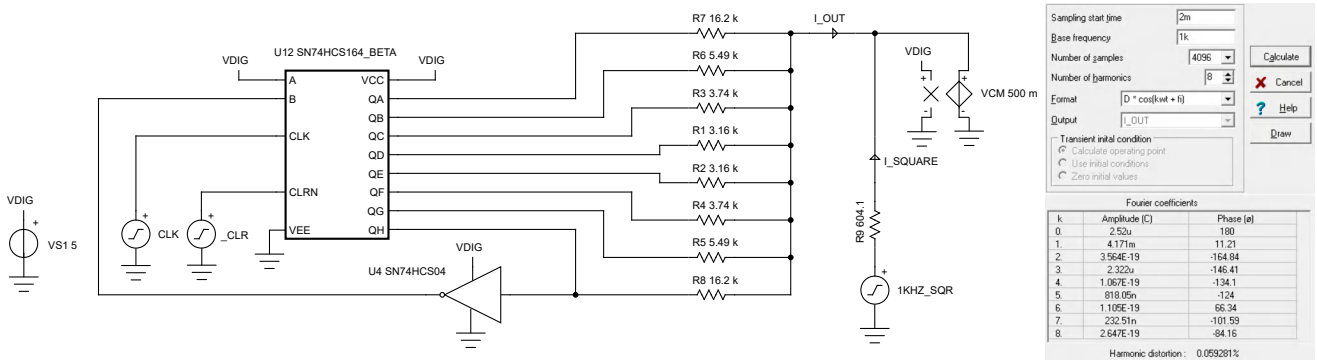
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4.0	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	

Register, R_O appears to be ≈ 31.7 Ω sourcing or sinking with V_{CC} = 4.5 V.

Figure 5-1. Output Drive Specification for the SN74HCS164 Shift Register

For sourcing current, the output resistance typically is (4.5 V – 4.3 V) / 0.006 A ≈ 33.3 Ω. For sinking current, the typical output resistance is 0.18 V / 0.006 A ≈ 30.0 Ω. The average output resistance is then approximately 31.7 Ω, which is about 1% of the value of the inner resistors of the previous idealized case; significant given the level of THD so far in question. Note that the worse case MIN, MAX values are dramatically different and result in much higher and more asymmetric output resistance values.

Recalculating the resistor network by assuming the previously discussed typical output resistance, the following network and an overall Thevenin output resistance of 597.6 Ω is determined. Using the same FFT analysis the THD for this compensated version is < 0.06%, and the 3rd harmonic is 65 dB below the fundamental. This is nearly a 8-dB improvement in 3rd harmonic performance compared to Figure 4-3, obtained simply by optimizing the resistor values to account for average output resistance.



THD calculation < 0.06% for simulation using these values.

Figure 5-2. Recalculated E96 Resistor Values Compensate for Average (About 31.7 Ω) Flip-Flop Output Resistance

Alternatively, the effects of output resistance can be reduced (though not eliminated) by simply scaling up the Thevenin resistance of the whole network – the previous example uses a relatively low Thevenin resistance to accentuate the impact of flip-flop resistance on THD.

6 Voltage-Mode Thevenin Equivalent

The examples shown so far have operated in a current-mode fashion, that is, driving current into a virtual ground. Due to the numerous parallel resistors involved, this mode of operation is easier to analyze (per Appendix A) than the voltage mode equivalent. Often it is useful to operate in voltage mode and a simple Thevenin transformation results in a voltage source having peak-to-peak amplitude of $V_{CC} – V_{EE}$ and an output resistance of the parallel combination of all the resistors, which is chosen as a design parameter. Figure 6-1 shows a voltage mode version and the open-circuit voltage response; notice the common mode DC offset of 2.5 V in the output.

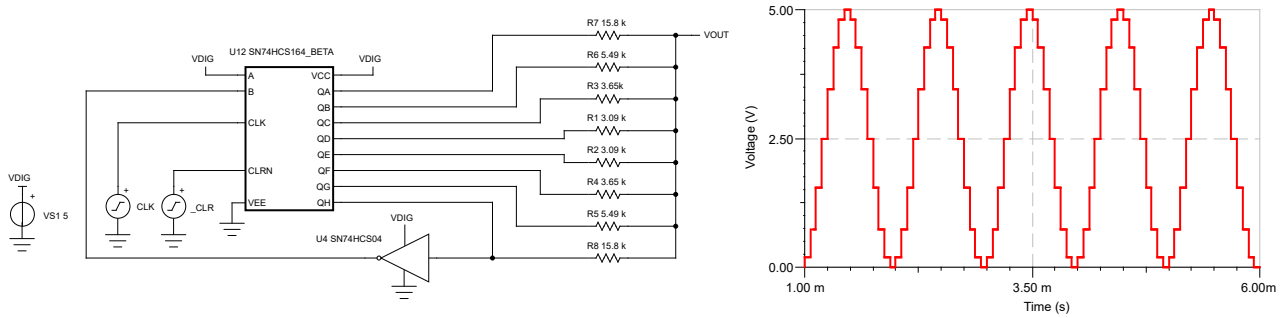


Figure 6-1. Voltage Mode Operation and Open-Circuit Output Transient Response, $R_{Thev.} \approx 597.6\ \Omega$

The Thevenin output resistance can be used as an element of a harmonic filter to further improve distortion performance as demonstrated in Section 7.

7 Harmonic Filtering

Using the voltage mode of operation, adding one capacitor to the output creates a simple first-order low-pass filter, having a corner frequency of $F_C = \frac{1}{2\pi R_{Thev}.C}$.

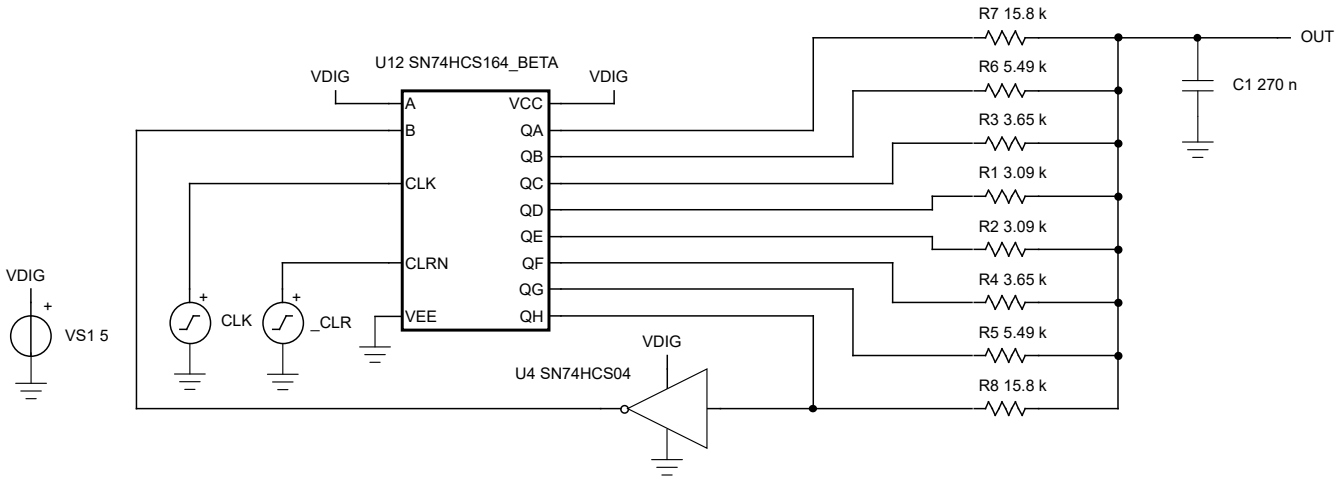


Figure 7-1. Added Output Capacitor for Simple 1st Order Harmonic Filter, $R_{Thev.} \approx 598\ \Omega$, $F_C \approx 1$ kHz

This smooths the steps of the waveform considerably and reduces THD by a factor of approximately 2 down to < 0.03%, see Figure 7-2, but a buffer is likely required to drive any subsequent circuit stage.

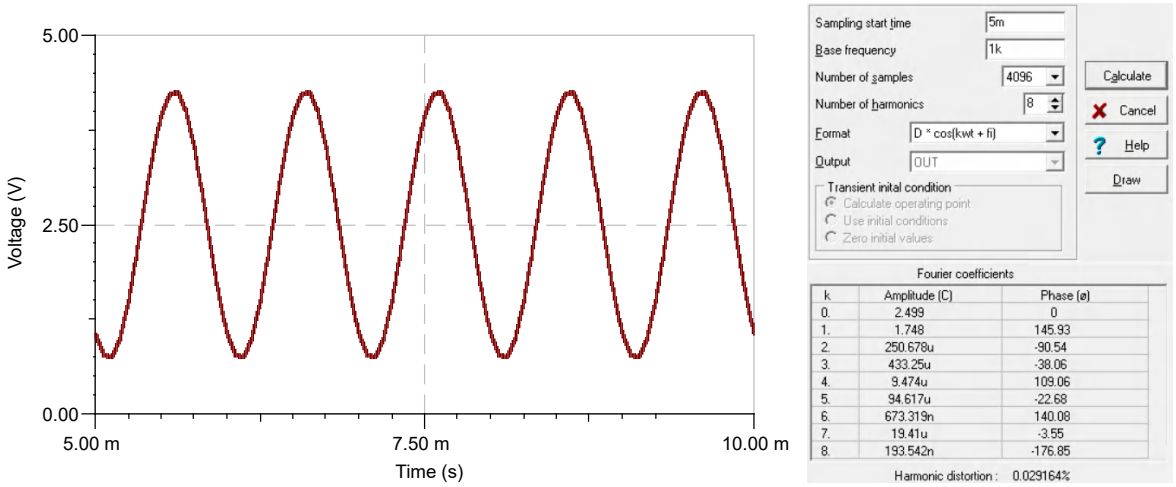


Figure 7-2. Waveform Reconstruction and THD Using Simple 1st Order Harmonic Filter

If a buffer is required, only an additional resistor (or two) and capacitor is needed to achieve a 2nd order filter. An active second-order Chebyshev harmonic filter having bandwidth of 1 kHz built using a high-quality op amp as shown in Figure 7-3, results in the response of Figure 7-4 while also providing a low impedance output for later stages. To minimize THD contribution from the op amp, the OPAx990 family is selected for superior linearity while the SPICE model is still realistic. Note that the bias shown for the op amp is symmetric about $V_{CM} \pm 5\ V$, where $V_{CM} = {}^{V_{DIG}}/_{2} = 2.5\ V$, and this common-mode voltage appears on the output as well.

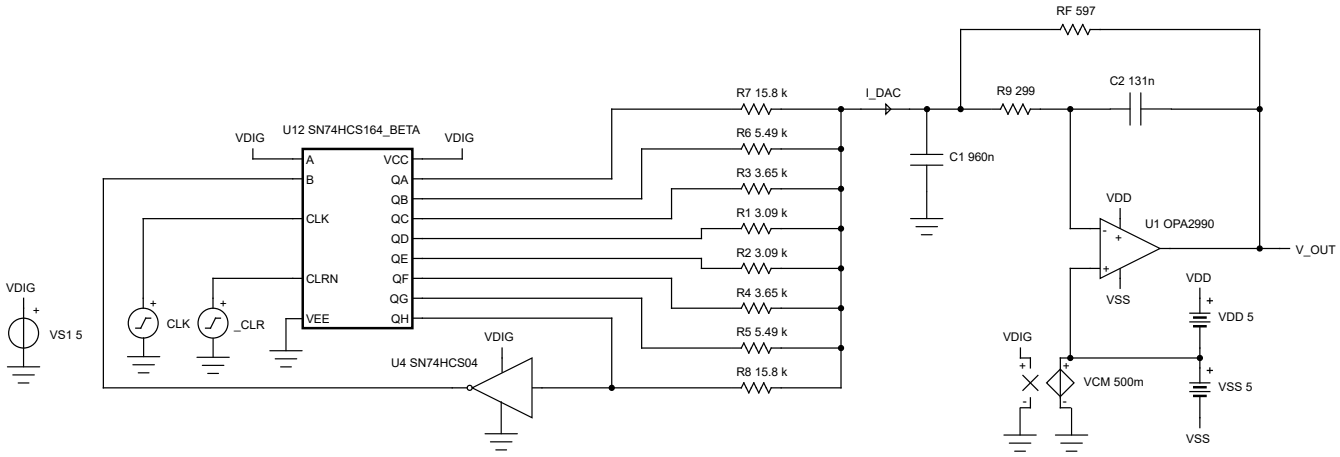


Figure 7-3. OPA2990 Series Op Amp Simulation Schematic to Perform 2nd Order Harmonic Filtering

The transient simulation results and corresponding Fourier analysis indicate simulated THD < 0.01%.

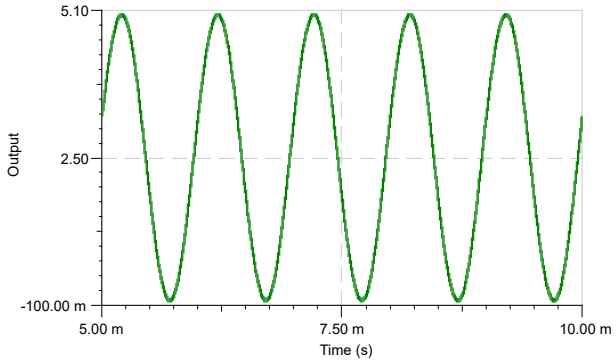


Figure 7-4. Transient Simulation Using the OPA2990 Series Op Amp in a 2nd Order Active Harmonic Filter

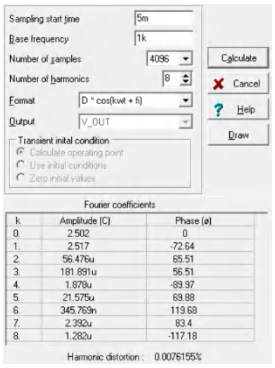


Figure 7-5. 2nd and 3rd Harmonics are < –82 dB, Relative to the Fundamental

These results represent *the most optimistic* scenario where all resistor pairs are matched, there is no random tolerance variation from the chosen E96 series values, and using an aggressive Chebyshev 2nd order filter response. Real-world THD performance degrades as actual resistor tolerance (±1% for E96) manifests, but additional harmonic filtering or extending the register length are trade-offs to consider for improving performance if needed. The Chebyshev response has some pass-band ripple and additional phase shift, but other filter responses are available. The first 5 ms of simulation is ignored because it takes this time for the 2nd order filter to settle into steady-state operation.

8 Tracking Harmonic Filter

For applications requiring a tunable frequency output, a fixed harmonic filter may not be suitable. A switch-capacitor low-pass filter such as the TLC04 or TLC14 may be clocked coherently with the shift register to provide a tuneable corner frequency that accurately tracks the output of the generator. For instance, the TLC04 provides a 4th order Butterworth response having cutoff frequency in the range of 0.1 Hz–30 kHz. The TLC04 is clocked at 50 × the desired corner frequency, while the TLC14 is clocked at 100 × the desired corner frequency. For example, for a 1-kHz output, a 64-kHz clock may drive the TLC04 for a corner frequency of 64 kHz / 50 = 1.28 kHz. Figure 8-1 shows the same clock is divided by 4 prior to clocking an 8-stage Johnson counter to generate a 1-kHz sinusoid.

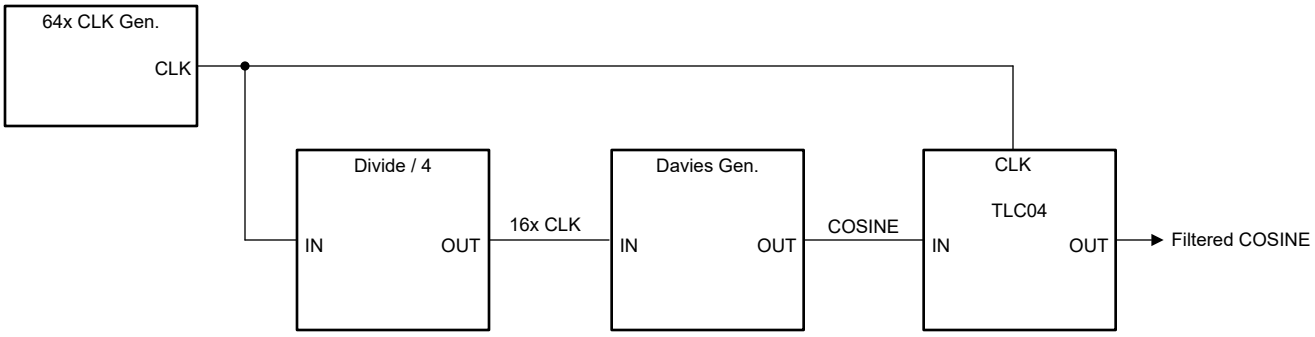
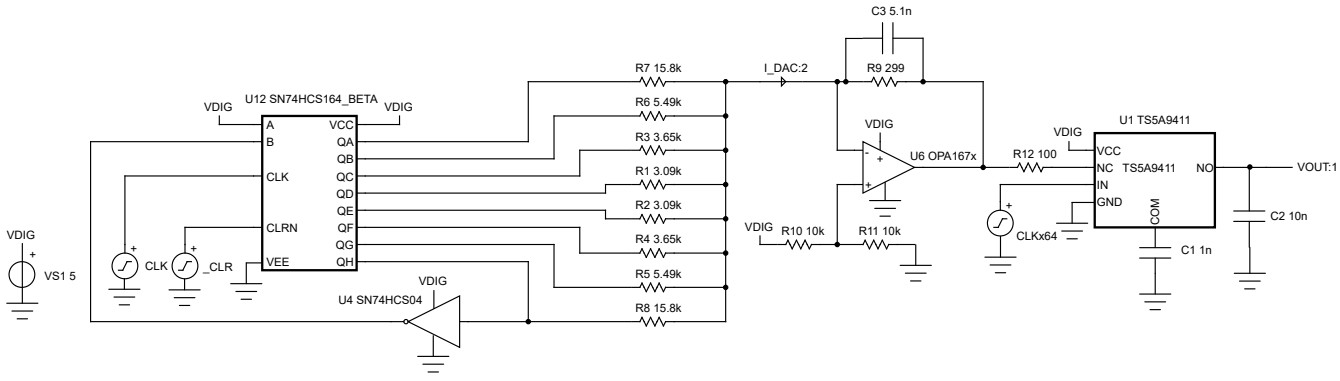


Figure 8-1. TLC04 Switched-Capacitor 4th Order Filter Used as a Tracking Filter to Remove Harmonics From the Output of the Davies Generator

This arrangement can be tuned to any frequency within the capability of the TLC04 simply by changing the input clock frequency. A simulation model of the TLC04 is not available, but a discrete switched capacitor filter simulation follows.

The primary drawback to switched capacitor type filters is the tendency to inject broadband noise into the output due the charge injection of the analog switches involved. Switched-capacitor filters may be constructed from discrete analog switches, but care must be taken regarding the charge-injection characteristics for the same concerns. For instance, the TS5A9411 has relatively low charge injection and is suitable for basic switched-capacitor applications.

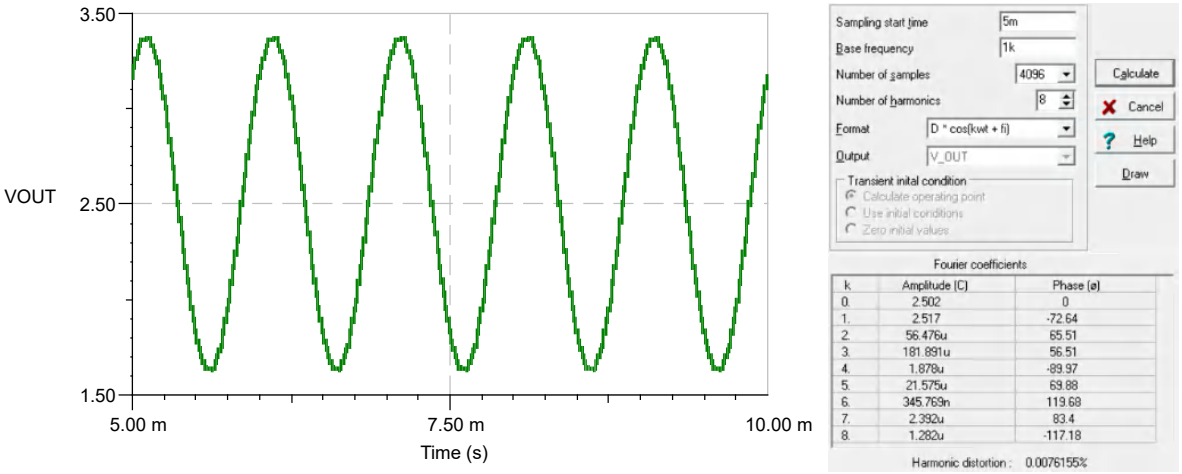
Figure 8-2 shows a 1st order tracking harmonic filter based on the OPA1671 and TS5A9411. The OPA1671 is a low-voltage amplifier having low noise (7 nV/$\sqrt{\text{Hz}}$), wide gain-bandwidth (13 MHz), and high-output drive characteristics that can easily drive the switched capacitor load.



Switched-capacitor filter clocked at 64 × sinusoidal output frequency.

Figure 8-2. Tunable Sinusoid Generator With Variable 1st Order Harmonic Filter Constructed From a DPST Analog Switch

Figure 8-3 shows the waveform and THD performance.



The harmonic filter is constructed from a discrete DPST analog switch, THD ≈ 0.025%

Figure 8-3. Simulation Results of Tunable Sinusoid Generator With Variable Switched-Capacitor 1st Order Harmonic Filter

Figure 8-4 shows a zoomed-in view of the waveform, the artifacts of the switched-capacitor filter are apparent.

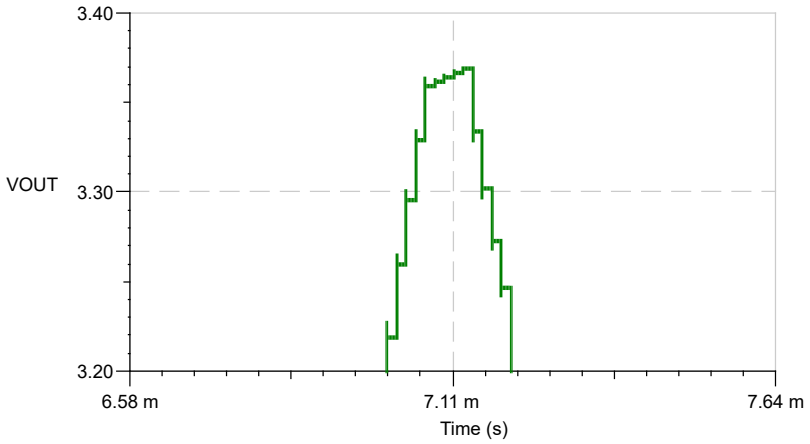


Figure 8-4. Zoom View of Waveform Reveals Artifacts of 1st Order Switched-Capacitor Harmonic Filter

The fuzzy-edges due to charge injection increases the system noise floor, and there is some slanting at the top of the curve. While these do not impact THD appreciably, it may cause other issues – nevertheless, this is a very simple solution for making an electronically-tunable harmonic filter.

9 Multiphase Output

Additional coherent phases may be derived from the same shift register. By driving additional resistor networks with delayed outputs 2, 3, 4 or more phased outputs can be created. The 6-bit Johnson counter is the shortest length that can create 2, 3, or 4 phase outputs, even simultaneously when driven as shown throughout Figure 8-1.

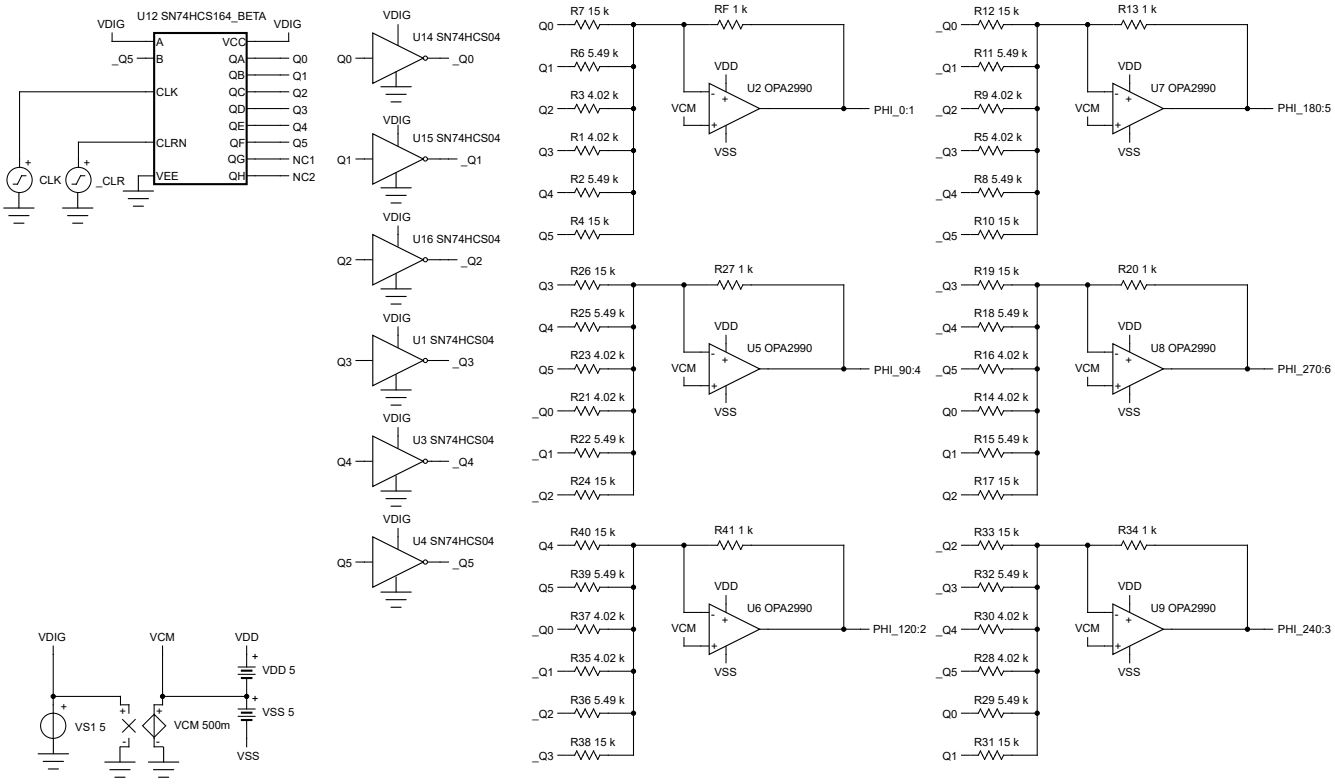
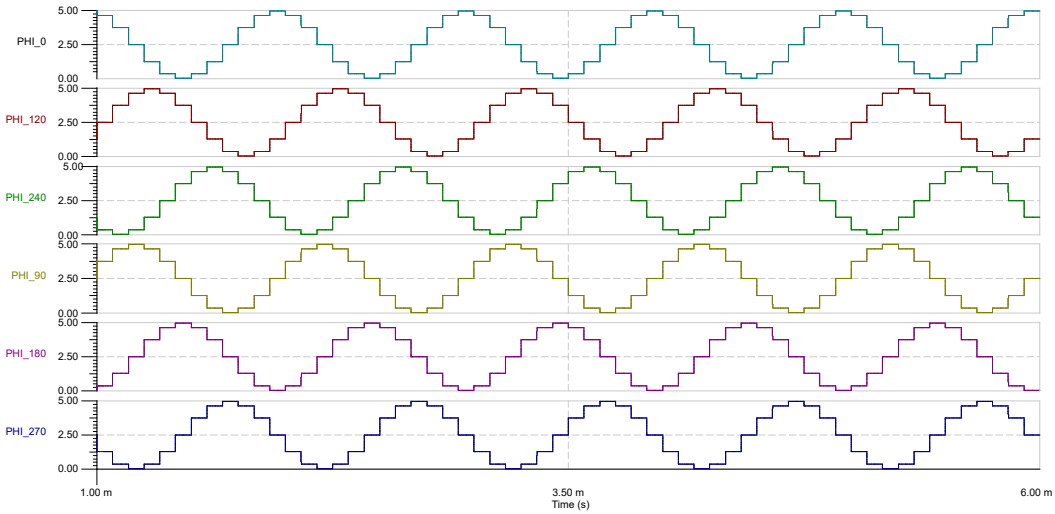


Figure 9-1. 6-bit Johnson Counter can Generate Various Useful Phase Relationships; 90°, 120°, 180°, 240°, 270°

The simulation results of Figure 8-1 are found in Figure 8-2. For simplicity, output filtering has been omitted from these results. Note that variation in harmonic filter components can cause unwanted phase shift between outputs.



See the *Voltage Mode Operation and Open-Circuit Output Transient Response* circuit in Figure 6-1.

Figure 9-2. Multiphase Output Simulation

10 Conclusion

Using Davies' approach is a straightforward method for generating sinusoids having consistent amplitude, frequency, and harmonic distortion. The approach can be tailored as needed for frequencies up through 10s of MHz using simple and inexpensive MSI shift register logic such as the HCS series from Texas Instruments. Starting first with a stepped sinusoid dramatically reduces the harmonic filtering required to obtain the final output, and the shift register can be lengthened as needed to further relax filtering requirements. Starting with a lookup table and applying a simple algorithm to choose from standard EIA series optimizes the THD performance without requiring custom value resistors. The output frequency can be changed virtually instantaneously, and tunable harmonic filters can be constructed from switched-capacitor networks for outputs having a wide spectrum of output. Multiphase outputs are also possible. These circuits are easily simulated in SPICE, though harmonic distortion predictions can be carefully scrutinized since only harmonics up through the Nyquist frequency can be included, and modeling limitations can mask the true non-linearities of the devices used.

11 Acknowledgment

Gratitude is expressed to the following:

- Emrys Maier (Texas Instruments) for providing the beta SN74HCS164 SPICE model
- John Griffith (Texas Instruments), John Kenny (Keysight Technologies), and Matthew D'Asaro (Seabird Scientific) for prompt and helpful rough draft reviews.

12 References

1. A. C. Davies, "*Digital Generation of Low-Frequency Sine Waves*", June 1969, IEEE Transactions on Instrumentation and Measurement, Vol. IM-18, No. 2, pp. 97-105.
2. D. Lancaster, "*Create Sinewaves Using Digital ICs*", November 1976, Radio-Electronics, Vol. 47, pp. 59-66.
3. R. R. Johnson, "*Electronic Counter*", US Patent 3030581, August 1953.
4. Texas Instruments, *SN74HCS164 8-Bit Parallel-Out Serial Shift Registers With Schmitt-Trigger Inputs* data sheet

A Analytical Solution for Resistance Network Values

Consider an even-length Johnson counter of length *N* driving weighted resistors (conductors, G_i) as shown into a current summing node at the inverting input of the op amp. For symmetry reasons assume the flip-flops output is ±1 V representing normalized high and low states, see Figure A-1.

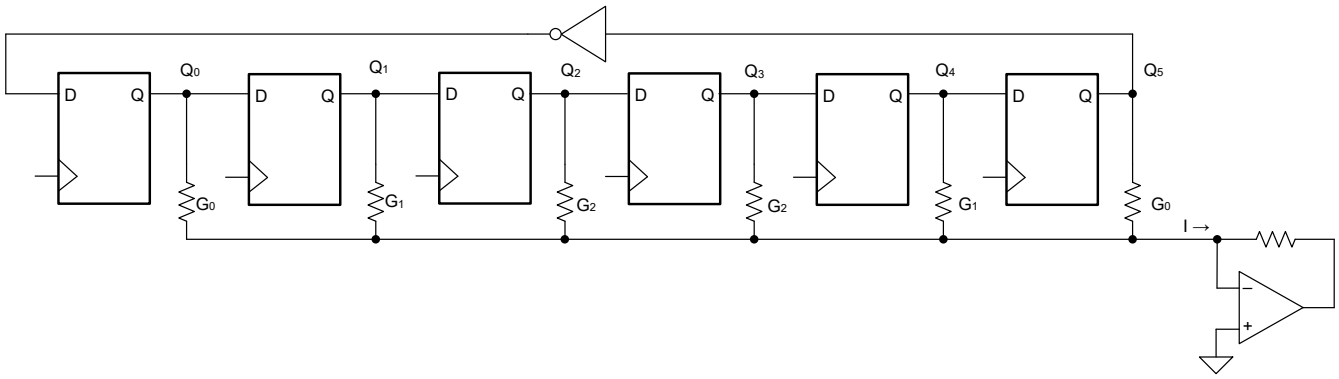


Figure A-1. Simplified Johnson Counter With Weighted Resistors Driving a Transconductance Amplifier

When all flip-flops are high (11…11), maximum positive current flows into the virtual ground at the op amp, corresponding to the peak of the cosine function. To normalize the overall Thevenin circuit conductance to 1S (1 Ω) let I_{PEAK} = 1 A. The contributions of the resistors are weighted to form the steps along the cosine waveform as follows in Figure A-2, summing to 1 A.

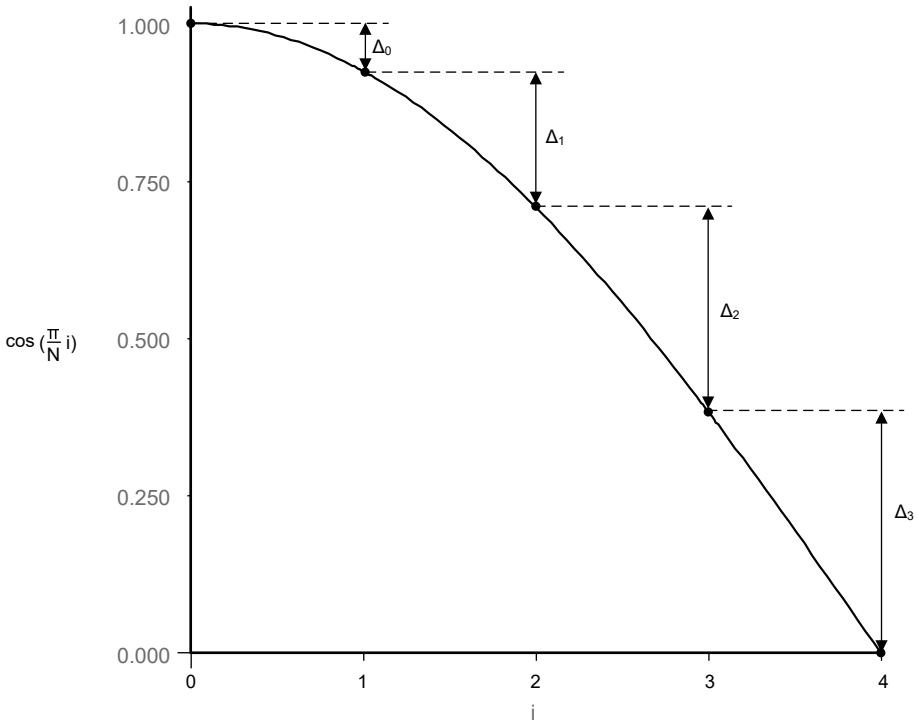


Figure A-2. Weighted Current Contributions of Each Pair of R_i Resistors sum up to 1 A (Normalized)

For each Δ_i when both G_i resistors are driven high by their respective flip-flops, see Equation 5.

$$\Delta_i = 2G_i = cos\left(\frac{\pi}{N}i\right) - cos\left(\frac{\pi}{N}(i+1)\right) \quad (5)$$

Using a trigonometric identity and simplifying Equation 5 yields Equation 6.

$$2G_i = \ -2\ sin\left(\frac{\pi}{2N}(2i+1)\right) sin\left(\frac{-\pi}{2N}\right) \rightarrow G_i = sin\left(\frac{\pi}{2N}(2i+1)\right) sin\left(\frac{\pi}{2N}\right) \quad (6)$$

Converting each conductance to a resistance,

$$R_i = \frac{1}{G_i} = \frac{1}{sin\left(\frac{\pi}{2N}\right)} \times \frac{1}{sin\left(\frac{\pi}{2N}(2i+1)\right)} \quad (7)$$

Recall R_i is normalized to 1 Ω; to get the desired overall Thevenin output resistance R_O, each resistor must be scaled by R_O, see Equation 8.

$$R_{i,\,denormalized} = \frac{R_O}{G_i} = \frac{R_O}{sin\left(\frac{\pi}{2N}\right)} \times \frac{1}{sin\left(\frac{\pi}{2N}(2i+1)\right)} \quad (8)$$

For an odd-length register, the value for the lone middle resistor is computed separately as Equation 9 and Equation 10 show.

$$G_{\frac{N-1}{2}} = cos\left(\frac{\pi}{N}\frac{N-1}{2}\right), for\ odd\ N \quad (9)$$

$$R_{\frac{N-1}{2},\ denormalized} = \frac{R_O}{G_{\frac{N-1}{2}}} = \frac{R_O}{cos\left(\pi\frac{N-1}{2N}\right)},\ for\ odd\ N \quad (10)$$

B Forbidden States of the Johnson Counter

Johnson counters have a subtle but potentially troublesome issue of unused states. A Johnson counter containing *N* flip-flops is a state machine having 2^N unique states of which only 2 × *N* are used, leaving 2^N – 2 × *N* unused. For an 8-bit register, that amounts to 240 unused states– the vast majority. If the Johnson counter somehow gets out of the desired cycle due to a glitch (cosmic ray, power supply noise, bad start-up conditions, and so forth) additional logic is required for recovery; otherwise the counter remains forever locked out of the desired cycle, only clocking through unused states and producing bad output. The additional octal input NAND gate and one-shot timer shown in Figure B-1 demonstrate one relatively easy way using common parts to detect and correct this fault condition within a few output cycles. As a side benefit, during normal operation the octal NAND gate generates a falling edge coinciding with 0° of the cosine function. This sync pulse extends the output of the ‘123 one-shot indefinitely so long as the Johnson counter is operating correctly. If the sync pulse goes missing beyond the timeout of the one-shot, the output goes low and 1s are clocked into the shift register via the 2-input NAND until the circuit is reset back to the correct pattern.

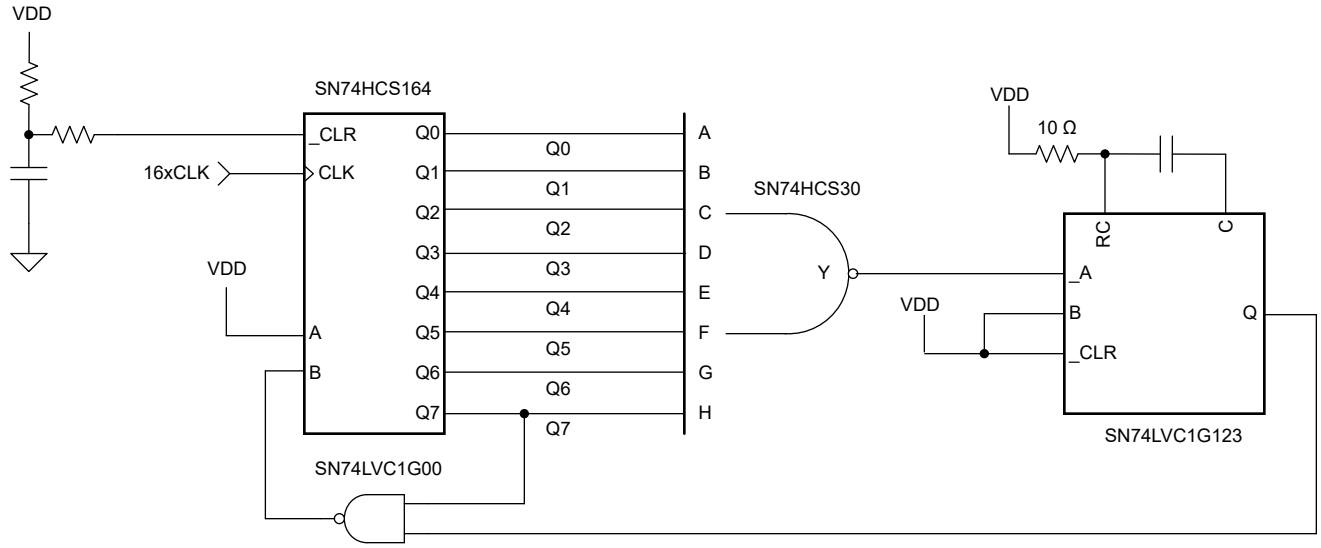


Figure B-1. Additional Logic and Timer to Rescue the Johnson Counter From Unused States

The new HCS series of MSI logic gates feature Schmitt triggers on all inputs, including _CLR. This allows for easy RC power-on reset as shown in Figure B-1. The inline resistor on the _CLR signal limits the current from the reset capacitor through the ESD structures of the logic gate when VDD is powered down quickly.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265