Application Note

Bidirectional Topologies for the INA901-SP

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ABSTRACT

This paper discusses topologies that allow for the unidirectional INA901-SP in a bidirectional application. It also discusses potential pitfalls that must be considered when designing such a circuit, and provides analysis and data on how calibration can improve application performance.

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Trademark

1 Theory of Operation

In aerospace and defense, current sensing can be implemented in a variety of different applications. Whether it be for overcurrent and undercurrent detection for protection of systems, or monitoring current for telemetry for satellites and power supervision, or closed loop control in applications such as motors, current sensing is often a needed function. Often in these space-grade applications, it is necessary to measure currents in both directions thus needing a bidirectional device to accomplish the design goal.

For applications where only low-orbit space requirements are needed, the INA240-SEP device provides bidirectional current sensing capabilities with a single integrated circuit (IC). The INA240-SEP is Single Event Latch-up (SEL) immune to 42 MeV-cm^2/mg at 125°C and total ionizing dose (TID) RLAT for every wafer lot of up to 20 krad(Si). Where higher levels of radiation requirements are needed for higher orbit applications, the INA901-SP is Single Event Latch-up (SEL) Immune to 75 MeV-cm^2/mg at 125°C and Radiation Hardness Assured (RHA) 50 krad(Si) at Low Dose Rate. However, while the INA240-SEP supports bidirectional functionality, the INA901-SP only supports unidirectional sensing, and thus a challenge arises when bidirectional support is needed, but at a higher radiation hardness.

Since the INA901-SP is unidirectional, this application note explores how to design bidirectional circuits using an INA901 and additional components to achieve either a low-side or high-side implementation, and the associated tradeoffs with such a design.

2 Low-Side Implementation

A straightforward design process for the INA901 is presented in the *Space-Grade, 50-krad, Low-Side Bidirectional Current Sense Monitor* application brief. Use this application note to create the needed reference voltage. When designing with the INA901, ensure that the sense voltage is maintained above 20 mV, because the optimal performance of the INA901 is achieved when operation occurs above this condition.

The design begins with the need to establish an offset point similar to that provided by the REF pins of a bidirectional current amplifier. Under normal unidirectional conditions, resistors on the sense lines are typically discouraged, due to the fact that these resistors can add an offset to the measurement; this results in additional gain error due to discrepancies between the voltage produced on the shunt, and the voltage ultimately observed at the pins of the amplifier. It is possible; however, to use this as a design advantage, and purposefully produce a known offset about which the shunt voltage will swing.

The circuit demonstrates this by creating a precise offset current that flows across an offset resistor, shown as R1 in INA901-SP Low Side Bidirectional Implementation. For the low-side implementation, as the common mode of the inputs is approximately GND, then the needed current can easily be created via a pathway off of supply, using a second resistor, R2, to establish the needed current value. In this topology, it must be noted that the current created is modified by the input bias current, denoted in the schematic as "Ib+", as this is still needed by the INA901 to maintain linear operation. The sense voltage, $V_{SENSE,}$ will also cause I_{OFFSET} to deviate slightly, and therefore slightly shift the offset point over the range of measurement. These changes are small enough; however, that they are still within an acceptable margin of error. Disregarding the bias current, Equation 1 shows that the calculated offset may be approximated as the actual offset current seen by R1.

$$I_{OFFSET,\ CALC} = I_{OFFSET,\ ACTUAL} = I_{OFFSET} \tag{1}$$

The value attained relaxes calculation. Begin by choosing desired values for R1 and R2 to establish the desired offset. With the approximation that the effects of the input bias currents are negligible, these resistors provide two potential variables to write linear equations to achieve the desired reference point. This is established in Equation 2 through Equation 4:

$$I_{OFFSET} = \frac{V_S - V_{IN+}}{R2} \tag{2}$$

$$V_{SENSE,\ OFFSET} = I_{OFFSET} \times R1 \tag{3}$$

$$V_{OUT,\ REF} = V_{SENSE,\ OFFSET} \times GAIN \tag{4}$$

The established referred to input (RTI) offset from Equation 2 is presented to the pins of the INA901 as a relatively constant positive voltage which produces an offset, and the voltage created on V_{SHUNT} will either add or subtract from this quantity, based on the direction of current flow. This offset is then acted on by Equation 3, producing the actual output quantity of REF on the output of the INA901.

As an example, consider a system measuring –7.5 A to 7.5 A bidirectionally. Choosing a 10-mΩ shunt, the expected range of V_{SHUNT} produced will ideally be –75 mV to 75 mV. To this range of values, add an appropriate offset voltage, referred to the input. It is important to note that V_{SHUNT} does not equal V_{SENSE} here, as V_{SENSE} (the voltage seen by the sense pins of the INA901 and ultimately gained by the amplifier) will be modified by the created offset voltage.

Utilizing Equation 2 through Equation 4, the values of I_{OFFSET} = 2.5 mA (R2 = 2 kΩ, from the 5-V supply node), and R1 = 39.2 Ω were selected to produce a 1.96-V offset. The initial design conceptualized a 2-V offset from a 40-Ω resistor, but the closest commercially available resistor option is 39.2 Ω. Additional combinations may result in more numerically convenient options if investigated, or custom resistors may be sought at an increased cost of design. From Equation 2, the RTI offset is calculated using Equation 5.

$$V_{SENSE,\ OFFSET} = I_{OFFSET} \times R1 = 98\ mV \tag{5}$$

Applying this voltage to the previously-designed input range, the expected design should now produce a V_{SENSE} range of 23 mV to 173 mV, or 460 mV to 3.46 V at the output of the INA901, assuming an ideal gain of 20

V/V. Note that this range was designed to ensure V_{SENSE} > 20 mV at the lower end, optimizing the operating use-cases of the INA901. INA901-SP Low Side Bidirectional Implementation shows the completed design schematic.

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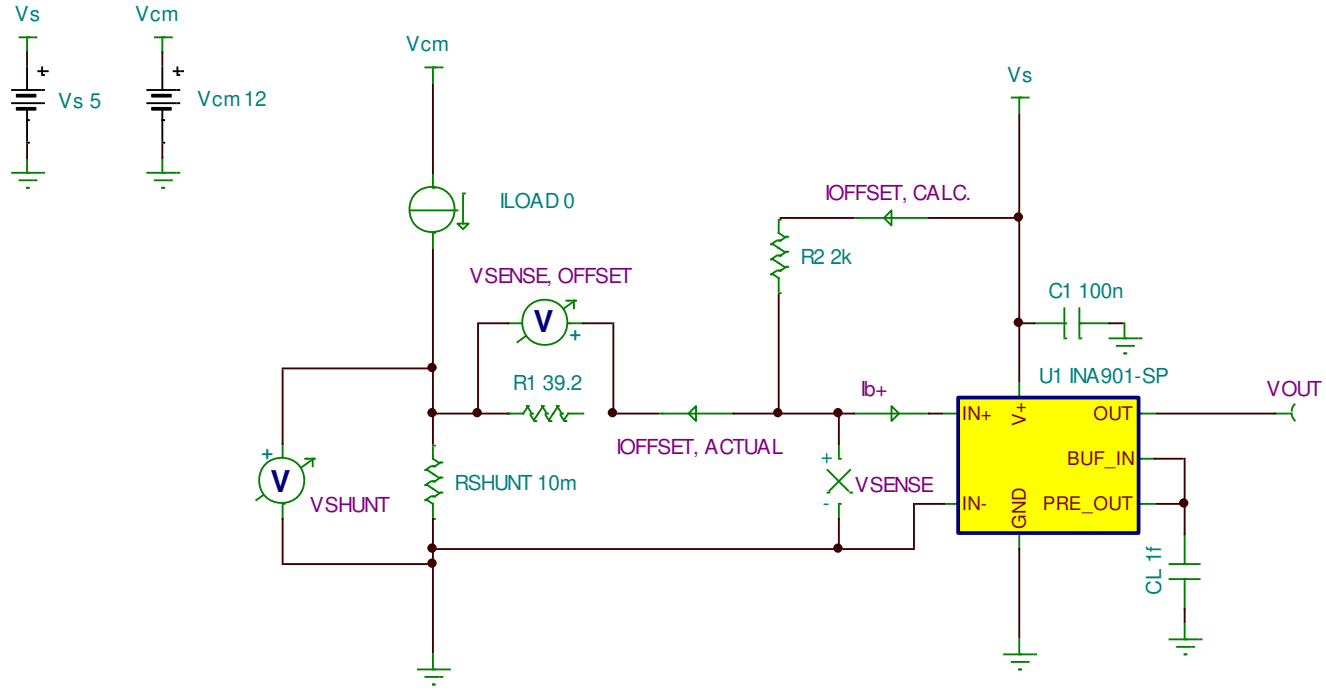

Figure 2-1. INA901-SP Low-Side Bidirectional Implementation

In this configuration, an error will occur as V_{SHUNT} voltage increases. Note that the offset current is established via the difference between the supply voltage, and the voltage on the IN+ node as per Equation 1. IN+ is not a true 0 V, but will fluctuate as V_{SHUNT} increases or decreases, resulting in additional error. INA901-SP Low Side Simulation Results shows simulated results and values for this design.

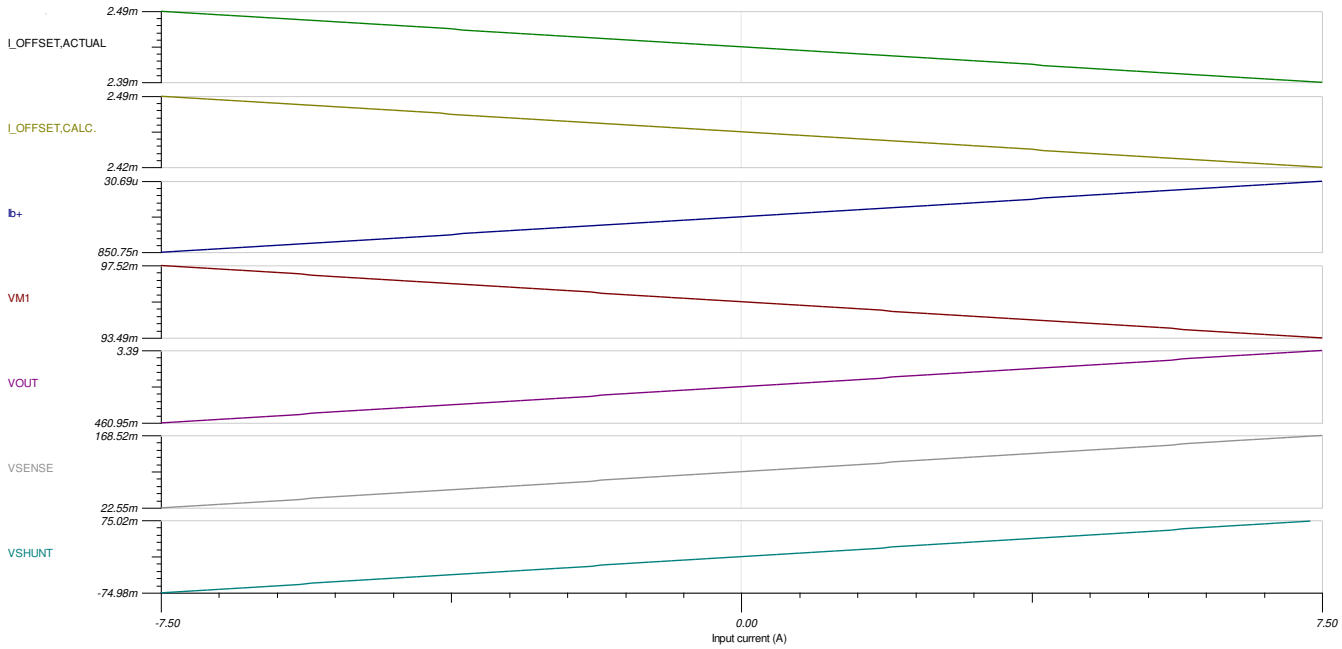

Figure 2-2. INA901-SP Low-Side Simulation Results

Note that these curves are captured at ideal resistor values for R1 and R2, and resistor value tolerance, even at room temperature, will inject additional error between simulated and real results. The INA901 TINA-TI SPICE model also provides the ability to examine the input bias currents over load current range of the device.

From the TINA simulation data and schematic, a few constraints can be observed for this implementation:

1. This topology cannot be implemented on the high side where $V_{CM} > V_S$, as the current must flow toward the IN+ pin to achieve the necessary offset. Therefore, the common-mode voltage of the IN+ pin must be less than that of the supply voltage to ensure valid operation.
2. The offset current created by Equation 1 shows that, as a consequence, the offset voltage point deviates slightly with the sense voltage, producing a linear error along with the sense voltage.
3. Because this is a low-side implementation, the trade-offs that come with measuring on the low side are in effect here. This includes the inability of the load to detect ground faults.

This design was then prototyped for real-world comparison. Table 2-1 through Table 2-3 display data captured via this topology at ambient temperature, as well as temperature extremes of –55°C and 125°C. For these data sets, E96 resistors of 0.1% tolerance were utilized, with a temperature coefficient of 50 ppm/°C. More tightly grouped curves may be obtained by choosing resistors with more stringent temperature drift specifications.

Table 2-1. INA901 Low-Side Results – Test Conditions: V_{CM} = 0 V, V_S = 5 V, T = 25°C

I_{LOAD} (A)	V_{SHUNT}, Meas. (V)	Output Voltage, Meas. Ideal (V)	V_{OUT}, Meas. (V)	Error (%)	V_{OUT}, Calibrated (V)	Error, Calibrated (%)
–7.5	–0.074997	0.46006	0.42527	–7.56%	0.45701	–0.66%
–6.25	–0.062498	0.71004	0.67569	–4.84%	0.70743	–0.37%
–5	–0.049998	0.96004	0.92612	–3.53%	0.95786	–0.23%
–3.75	–0.037498	1.21004	1.17658	–2.77%	1.20832	–0.14%
–2.5	–0.024998	1.46004	1.4271	–2.26%	1.45884	–0.08%
–1.25	–0.012498	1.71004	1.6777	–1.89%	1.70944	–0.04%
0	0.000012	1.96024	1.9285	–1.62%	1.96024	0.00%
1.25	0.012512	2.21024	2.1743	–1.63%	2.20604	–0.19%
2.5	0.025012	2.46024	2.42	–1.64%	2.45174	–0.35%
3.75	0.037511	2.71022	2.6657	–1.64%	2.69744	–0.47%
5	0.05001	2.9602	2.9115	–1.65%	2.94324	–0.57%
6.25	0.062513	3.21026	3.1573	–1.65%	3.18904	–0.66%
7.5	0.075012	3.46024	3.403	–1.65%	3.43474	–0.74%

Table 2-2. INA901 Low-Side Results – Test Conditions: V_{CM} = 0 V, V_S = 5 V, T = 125°C

I_{LOAD} (A)	V_{SHUNT}, Meas. (V)	Output Voltage, Meas. Ideal (V)	V_{OUT}, Meas. (V)	Error (%)	V_{OUT}, Calibrated (V)	Error, Calibrated (%)
–7.5	–0.074998	0.46004	0.43285	–5.91%	0.46459	0.99%
–6.25	–0.062498	0.71004	0.68348	–3.74%	0.71522	0.73%
–5	–0.049999	0.96002	0.93382	–2.73%	0.96556	0.58%
–3.75	–0.037498	1.21004	1.1842	–2.14%	1.21594	0.49%
–2.5	–0.024998	1.46004	1.4346	–1.74%	1.46634	0.43%
–1.25	–0.012498	1.71004	1.6849	–1.47%	1.71664	0.39%
0	–0.000002	1.95996	1.9353	–1.26%	1.96704	0.36%
1.25	0.012506	2.21012	2.1815	–1.29%	2.21324	0.14%
2.5	0.025006	2.46012	2.427	–1.35%	2.45874	–0.06%
3.75	0.037506	2.71012	2.6727	–1.38%	2.70444	–0.21%
5	0.050007	2.96014	2.9182	–1.42%	2.94994	–0.34%
6.25	0.062506	3.21012	3.1638	–1.44%	3.19554	–0.45%
7.5	0.075006	3.46012	3.4094	–1.47%	3.44114	–0.55%

Table 2-3. INA901 Low-Side Results – Test Conditions: V_{CM} = 0 V, V_S = 5 V, T = –55°C

I_{LOAD} (A)	V_{SHUNT}, Meas. (V)	Output Voltage, Meas. Ideal (V)	V_{OUT}, Meas. (V)	Error (%)	V_{OUT}, Calibrated (V)	Error, Calibrated (%)
–7.5	–0.074999	0.46002	0.42959	–6.61%	0.46133	0.28%
–6.25	–0.062498	0.71004	0.68015	–4.21%	0.71189	0.26%
–5	–0.049998	0.96004	0.93083	–3.04%	0.96257	0.26%
–3.75	–0.037498	1.21004	1.1815	–2.36%	1.21324	0.26%
–2.5	–0.024998	1.46004	1.4322	–1.91%	1.46394	0.27%
–1.25	–0.012498	1.71004	1.6829	–1.59%	1.71464	0.27%
0	0.000006	1.96012	1.9339	–1.34%	1.96564	0.28%
1.25	0.012506	2.21012	2.1798	–1.37%	2.21154	0.06%
2.5	0.025006	2.46012	2.4257	–1.40%	2.45744	–0.11%
3.75	0.037505	2.7101	2.6715	–1.42%	2.70324	–0.25%
5	0.050006	2.96012	2.9174	–1.44%	2.94914	–0.37%
6.25	0.062506	3.21012	3.1632	–1.46%	3.19494	–0.47%
7.5	0.075007	3.46014	3.4092	–1.47%	3.44094	–0.55%

While this design allows bidirectional current sensing, the device remains a unidirectional device. This implies that one direction of sensing is more inaccurate than the other, as one direction drives the output stage towards its full scale range, where error is minimized against the gain error of the INA901, while the latter direction drives the device towards its referenced ground, and the inherent offset of the device applies additional error in this condition.

For use of such topologies, perform at least a one point calibration for optimal results. This is achieved in logic by capturing the true offset on the output created at the condition V_{SHUNT} = 0 V, and shifting the output curve data down to this calculated offset point. Table 2-1 through Table 2-3 provide data points captured pre-calibration, as well as expected error pre- and post-calibration. Observe in Figure 2-3, that by performing calibration, error can be kept to 1% or less for the entirety of the measurement range. Resistors with additional drift specification may help achieve even better results.

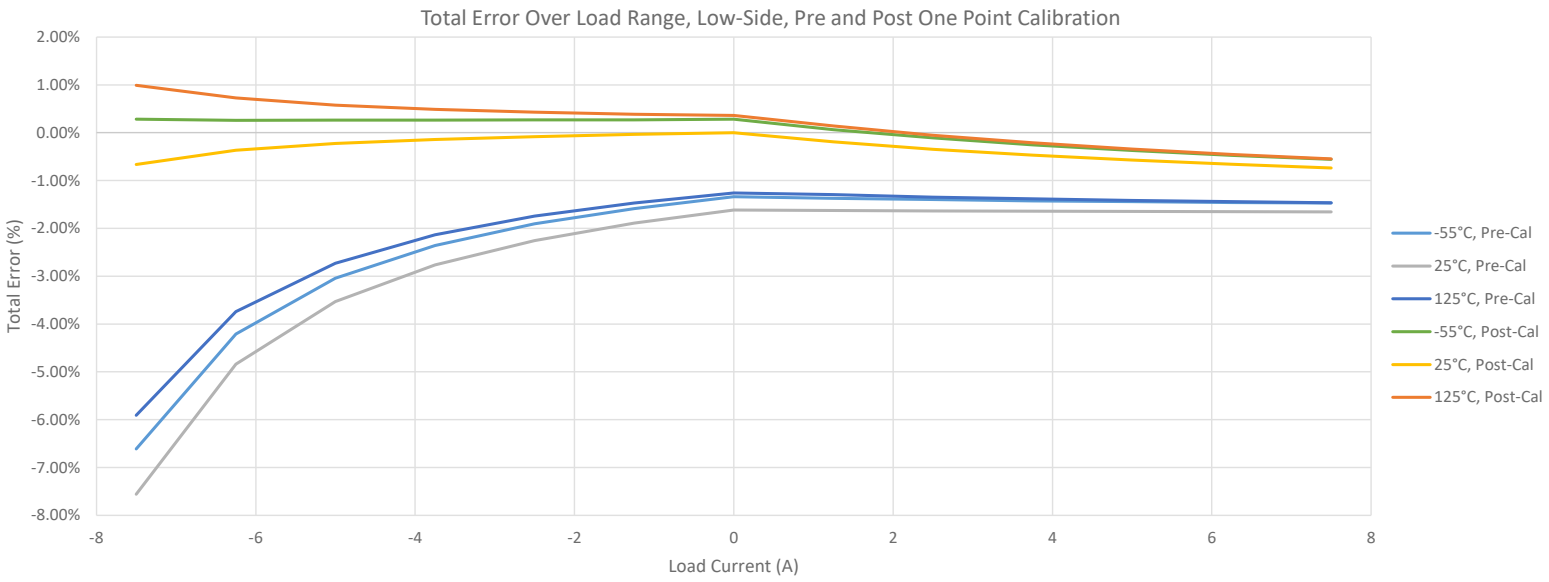

Figure 2-3. Low-Side, Bidirectional Error Over Range, Pre- and Post-Calibration

3 High-Side Implementation

From the successful model on the low side, an inverted analog of the previous circuit may be realized to also implement such a design on the high side. However, a new challenge is observed for this design: for the previous low-side design, current flows from the supply pin towards the common-mode voltage, which is held to approximately 0 V. For a high-side implementation, the current must flow in the same direction across a resistor populated on the IN– leg, which in this circumstance is from the common-mode voltage to the ground. If the intended common mode is to be held constant, then the design is trivial, and a simple resistor to GND may designed as in the low-side case. However, for high-side designs, this is rarely the case, and large swings in the common-mode voltage result in proportionally large swings to the current that produces the desired offset. This makes the design goal clear: a constant current source is needed, utilizing parts that are readily available for space applications.

To design a current sink on the IN– sense line, there are several potential topologies, but this is easily achievable with a TL1431-SP programmable reference and a corresponding BJT NPN transistor.

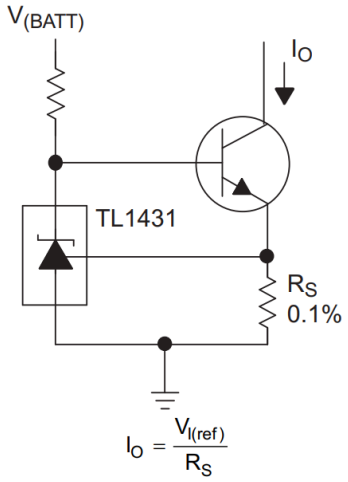

Figure 3-1. TL1431-SP Precision Constant Current Sink Schematic

As demonstrated in TL1431-SP Precision Constant Current Sink Schematic, this design uses a precision resistor to achieve the sink current needed. Conveniently, as the default reference of the TL1431-SP is 2.5 V, the offset current of the previous design can be recreated with a 1-kΩ resistor, for R_S.

$$I_{OFFSET} = \frac{V_{I,REF}}{Rs} = \frac{V_{I,REF}}{R2} = \frac{2.5\ V}{1\ k\Omega} = 2.5\ mA \quad (6)$$

The tradeoff to this design is that, as stated, the reference voltage of the TL1431-SP is 2.5 V, which means that the power dissipated across the chosen NPN transistor is:

$$P_{LOSS,\,NPN} = \left(V_{CM} - 2.5\ V\right) \times I_{OFFSET} \quad (7)$$

Note that the power dissipated in the BJT is directly proportional to the offset current, allowing an optimal point to be reached between power dissipated in the BJT and the offset created for the INA901. However, even in cases where the BJT power must be maximized, this power loss should be manageable. For the proposed design, even for valid common modes above the design case, the worst-case power dissipation is calculated to be:

$$P_{LOSS,\,NPN} = \left(V_{CM,\,WC} - 2.5\ V\right) \times I_{OFFSET} = \left(65\ V - 2.5\ V\right) \times 2.5\ mA = 156.25\ mW \quad (8)$$

The previous analysis also allows two additional observations. First, the NPN chosen for the application must be V_{CE} voltage rated for at least the common-mode voltage less 2.5 V, although an additional margin for potential common-mode transients is advised to provide robust performance and minimize potential failures. Second, similar to the low-side design, this shows that this circuit also has a limitation based on directionality of current, and is only suited for applications of V_{CM} > 2.5 V.

Similar to the low-side design, it is advised that the offset current be established such that the sense voltage of the INA901 is maintained above 20 mV to ensure optimal performance. From here, the analysis follows that of the low-side circuit, with the exception that the offset is created on the IN– leg of the amplifier.

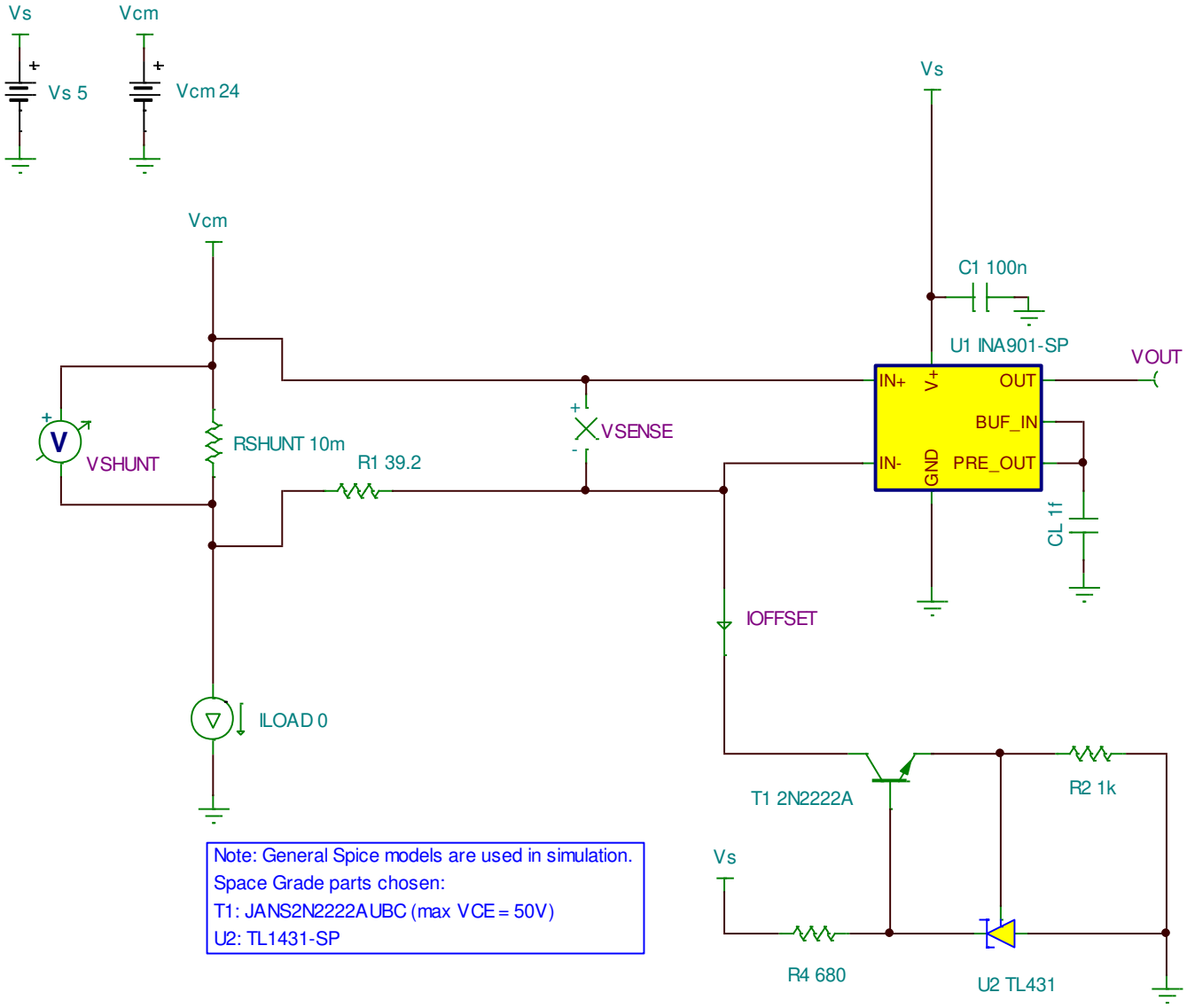

Figure 3-2. INA901-SP High-Side Bidirectional Implementation

The previous resulting steps provide the needed results for a high-side approach. The designed 2.5 mA ideal I_{OFFSET} and chosen 39.2-Ω resistor for R1 combine to produce an ideal 98-mV RTI input voltage, which shifts the V_{SENSE} range again to 23 mV and 173 mV. INA901-SP High Side Simulation Results shows the TINA-TI simulated output results.

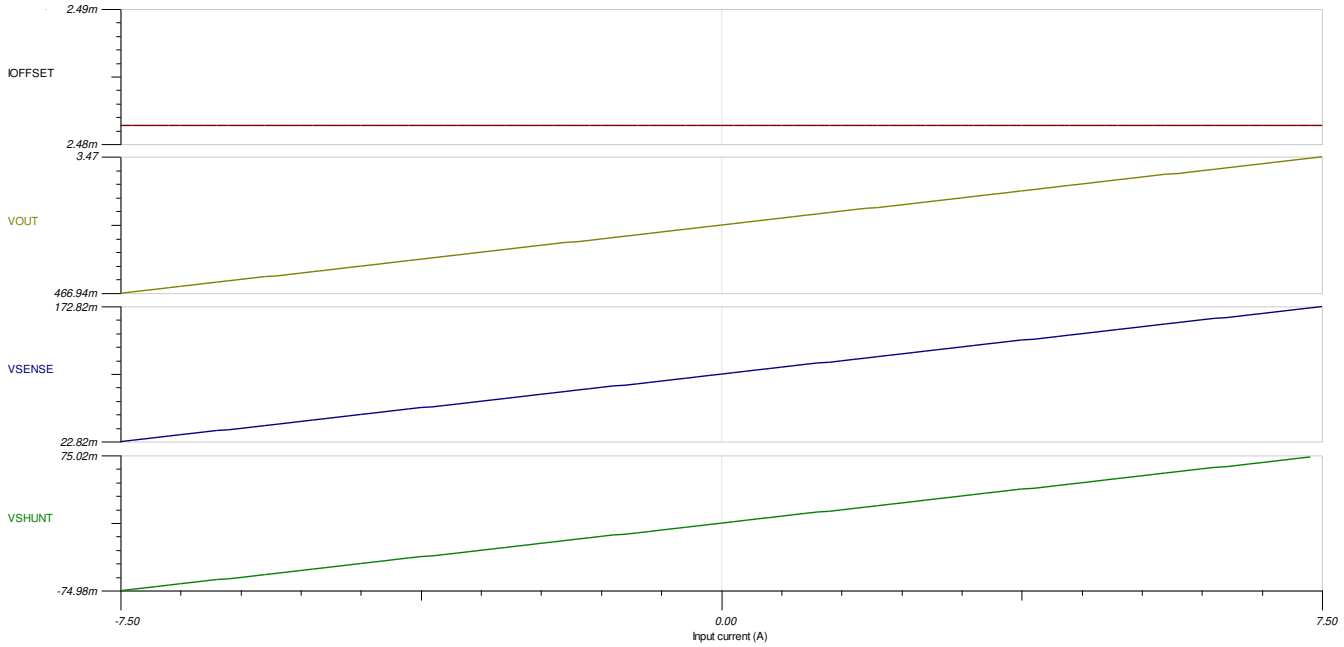

Figure 3-3. INA901-SP High-Side Simulation Results

This design was also prototyped alongside the low-side design for real-world comparison. Table 3-1 through Table 3-3 display data captured via this topology at ambient temperature, as well as temperature extremes of –55°C and 125°C. For these data sets, E96 resistors of 0.1% tolerance were again utilized, maintaining a temperature coefficient of 50 ppm/°C. The BJT utilized here is 2N2222A, which has a maximum collector-emitter voltage of 40 V, which provides sufficient margin for the 24-V_{CM} test condition. Space versions of this part exist (JANS2N2222AUBC) with even higher V_{CE} capabilities (50 V), and was a motivation for this choice.

Table 3-1. INA901 High-Side Results – Test Conditions: V_{CM} = 24 V, V_S = 5 V, T = 25°C

I_{LOAD} (A)	V_{SHUNT}, Meas. (V)	Output Voltage, Meas. Ideal (V)	V_{OUT}, Meas. (V)	Error (%)	V_{OUT}, Calibrated (V)	Error, Calibrated (%)
–7.5	–0.074994	0.46012	0.45511	–1.09%	0.46215	0.44%
–6.25	–0.062494	0.71012	0.70474	–0.76%	0.71178	0.23%
–5	–0.049994	0.96012	0.95445	–0.59%	0.96149	0.14%
–3.75	–0.037494	1.21012	1.2041	–0.50%	1.21114	0.08%
–2.5	–0.024994	1.46012	1.4538	–0.43%	1.46084	0.05%
–1.25	–0.012493	1.71014	1.7035	–0.39%	1.71054	0.02%
0	0.000007	1.96014	1.9531	–0.36%	1.96014	0.00%
1.25	0.012507	2.21014	2.2028	–0.33%	2.20984	–0.01%
2.5	0.025007	2.46014	2.4525	–0.31%	2.45954	–0.02%
3.75	0.037507	2.71014	2.7022	–0.29%	2.70924	–0.03%
5	0.050007	2.96014	2.9519	–0.28%	2.95894	–0.04%
6.25	0.062507	3.21014	3.2015	–0.27%	3.20854	–0.05%
7.5	0.075008	3.46016	3.4512	–0.26%	3.45824	–0.06%

Table 3-2. INA901 High-Side Results – Test Conditions: V_{CM} = 24 V, V_S = 5 V, T = 125°C

I_{LOAD} (A)	V_{SHUNT}, Meas. (V)	Output Voltage, Meas. Ideal (V)	V_{OUT}, Meas. (V)	Error (%)	V_{OUT}, Calibrated (V)	Error, Calibrated (%)
–7.5	–0.074994	0.46012	0.45782	–0.50%	0.46486	1.03%
–6.25	–0.062494	0.71012	0.70733	–0.39%	0.71437	0.60%
–5	–0.049994	0.96012	0.95689	–0.34%	0.96393	0.40%
–3.75	–0.037494	1.21012	1.2065	–0.30%	1.21354	0.28%
–2.5	–0.024994	1.46012	1.4561	–0.28%	1.46314	0.21%
–1.25	–0.012494	1.71012	1.7057	–0.26%	1.71274	0.15%
0	0.000006	1.96012	1.9553	–0.25%	1.96234	0.11%
1.25	0.012504	2.21008	2.205	–0.23%	2.21204	0.09%
2.5	0.025004	2.46008	2.4547	–0.22%	2.46174	0.07%
3.75	0.037504	2.71008	2.7044	–0.21%	2.71144	0.05%
5	0.050004	2.96008	2.9541	–0.20%	2.96114	0.04%
6.25	0.062505	3.2101	3.2037	–0.20%	3.21074	0.02%
7.5	0.075004	3.46008	3.4535	–0.19%	3.46054	0.01%

Table 3-3. INA901 High-Side Results – Test Conditions: V_{CM} = 24V, V_S = 5 V, T = –55°C

I_{LOAD} (A)	V_{SHUNT}, Meas. (V)	Output Voltage, Meas. Ideal (V)	V_{OUT}, Meas. (V)	Error (%)	V_{OUT}, Calibrated (V)	Error, Calibrated (%)
–7.5	–0.074994	0.46012	0.4447	–3.35%	0.45174	–1.82%
–6.25	–0.062494	0.71012	0.69431	–2.23%	0.70135	–1.24%
–5	–0.049994	0.96012	0.94398	–1.68%	0.95102	–0.95%
–3.75	–0.037493	1.21014	1.1937	–1.36%	1.20074	–0.78%
–2.5	–0.024993	1.46014	1.4433	–1.15%	1.45034	–0.67%
–1.25	–0.012494	1.71012	1.693	–1.00%	1.70004	–0.59%
0	0.000006	1.96012	1.9429	–0.88%	1.94994	–0.52%
1.25	0.012506	2.21012	2.1925	–0.80%	2.19954	–0.48%
2.5	0.025006	2.46012	2.4422	–0.73%	2.44924	–0.44%
3.75	0.037506	2.71012	2.6919	–0.67%	2.69894	–0.41%
5	0.050006	2.96012	2.9417	–0.62%	2.94874	–0.38%
6.25	0.062507	3.21014	3.1914	–0.58%	3.19844	–0.36%
7.5	0.075006	3.46012	3.4411	–0.55%	3.44814	–0.35%

This design also operates in a unidirectional manner, similar to the low-side approach; therefore, the offset should be calibrated for best results. Unlike the low-side approach, because the offset current is set via a constant current source, the offset voltage is maintained independently of the sense voltage, although there may still be some deviation due to temperature drift in R2. This can be optimized through low-drift, high-precision resistor selection.

Table 3-1 through Table 3-3 list the actual data points captured from bench testing, and list the error compared against calculated design ideals, as well as adjusted error from a one-point calibration performed in post. It can be observed that by performing this calibration, error can be improved upon for the majority of the measurement range, and the linear error present in the low-side design due to the shifting sense node is eliminated.

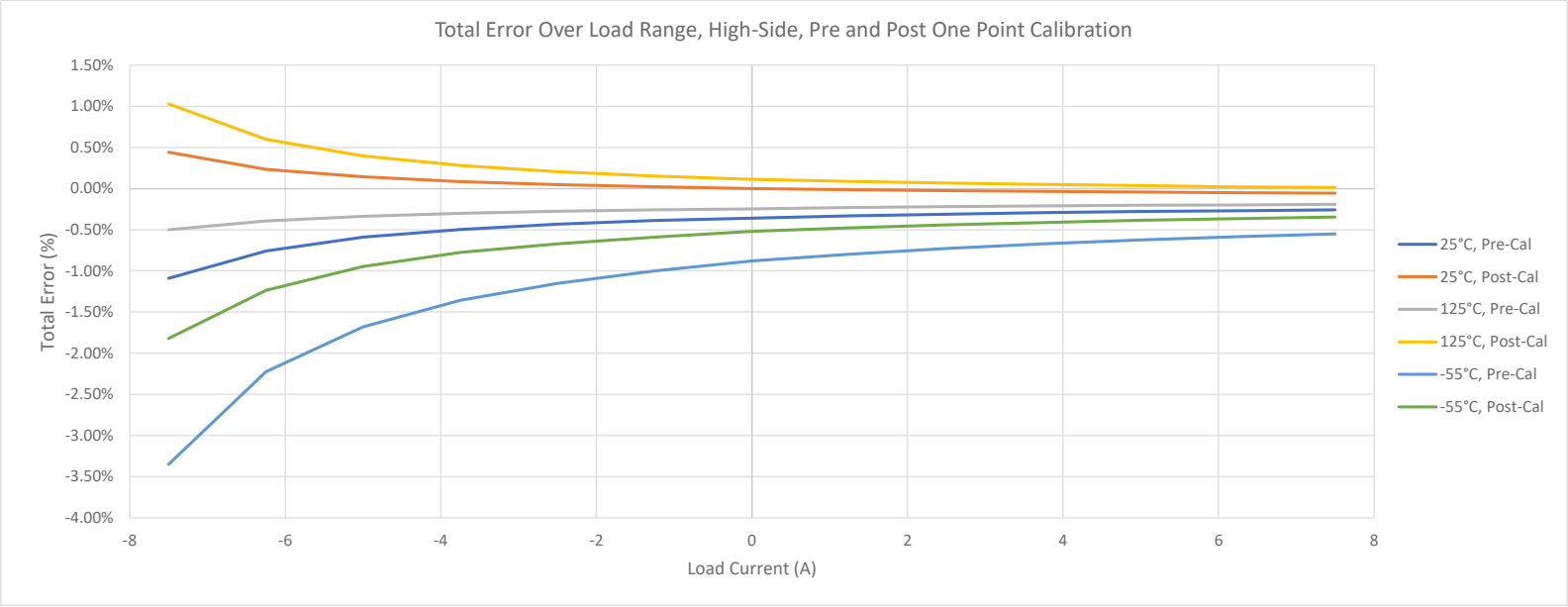

Figure 3-4. High-Side, Bidirectional Error Over Range, Pre- and Post-Calibration

4 Summary

This application note demonstrates two separate topologies for bidirectional design of the INA901-SP, and provides executed bench tests to demonstrate that less than one percent error over a wide current operating range is potentially achievable via use of these topologies when a calibration is able to be performed.

Care must be taken when implementing such a system, as challenges and pitfalls do exist, as the method for this implementation is observed as an erroneous measurement when using the INA901, or any current sense amplifier for that matter, in its normal operating use case.

Finally, it is observed that for optimal results from the viewpoint of part count, propagation delay, or many other potential factors, the design must be compartmentalized into a specific use case such as high- or low-side sensing, and these use cases are unable to be deviated from. The following conclusions for the two circuits were made:

1. In the case of low-side sensing, the V_{CM} of the IN+ pin must be held to less than that of the supply voltage to ensure proper operation. While implementation on the high side may be possible, provided the condition 0 < V_{CM}+V_{SENSE} < V_S is satisfied, this seems impractical, and this potential use case was not explored.
2. In the case of high-side sensing, the V_{CM} of the IN– pin must be held to less than that of the established REF voltage of the TL1431-SP, which is 2.5 V.

These conclusions show that neither design is common-mode independent, and the common mode of the design must be taken into account to ensure that invalid use cases will not be performed.

Due diligence was conducted on additional topologies that potentially operate independently of the amplifier V_{CM}, but were ultimately shelved due to high part count, the need to operate within the < 20-mV sense condition, propagation delay of the circuitry, and complexity of design. Figure 4-1 and Figure 4-2 illustrate an example of one of these topologies, without comment, as a starting point for potential operating use cases that require this need, but it is left to the reader as to the potential fit for their given system. Due to the delays of the signal chain, such designs should only be used for applications such as telemetry, and not time-sensitive applications such as overcurrent protection or motor control. Note that even this circuit is slightly common-mode limited, due to the 1.5-V referenced GND of component U2.

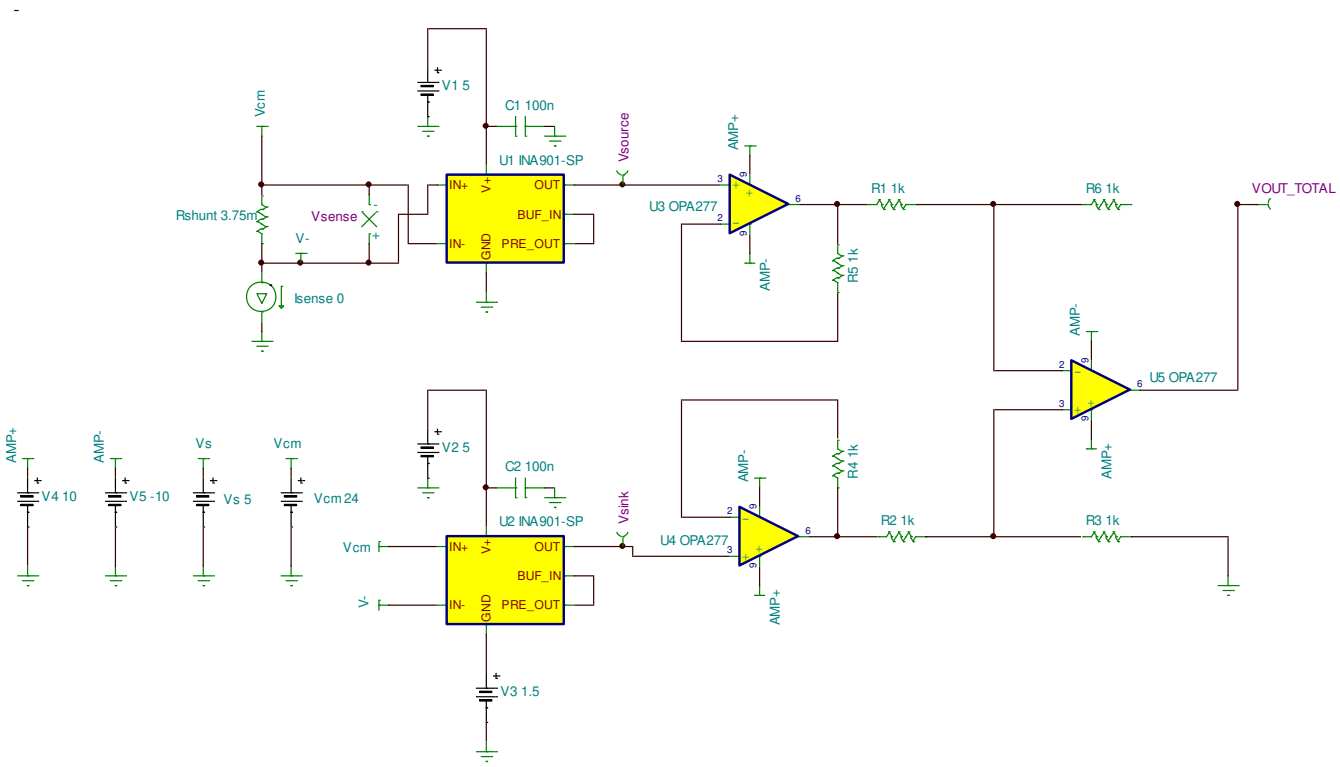

Figure 4-1. INA901 Bidirectional Design With Independent VCM (–13.5 V to 65 V)

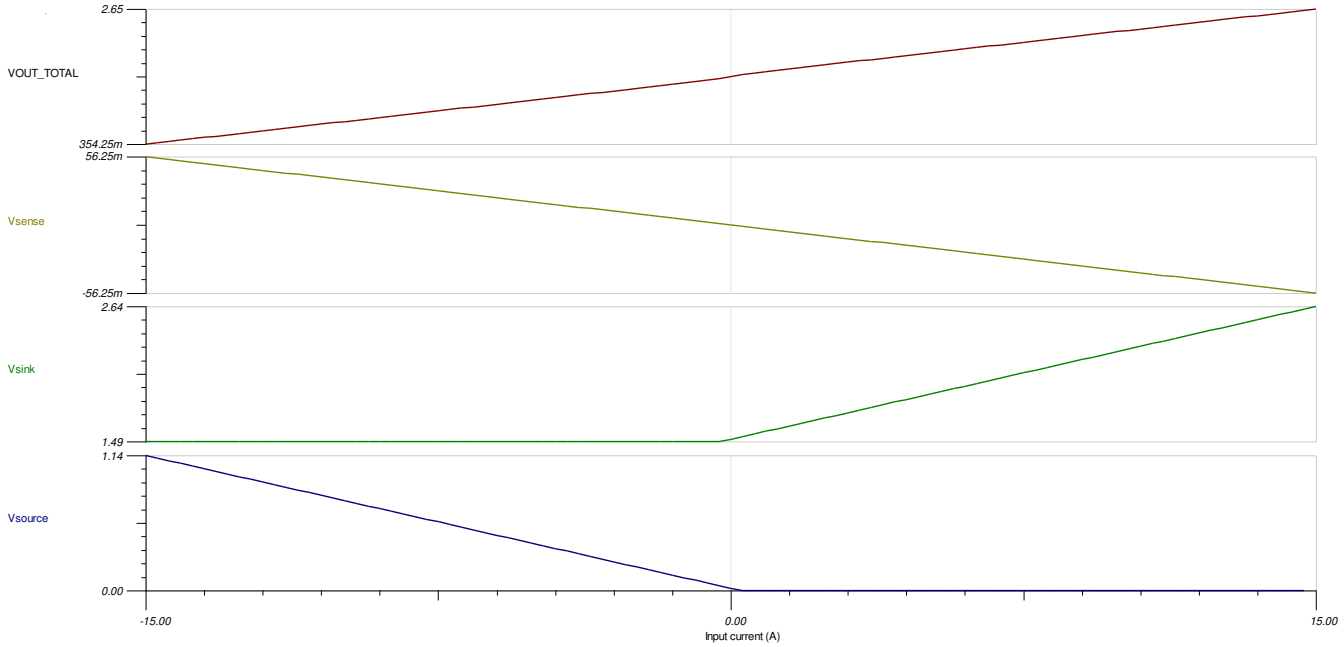

Figure 4-2. INA901 Independent VCM Design Simulated Results

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