ALM2402F-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for ALM2402F-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

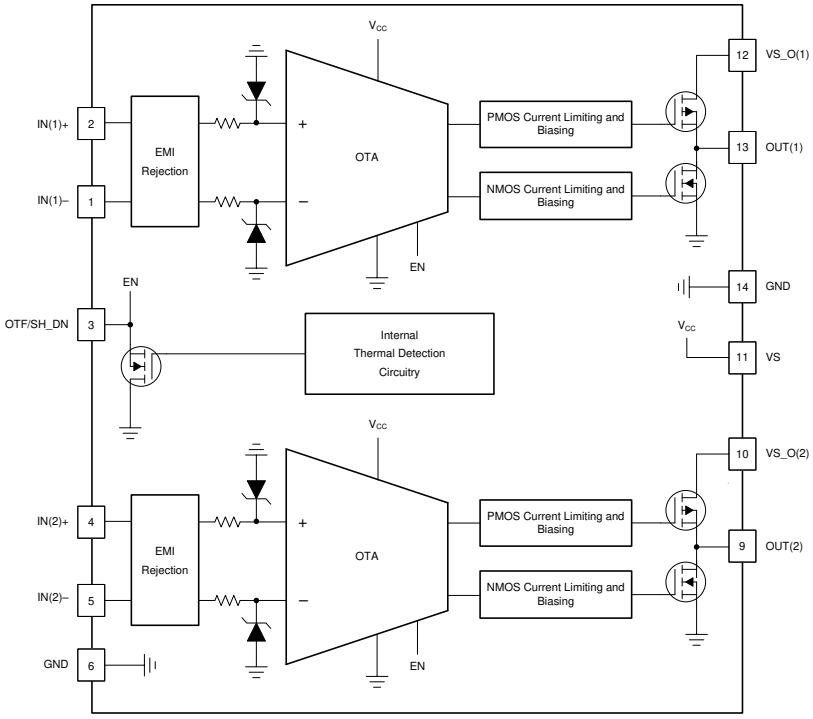

Figure 1. Functional Block Diagram

ALM2402F-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for ALM2402F-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	12
Die FIT Rate	4
Package FIT Rate	8

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 290 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ALM2402F-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	20%
Out saturate high	25%
Out saturate low	25%
Out functional not in specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ALM2402F-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to supply (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the ALM2402F-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the ALM2402F-Q1 datasheet.

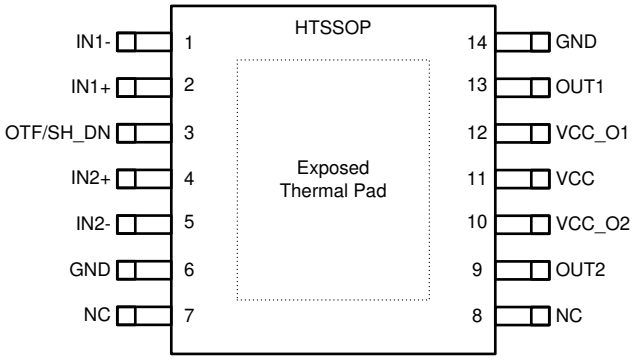

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 'Short circuit to Power' means short to VS or VS_O.
- 'Short circuit to GND' means short to GND.
- OTF/SH_DN pin is configured in such a state as to enable the amplifier

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN(1)–	1	Negative feedback not present to device. Depending on IN(1)+ configuration, output will most likely move to VS_O voltage. Device will likely not sustain damage but application will be effected.	D
IN(1)+	2	Device common-mode tied to negative rail. Depending on IN(1)– configuration, output will likely not respond due to the device being put in an invalid common-mode condition. Device will likely not sustain damage, but application will be effected.	D
OTF/SH_DN	3	Device common-mode tied to negative rail. Depending on IN(2)- configuration, output will likely not respond due to the device being put in an invalid common-mode condition. Device will likely not sustain damage, but application will be effected.	D
IN(2)+	4	Device common-mode tied to negative rail. Depending on IN(2)– configuration, output will likely not respond due to the device being put in an invalid common-mode condition. Device will likely not sustain damage, but application will be effected.	D
IN(2)–	5	Negative feedback not present to device. Depending on IN(2)+ configuration, output will most likely move to VS_O voltage. Device will likely not sustain damage but application will be effected.	D
GND	6	No effect, similar potential and purpose.	D
NC	7	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
NC	8	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
OUT(2)	9	Output shorted to GND. Depending on circuit configuration, device will likely be forced into short circuit condition with pin voltage ultimately left at GND. Prolonged exposure to short circuit conditions could result in long term reliability issues. Thermal shutdown likely. Device will likely not sustain damage, but application will be effected.	D
VS_O(2)	10	Device power supply will be shorted to ground. Output stage will not be biased correctly and signals applied to OUT(2) or OUT(1), likely via feedback components to respective IN(1)- or IN(2)-, would be in violation of absolute maximum specifications, possibly resulting in device damage.	A
VS	11	Device power supply will be shorted to ground. Input stage will not be biased correctly and signals applied to IN(1)+, IN(2)+, IN(1)-, IN(1)+ would be in violation of absolute maximum specifications, likely resulting in device damage.	A
VS_O(1)	12	Device power supply will be shorted to ground. Output stage will not be biased correctly and signals applied to OUT(2) or OUT(1), likely via feedback components to respective IN(1)- or IN(1)+, would be in violation of absolute maximum specifications, possibly resulting in device damage.	A
OUT(1)	13	Output shorted to GND. Depending on circuit configuration, device will likely be forced into short circuit condition with pin voltage ultimately left at GND. Prolonged exposure to short circuit conditions could result in long term reliability issues. Thermal shutdown likely. Device will likely not sustain damage, but application will be effected.	D
GND	14	Device power supply will be shorted to ground. Output stage will not be biased correctly and signals applied to OUT(2) or OUT(1), likely via feedback components to respective IN(1)- or IN(1)+, would be in violation of absolute maximum specifications, possibly resulting in device damage.	A

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN(1)–	1	Negative feedback not present to device. Depending on IN(1)+ configuration, output will likely move to either VS_O or GND voltage. Device will likely not sustain damage, but application will be effected.	D
IN(1)+	2	No common-mode bias present to device. Depending on IN(1)- configuration, output will likely move to either VS_O or GND voltage. Device will likely not sustain damage, but application will be effected.	D
OTF/SH_DN	3	Shutdown pin not driven, thermal shutdown cannot be monitored. Also, depending on resulting bias voltage applied to the pin while floating, there is potential for the device to be shutdown or enabled outside intended application. Device will likely not sustain damage, but application will be effected.	D
IN(2)+	4	No common-mode bias present to device. Depending on IN(2)- configuration, output will likely move to either VS_O or GND voltage. Device will likely not sustain damage, but application will be effected.	D
IN(2)–	5	Negative feedback not present to device. Depending on IN(2)+ configuration, output will likely move to either VS_O or GND voltage. Device will likely not sustain damage, but application will be effected.	D
GND	6	No current return path for output current on this pin. For lower currents, device operation and functionality should remain similar. For higher currents, device could potentially have long term reliability concerns if this pin is left floating for an extended period of time.	A
NC	7	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
NC	8	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
OUT(2)	9	Output disconnected, no feedback or output drive. Device will likely not sustain damage, but application will be effected.	D
VS_O(2)	10	Output power supply left floating. For lower currents, device operation and functionality should remain similar. For higher currents, device could potentially have long term reliability concerns or damage.	C
VS	11	Input stage supply left floating. Depending on circuit configuration, VS pin will likely settle at GND voltage. Input stage will not be biased correctly and signals applied to IN(1)+, IN(2)+, IN(1)-, IN(1)+ would be in violation of absolute maximum specifications, likely resulting in device damage.	A
VS_O(1)	12	Output power supply left floating. For lower currents, device operation and functionality should remain similar. For higher currents, device could potentially have long term reliability concerns or damage.	A
OUT(1)	13	Output disconnected, no feedback or output drive. Device will likely not sustain damage, but application will be effected.	D
GND	14	No current return path for output current on this pin. For lower currents, device operation and functionality should remain similar. For higher currents, device could potentially have long term reliability concerns or damage.	A

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN(1)–	1	Both inputs will be tied together. Depending on the offset of the device, this will likely move the output voltage near mid supply (VS_O/2). Device will likely not sustain damage, but application will be effected.	D
IN(1)+	2	If OTF/SH_DN is being driven by source, IN(1)+ and OTF/SH_DN sources tied together. If OTF/SH_DN is being monitored with no source, there is potential for IN(1)+ bias voltage to be above allowable voltage limit for OTF/SH_DN and result in damage to the pin. Also, in either case, depending on resulting bias voltage applied to the pins, there is potential for the device to be shutdown or enabled outside intended application.	D
OTF/SH_DN	3	If OTF/SH_DN is being driven by source, IN(2)+ and OTF/SH_DN sources tied together. If OTF/SH_DN is being monitored with no source, there is potential for IN(2)+ bias voltage to be above allowable voltage limit for OTF/SH_DN and result in damage to the pin. Also, in either case, depending on resulting bias voltage applied to the pins, there is potential for the device to be shutdown or enabled outside intended application.	D
IN(2)+	4	Both inputs will be tied together. Depending on the offset of the device, this will likely move the output voltage near mid supply (VS_O/2). Device will likely not sustain damage, but application will be effected.	D
IN(2)–	5	Negative feedback not present to device. Depending on IN(2)+ configuration, output will most likely move to VS_O voltage. Device will likely not sustain damage but application will be effected.	D
GND	6	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
NC	7	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
NC	8	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
OUT(2)	9	Output shorted to VS_O. Depending on circuit configuration, device will likely be forced into short circuit condition with pin voltage ultimately left at VS_O. Prolonged exposure to short circuit conditions could result in long term reliability issues. Thermal shutdown likely. Device will likely not sustain damage, but application will be effected.	D
VS_O(2)	10	VS_O shorted to VS. In applications where VS_O = VS there will be no change to device functionality. In application where VS_O != VS, sources will be shorted resulting in unknown state for supply voltage. Power dissipation on VS_O could increase or decrease, impacting power calculations or resulting in thermal shutdown. Assuming the supply voltages stay within the Absolute Maximum Specifications during this event, device will likely not sustain damage but application will be effected.	D
VS	11	VS_O is shorted to VS. In applications where VS_O = VS there will be no change to device functionality. In application where VS_O != VS, sources will be shorted resulting in unknown state for supply voltage. Power dissipation on VS_O could increase or decrease, impacting power calculations or resulting in thermal shutdown. Assuming the supply voltages stay within the Absolute Maximum Specifications during this event, device will likely not sustain damage but application will be effected.	D
VS_O(1)	12	Output shorted to VS_O. Depending on circuit configuration, device will likely be forced into short circuit condition with pin voltage ultimately left at VS_O. Prolonged exposure to short circuit conditions could result in long term reliability issues. Thermal shutdown likely. Device will likely not sustain damage, but application will be effected.	D
OUT(1)	13	Output shorted to GND. Depending on circuit configuration, device will likely be forced into short circuit condition with pin voltage ultimately left at GND. Prolonged exposure to short circuit conditions could result in long term reliability issues. Thermal shutdown likely. Device will likely not sustain damage, but application will be effected.	D
GND	14	Negative feedback not present to device. Depending on IN(1)+ configuration, output will most likely move to VS_O voltage. Device will likely not sustain damage but application will be effected.	D

Table 8. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN(1)–	1	Negative feedback not present to device. Depending on IN(1)+ configuration, output will most likely move to GND voltage. Device will likely not sustain damage, but application will be effected.	D
IN(1)+	2	Device common-mode tied to positive rail. Depending on IN(1)- configuration, output will likely not respond due to the device being put in an invalid common-mode condition. Device will likely not sustain damage, but application will be effected.	D
OTF/SH_DN	3	OTF/SH_DN driven to VCC or VCC_O. Depending on supply voltage, device could violate Absolute Maximum Ratings and result in damage to the device. OTF/SH_DN cannot be monitored or controlled properly in application.	D
IN(2)+	4	Device common-mode tied to positive rail. Depending on IN(2)- configuration, output will likely not respond due to the device being put in an invalid common-mode condition. Device will likely not sustain damage, but application will be effected.	D
IN(2)–	5	Negative feedback not present to device. Depending on IN(2)+ configuration, output will most likely move to GND voltage. Device will likely not sustain damage, but application will be effected.	D
GND	6	Device power supply will be shorted to ground. If supply short is coming from VS, input stage will not be biased correctly and signals applied to IN(1)+, IN(2)+, IN(1)-, IN(2)+ would be in violation of absolute maximum specifications, likely resulting in device damage. If supply short is coming form VS_O, output stage will not be biased correctly and signals applied to OUT(2) or OUT(1), likely via feedback components to respective IN(1)- or IN(1)+, would be in violation of absolute maximum specifications, possibly resulting in device damage.	A
NC	7	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
NC	8	No effect, assuming design has left this pin disconnected as instructed in datasheet.	D
OUT(2)	9	Output shorted to VS_O or VS. Depending on circuit configuration, device will likely be forced into short circuit condition with pin voltage ultimately left at VS_O or VS. Prolonged exposure to short circuit conditions could result in long term reliability issues. Thermal shutdown likely. Device will likely not sustain damage, but application will be effected.	D
VS_O(2)	10	In cases where VS_O is shorted to VS: In applications where VS_O = VS there will be no change to device functionality. In application where VS_O != VS, sources will be shorted resulting in unknown state for supply voltage. Power dissipation on VS_O could increase or decrease, impacting power calculations or resulting in thermal shutdown. Assuming the supply voltages stay within the Absolute Maximum Specifications during this event, device will likely not sustain damage but application will be effected. In cases where VS_O is shorted to VS_O: No effect.	D
VS	11	In cases where VS_O is shorted to VS: In applications where VS_O = VS there will be no change to device functionality. In application where VS_O != VS, sources will be shorted resulting in unknown state for supply voltage. Power dissipation on VS_O could increase or decrease, impacting power calculations or resulting in thermal shutdown. Assuming the supply voltages stay within the Absolute Maximum Specifications during this event, device will likely not sustain damage but application will be effected. In cases where VS is shorted to VS: No effect.	D
VS_O(1)	12	In cases where VS_O is shorted to VS: In applications where VS_O = VS there will be no change to device functionality. In application where VS_O != VS, sources will be shorted resulting in unknown state for supply voltage. Power dissipation on VS_O could increase or decrease, impacting power calculations or resulting in thermal shutdown. Assuming the supply voltages stay within the Absolute Maximum Specifications during this event, device will likely not sustain damage but application will be effected. In cases where VS_O is shorted to VS_O: No effect.	D
OUT(1)	13	Output shorted to VS_O or VS. Depending on circuit configuration, device will likely be forced into short circuit condition with pin voltage ultimately left at VS_O or VS. Prolonged exposure to short circuit conditions could result in long term reliability issues. Thermal shutdown likely. Device will likely not sustain damage, but application will be effected.	D
GND	14	Device power supply will be shorted to ground. If supply short is coming from VS, input stage will not be biased correctly and signals applied to IN(1)+, IN(2)+, IN(1)-, IN(1)+ would be in violation of absolute maximum specifications, likely resulting in device damage. If supply short is coming form VS_O, output stage will not be biased correctly and signals applied to OUT(2) or OUT(1), likely via feedback components to respective IN(1)- or IN(2)-, would be in violation of absolute maximum specifications, possibly resulting in device damage.	A

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