Functional Safety Information

INA226-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for INA226-Q1 (VSSOP-10 package) to aid in a functional safety system design. Information provided are:

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- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

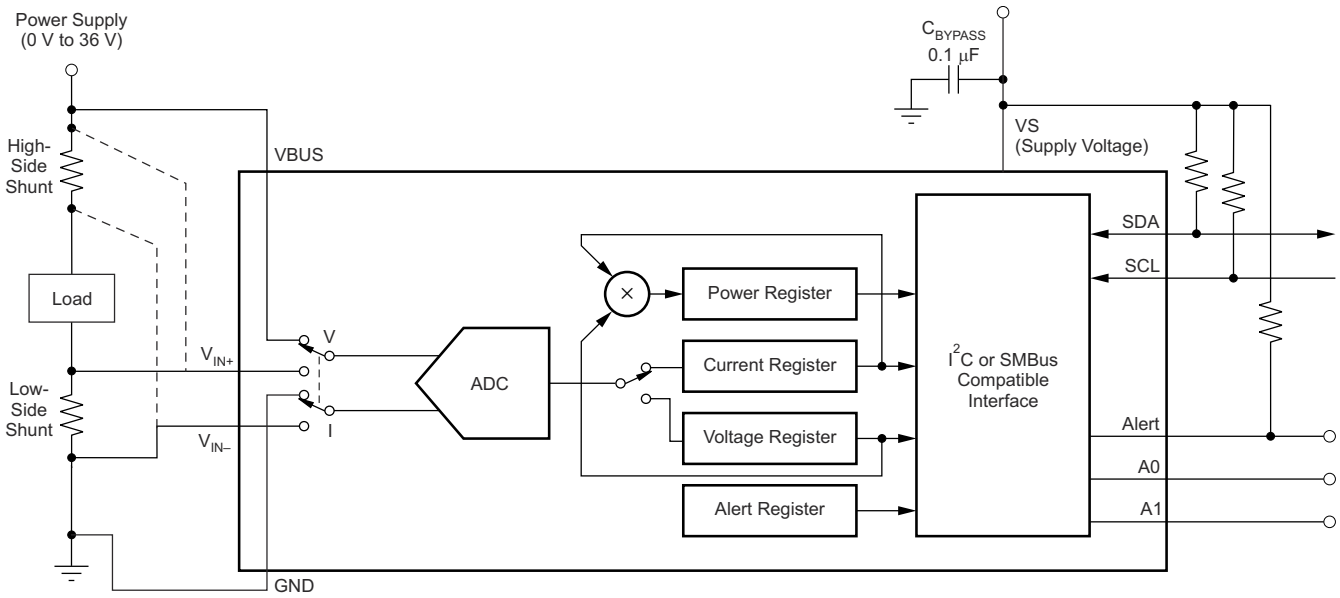

Figure 1-1. Functional Block Diagram

INA226-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for INA226-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	3
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 100mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA226-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
ADC output bit error	20
ADC gain out of specification	15
ADC offset out of specification	15
Communication error	10
Register bit error	10
ADC MUX select error	10
ALERT - false trip or failure to trip	15
Pin-to-pin short, any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the INA226-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the INA226-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA226-Q1 data sheet.

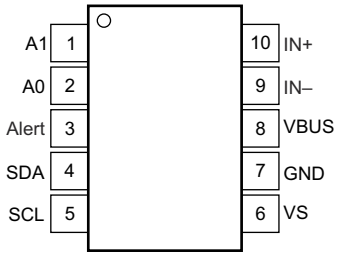

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 2.7V to 5.5V
- V_{BUS} = 12V
- Device is the only slave on the I^2C bus

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A1	1	Power supply shorted to GND if A1 is initially connected to VS. Slave address changes if A1 is not initially grounded.	B
A0	2	Power supply shorted to GND if A0 is initially connected to VS. Slave address changes if A0 is not initially grounded.	B
ALERT	3	Alert pin cannot be pulled high and thus alerts cannot be detected by host.	C
SDA	4	Halts digital communication.	B
SCL	5	Halts digital communication.	B
VS	6	Power supply shorted to GND and device is turned off.	B
GND	7	Normal operation.	D
VBUS	8	Cannot measure bus voltage. A short from the bus supply to GND occurs. High current flows from bus supply through VBUS trace and to GND. Shunt, trace, and bus voltage sources can be damaged.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN-	9	Corrupts (saturates or shorts) the input sense voltage unless IN- is already connected to GND. If high-side application, then bus voltage source is shorted to GND and is potentially damaged due to high-current. If low-side and IN+ is initially connected to bus GND, then sense voltage becomes zero.	B Only D if low-side sensing positive V_{SENSE}.
IN+	10	Corrupts (saturate or shorts) the input sense voltage unless IN+ is already connected to GND. If high-side application, then bus voltage source is shorted to GND and is potentially damaged due to high-current. If low-side and IN- is initially connected to bus GND, then sense voltage becomes zero.	B Only D if low-side sensing negative V_{SENSE}.

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A1	1	Changes the slave address of the device if A1 is not already floating.	C
A0	2	Changes the slave address of the device if A0 is not already floating.	C
ALERT	3	ALERT cannot be pulled high and alerts cannot be detected by host.	C
SDA	4	Halts digital communication.	B
SCL	5	Halts digital communication.	B
VS	6	No power to the device. Device can be partially biased through inputs. No damage to the device.	B
GND	7	No power to the device.	B
VBUS	8	Cannot measure the bus voltage and thus cannot calculate power.	C
IN-	9	Cannot measure sense voltage.	B
IN+	10	Cannot measure sense voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
A1	1	2 - A0	Can change the slave address of the device if A1 is not already the same as A0.	C
A0	2	3 - ALERT	Can halt the alert response if A0 is tied to GND or change the slave address if ALERT is pulled high and A0 is initially floating.	C
ALERT	3	4 - SDA	Halts digital communication as long as ALERT pin is active LOW. ALERT can be pulled low by SDA.	B
SDA	4	5 - SCL	Halts digital communication.	B
SCL	5	6 - VS	Shorts out the SCL pullup resistor and halts digital communication.	B
VS	6	7 - GND	Power supply is shorted to GND and device is turned off.	B
GND	7	8 - VBUS	Cannot measure bus voltage. A short from the bus supply to GND occurs. High current flows from bus supply through VBUS trace and to GND. Shunt, trace, and bus voltage sources can be damaged.	B
VBUS	8	9 - IN-	This can create a short in parallel with the shunt resistor, which effects sense voltage. Can potentially cause the short or trace connecting VBUS to IN- to burn up from high bus currents.	B
IN-	9	10 - IN+	This can short out the shunt resistance and make input voltage 0V. Can potentially cause the short or trace connecting IN+ to IN- to burn up from high bus currents.	B
IN+	10	1 - A1	A1 is a digital input pin and can be damaged if shorted to voltage greater than 6V. For high-side application, shorting IN+ and A1 can damage pin if IN+ common-mode voltage is greater than 6V. For a low-side application, this changes the slave address if A1 is not already connected to GND.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A1	1	Changes the slave address of the device if A1 is not already tied to VS.	C
A0	2	Changes the slave address of the device if A0 is not already tied to VS.	C
ALERT	3	Shorts out the ALERT pullup resistor. If ALERT activates (active LOW), then only the internal resistance of the transistor limits the I_{OL} current into ALERT. According to absolute maximum ratings, if I_{OL} > 10mA (which is likely with no pullup resistance), then damage to the internal transistor or device is possible. The increase in IOL current can increase the V_{OL} (low-level output voltage) of the ALERT pin during an alert event.	A
SDA	4	Shorts out the SDA pullup resistor and halts digital communication. If SDA is driven low by INA226-Q1 (slave), then device damage can occur if I_{OL} > 10mA, which is likely with no pullup resistance. The increase in I_{OL} current can likely increase the V_{OL} (low-level output voltage) of SDA.	A
SCL	5	Shorts out the SCL pullup resistor and halts digital communication.	B
VS	6	Normal operation.	D
GND	7	Power supply is shorted to GND and device turns off.	B
VBUS	8	Bus voltage source is shorted to VS rail. If VS is driven to voltage > 6V, the INA226-Q1 is damaged.	A
IN-	9	For high-side applications, this shorts bus source to VS rail. If VS is driven to voltage > 6V, then this can damage INA226-Q1. For low-side applications, this does not cause device damage, but can cause the VS supply to short to GND causing a sharp rise in current through the shunt, and the device can turn off.	A
IN+	10	For high-side applications, this shorts bus source to VS rail. If VS is driven to voltage > 6V, then this can damage INA226-Q1. For low-side applications, this does not cause device damage, but can cause the VS supply to short to GND causing a sharp rise in current through the shunt, and the device can turn off.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2020) to Revision B (November 2024) **Page**

- Amended for Redbull.....2

Changes from Revision * (January 2020) to Revision A (March 2020) **Page**

- Changed to latest report format, including FIT Rate, FMD, and Pin FMA.....2

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