Application Note

High Resolution, Small Form Factor Phase Current Sense for 48V Robotics and Servo Drives

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ABSTRACT

This application note introduces the newly released *AMC0106M05* and *AMC0106M25* functionally isolated modulators. The *M05* variant supports a ±50mV, the *M25* variant a ±250mV linear input range. Both devices come in a small, lead-less package. The AMC0106Mxx devices enable the design of an accurate and reliable, shunt-based current-sensing subsystem for three-phase inverters with a small form-factor. Typical applications are servo drives, and collaborative or humanoid robots powered from sub-60V power supplies. A circuit design and layout example for a 48V 3-phase GaN inverter with boot bootstrap supply with a ±50A linear current range is presented. The design is based on the AMC0106M05 variant and 1mΩ shunt. Test results are presented showing that a measurement resolution up to 14 effective number of bits (ENOB) is achieved. Phase current measurement is not affected by PWM switching, validating the high immunity against common-mode transients. And finally, this has shown that ripple voltage caused by the bootstrap supply has no effect on the phase current measurement for a wide range of PWM duty cycles.

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Trademarks

1 Introduction

High performance, three-phase inverters operated at 24V to 60V are gaining more traction in emerging industrial applications such as high-efficiency servo drives, and collaborative, surgery, and humanoid robots. Accurate and reliable phase current sensing is crucial in these applications to achieve smooth torque and precise position control. These applications are highly space constrained and the 3-phase inverters are often integrated into the motor. Therefore, a small design size with low profile and the ability to operate at high ambient temperatures up to 125°C are important. In-phase, shunt-based current sensing as shown in Figure 1-1 provides the highest resolution measurement of the motor current and is an industry standard design for high-performance motor drives. TI's newly released AMC0106Mxx functionally isolated modulators in a small, lead-less package enable such measurement in a much smaller design size than what has been achievable so far.

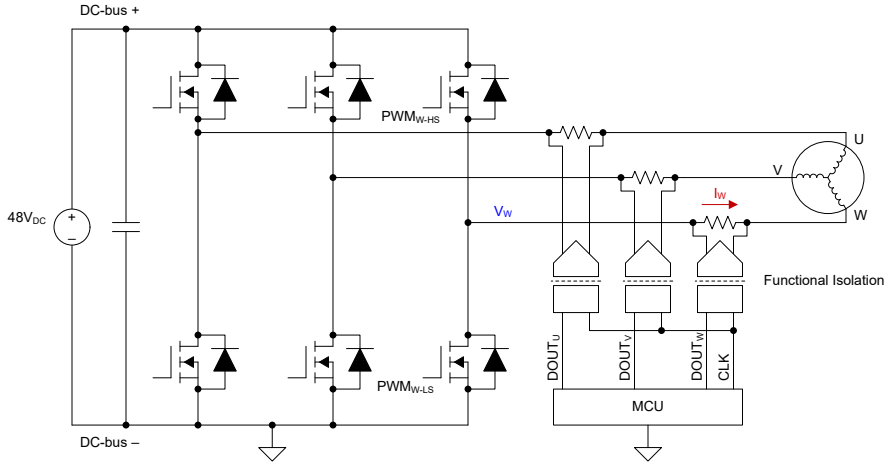


Figure 1-1. 48V, 3-Phase Inverter With Shunt-Based, In-Phase Current Sensing

2 Design Challenges

In-line phase current sensing enables higher performance, continuous measurement, and more precise control of the motor phase current over the entire PWM cycle compared to low-side shunt sensing. In a low-side shunt sensing system, the current is discontinuous and the phase current can only be measured during part of the PWM period, when the low-side power switch is turned on. These systems typically result in a less accurate and lower bandwidth phase current closed-loop control. Therefore, in-line phase current sensing is typically the choice for servo drives and robotic applications. However, the phase voltage is pulse-width modulated and periodically switched between GND and the DC-bus voltage, typically 48V. The microcontroller is referred to GND. This means that the phase current sense subsystem needs to handle a high common-mode voltage and high common-mode transients. The slew rate of the common-mode transients are in the range of 10V/ns. With emerging, fast switching GaN-FETs, slew rates are significantly higher. A digital interface between the microcontroller and current sensor is preferable and improves signal integrity and eliminates issues from ground bouncing during switching.

Figure 2-1 shows a simplified diagram of one of the motor phase currents and the corresponding PWM voltage over one PWM cycle. For closed-loop control, it is sufficient to measure the phase current in the center of the PWM. For small PWM duty cycles the rising or falling edge of the PWM switching falls into the sampling window of the delta-sigma ADC. Duty cycle is defined as the ON-time of the high-side FET relative to the PWM period.

An alternative approach is to continuously sample the phase currents at a sampling rate much higher than the PWM frequency. The individual samples are averaged to get an accurate measurement of the average current and eliminate the inherent current ripple. This method also supports fast short-circuit and over-current detection and sample rates up to 2.5Msps are not uncommon. An advanced use case for continuous oversampling is predictive maintenance. For example, analyzing the phase current spectral signature allows detecting the onset of bearing faults.

For both approaches, PWM switching occurs during phase current sampling. Therefore, it is critical that the phase current sensor is immune to high common mode voltage transients, and PWM switching and does not impact measurement accuracy.

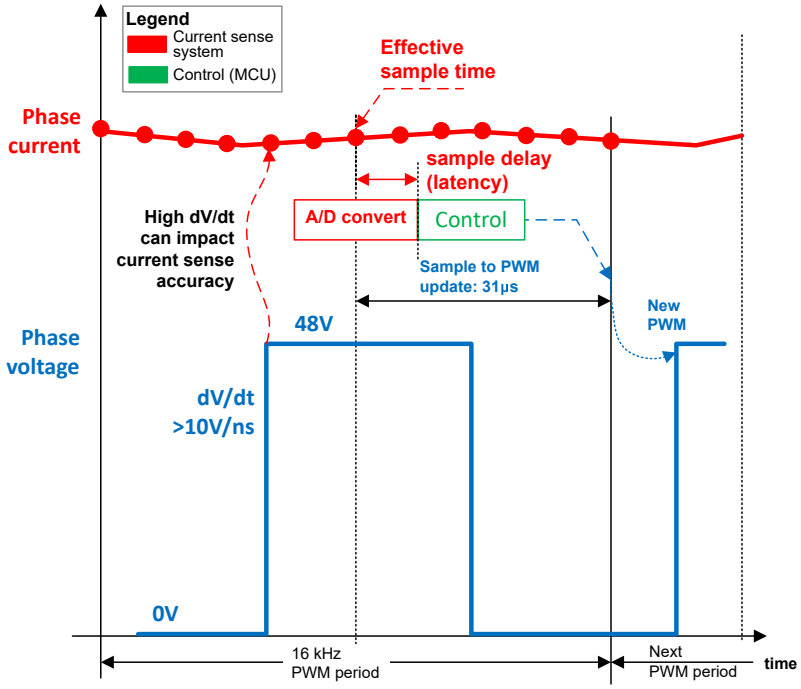


Figure 2-1. Current Sampling for Closed-Loop Phase Current Control and Short-Circuit Detection

A current sense subsystem for a high-performance servo drives shall meet the following requirements:

- High accuracy: better than 1%
- High resolution: better than 12 effective number of bits (ENOB)
- Low propagation delay (latency): <20µs
- High common mode voltage: >60V
- High common mode transient immunity (CMTI): >>10V/ns
- Fast short-circuit detection: <2µs
- A digital interface with high immunity against electromagnetic interferences such as conducted RF and fast transient bursts
- Immunity to external magnetic fields
- Small PCB design size and low profile

3 Design Approach

Several designs exist for in-phase current sensing in space constrained applications where a small form factor and low height are critical. In-package Hall sensors, shunts with non-isolated amplifiers, and shunts with isolated amplifiers or isolated delta-sigma modulators are just a few of them.

Shunt-based current sensing with a delta-sigma modulator offers the highest measurement resolution and is the method of choice for high-performance motor drives. The digital interface to the microcontroller offers the additional benefit of high EMC immunity. For <60V operation functional isolation is sufficient. Figure 3-1 shows a simplified block diagram of a shunt, a 8-pin, functionally isolated, modulator, and a microcontroller connected to the delta-sigma modulator through a two-wire interface for clock and data. The microcontroller contains a digital low-pass filter, such as a sync^3 filter, that also converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation).

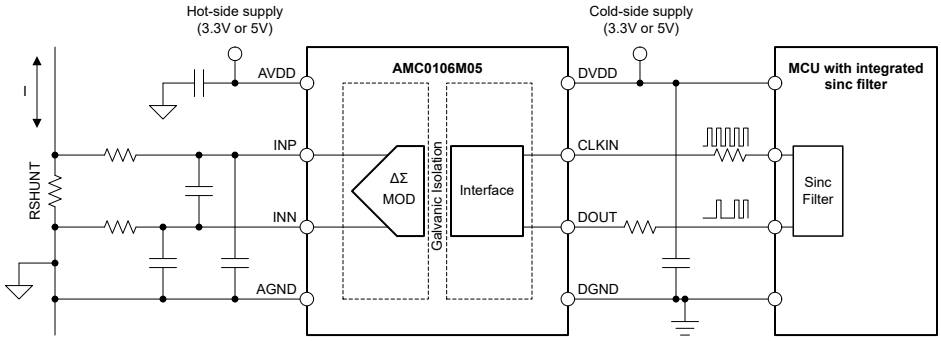


Figure 3-1. Isolated Phase Current Sense Subsystem with MCU Integrated Sync Filter

3.1 AMC0106Mxx Functionally Isolated Modulators

The AMC0106Mxx are precision, functionally isolated, second-order delta-sigma modulators designed for shunt-based current sensing. The M05 version supports a linear input range of ±50mV. The M25 supports a linear input range of ±250mV. The isolation barrier separates parts of the system that operate on different common-mode voltage levels. A typical application is phase current sensing in high-performance servo drives. The isolation barrier supports a working voltage up to $200V_{RMS}$ / $280V_{DC}$ and transient over voltages up to $570V_{RMS}$ / $800V_{DC}$.

The sigma-delta modulator on the *hot* side receives a clock from the *cold* side. The modulator translates the analog input signal into a bit stream of digital ones and zeros that is synchronous to the clock. The digital bit stream is transferred back to the cold side across the galvanic isolation barrier and output on the DOUT pin. The time average of the bit stream is proportional to the analog input voltage. The block diagram of the AMC0106Mxx is shown in Figure 3-2.

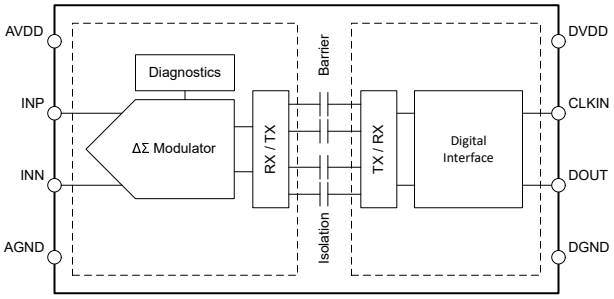


Figure 3-2. AMC0106Mxx Block Diagram

The modulator bit stream contains high frequency quantization noise. Therefore the bit stream is processed by a digital low-pass filter to increase measurement resolution. Many micro control units (MCUs) support delta-sigma filtering with a dedicated peripheral block, such as the Sigma-Delta Filter Module (SDFM) integrated with the C2000™ and Sitara™ microcontrollers. Alternatively, the digital filter is implemented in a field-programmable gate array (FPGA).

Isolates sigma-delta modulators have existed for many years and are an industry standard design for phase current sensing in high-performance motor drives. However, most isolated modulators are designed for high-voltage applications, are reinforced isolated, and come in packages with >8mm clearance distance. The AMC0106Mxx modulators are specifically designed for low-voltage applications, are functionally isolated, and come in a small, 2.7mm x 3.5mm lead-less package with 1mm creepage and clearance. With the small package size, the AMC0106Mxx isolated modulators enable small PCB layouts that are essential for small form-factor motor drives in robotic applications. Figure 3-3 shows a layout comparison between a AMC1306Mxx reinforced isolated modulator and an AMC0106Mxx functionally isolated modulator. The AMC0106Mxx layout consumes only half the PCB area as it's AMC1306Mxx counter part.

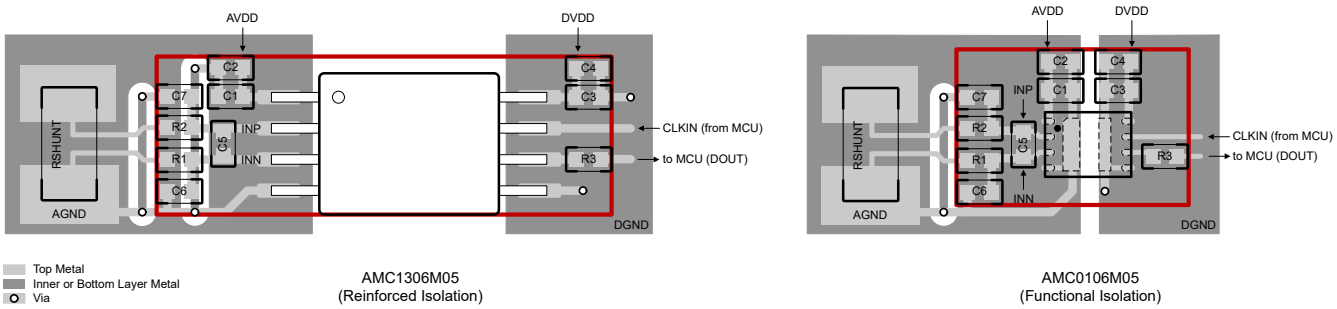


Figure 3-3. PCB Size Reduction AMC0106M05 versus AMC1306M05

3.2 Circuit Design and Layout

Figure 3-4 shows the schematic of the phase current sense subsystem using the functionally isolated modulator AMC0106M05 (U8) with a ±50mV linear input voltage range, and a 1mΩ, 3W shunt (R39). The 1mΩ shunt value determines that the linear input range is ±50A. The AMC0106M05 has a ±64mV clipping range, therefore the maximum current range is ±64A. The power dissipation in the shunt at $35A_{RMS}$ is 1.25W.

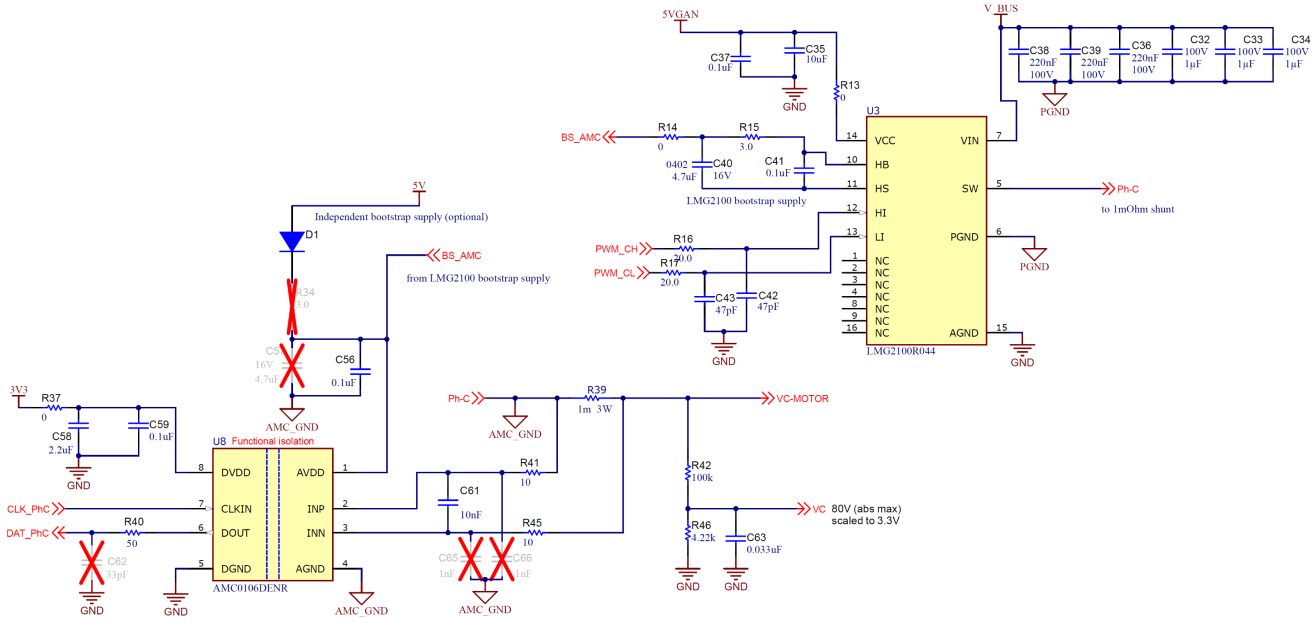


Figure 3-4. AMC0106M05 Schematic Using the LMG2100R44 Bootstrap Supply

The differential anti-aliasing low-pass filter (R41=10Ω, R45=10Ω, C61=10nF) in front of the isolated modulator has a cut-off frequency of 795kHz and helps to improve signal-to-noise performance of the signal path. The purpose of the low-pass filter is to attenuate high-frequency input noise below the desired noise level of the measurement. Without the input filter, noise close the sampling frequency (f_{CLKIN}), or multiples of the sampling frequency, is aliased to low-frequencies by the delts-sigma modulator and passes through the digital low-pass filter. The capacitors C65=1nF and C66=1nF are optional and improve common-mode input voltage rejection at

frequencies above 10MHz. C65 and C66 are sized 10x smaller than C61. For best performance, make sure C65 and C66 values match better than 5%. Mismatch between C65 and C66 causes differential input error during common-mode transients. NP0-type capacitors offer low temperature drift and are preferred for common-mode filtering.

The analog supply AVDD is decoupled with a 100nF capacitor, C56. AVDD is supplied by one of two bootstrap supply options. The default option leverages the LMG2100R044 bootstrap supply with C40=4.7µF and a current limit resistor R15=3Ω. The bootstrap diode is integrated into the LMG2100R044 GaN-FET. The AMC0106M05 typically draws 6.6mA from the AVDD supply. This configuration allows for operating at PWM frequencies from 10kHz to 100kHz with a maximum continuous duty cycle of a round 95%. Refer to the test results for more details.

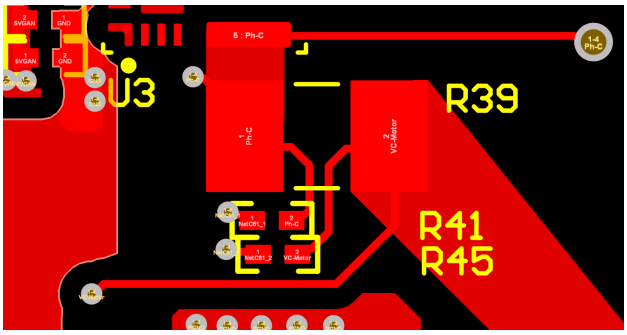
The resistor R14=0Ω is a configuration option to use a separate bootstrap supply. The resistor consists of an ultra fast rectifier diode D1, a 4.7µF capacitor C57 and a 3Ω current limit resistor R34, not populated with the default option.

The digital supply DVDD is decoupled with the capacitors C58=2.2µF and C59=100nF. A series 0Ω resistor (R37) is a placeholder for an optional ferrite bead. Ferrite beads help reduce coupling of transient load current spikes into the 3.3V plane and therefore improve EMI performance.

A 50Ω series line termination resistor R40 at the AMC0106M05 DOUT pin improves signal integrity. An optional capacitor C62=33pF allows for slew rate reduction of the modulator output bit-stream signal to further reduce EMI. For more information on improving the digital interface from an isolated modulator to a microcontroller refer to *Achieving Better Signal Integrity with Isolated Delta-Sigma Modulators in Motor Drives* and *Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs*.

Figure 3-5 shows the layout of the board with the shunt (R39) on the top-side of the PCB and the AMC0106M05 (U8) on the bottom side of the PCB. The shunt's terminals are connected to through a Kelvin connection to the two series input resistors R41 and R45 on the top layer. On the other side of the resistors, both signals are connected through vias to the corresponding input pins of the AMC0106M05 (INN and INP) that is placed on the bottom layer. The decoupling capacitor C61 is placed as close as possible to the input pins INN and INP and on the same layer as the AMC0106M05. The shunt terminal facing to the U3 LMG2100R044 GaN-FET's switch node (Ph-C) is connected through a via to the analog GND (AGND) pin of the AMC0106M05. The AVDD decoupling cap C56 is placed on the bottom layer close to the AVDD pin and connected to the AGND trace on the same layer.

PCB top layer (top view)



PCB bottom layer (bottom view)

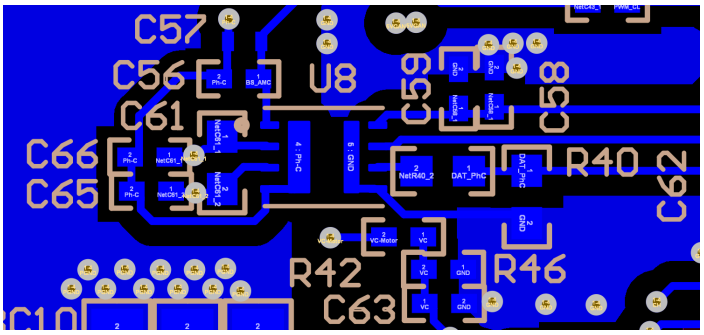


Figure 3-5. AMC0106M05 Top and Bottom Layer PCB Layout

3.3 Sinc^3 Filter Design

For testing, a sinc^3 filter was implemented on a TMS320F28379D Real-Time Microcontroller. A sinc^3 filter is a finite impulse response (FIR) filter with a constant propagation delay (group delay). The propagation delay depends on the sinc filter order, the sample clock frequency, and the oversampling ratio (OSR). For example, a sinc^3 filter with an 20MHz sample clock frequency and an oversampling ratio of 64 has a propagation delay of 4.8µs and a cut-off frequency f_{-3dB} of approximately 80kHz. The corresponding magnitude response and sampling window are shown in Figure 3-6 and Figure 3-7, respectively.

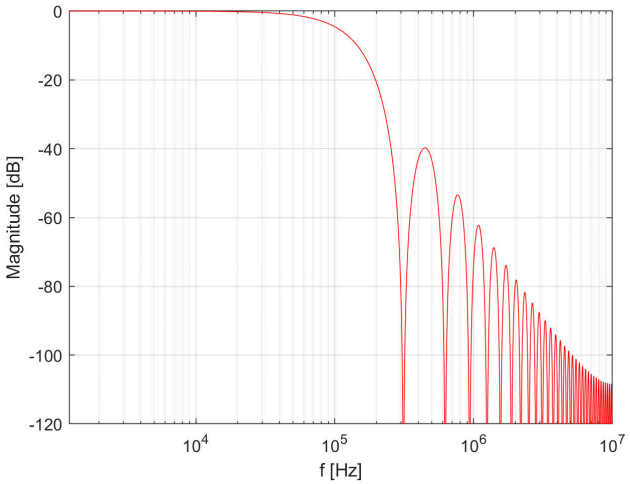


Figure 3-6. Magnitude Response, f_{mod} = 20MHz, sinc^3, OSR=64

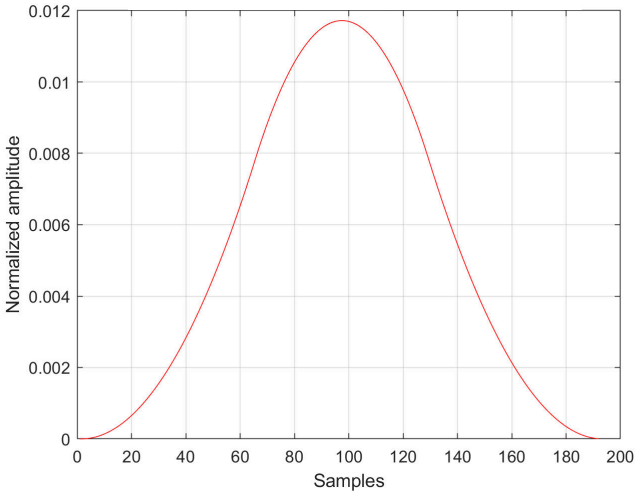


Figure 3-7. Sinc^3 OSR64 Filter Coefficients

An advantage of the delta-sigma approach is that short-circuit detection can be derived from the same modulator bit-stream by implementing a second decimation filter with a lower OSR and therefore lower latency. For example, a sinc^3 filter with an OSR of 8 running at a 20MHz sample rate, has a over-current response time (settling time) of only 1.2µs, as shown in Figure 3-8.

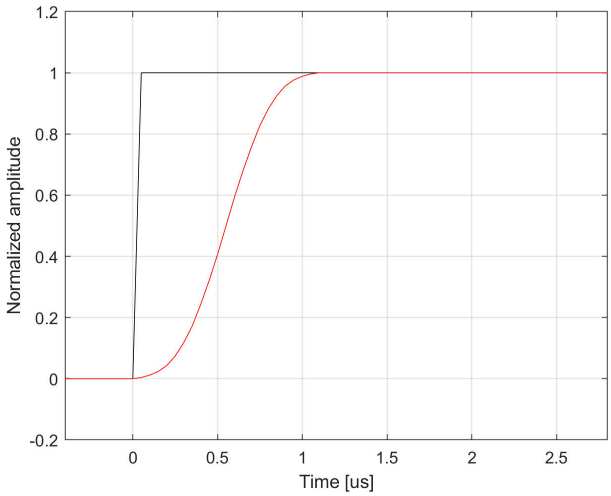


Figure 3-8. Step Response of a Sinc^3 OSR 8 Filter

For more details on how to implement sinc filters on a C2000™ microcontroller, see *Sigma Delta Filter Module (SDFM)*.

4 Test and Validation

4.1 Test Setup

A picture of the test setup is shown in Figure 4-1. The left side shows the overall setup with the top side view of the 3-phase GaN inverter. The right side shows the area on the bottom side of the PCB where the AMC0106M05 is placed.

In the following measurements phase notation U, V, W is used instead of the phase A, B, C notation used on the PCB design and schematic. For example, phase C on the schematic equals phase W in the measurement.

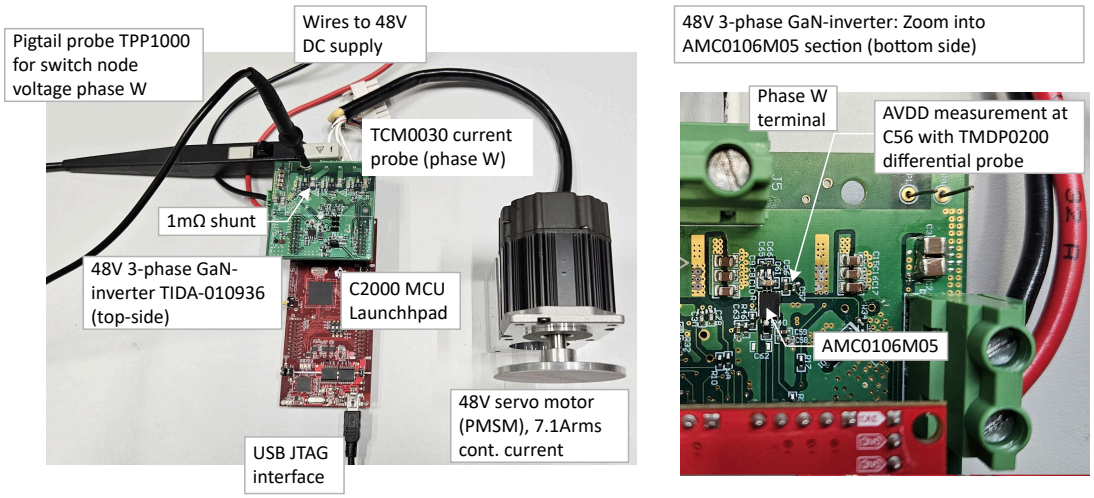


Figure 4-1. Picture of the Test Setup

4.2 Digital Interface

Figure 4-2 shows the timing of the digital interface. The AMC0106M05 is clocked at 20MHz. A new data bit is output on the rising edge of clock. The typical delay between the rising edge of clock to the rising (or falling) edge of data is 22ns. For information on how to optimize the setup and hold timing with the microcontroller, refer to *Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs*.

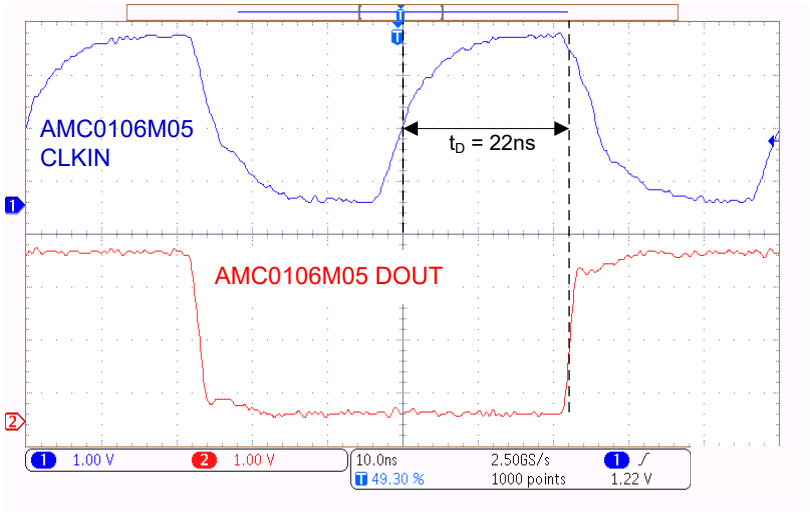


Figure 4-2. Digital Interface Timing

4.3 DC Accuracy, Noise, and Effective Number of Bits

A series of tests was performed to quantify measurement noise and the corresponding effective number of bits (ENOB) at different oversampling ratios and load currents. The ENOB was calculated from 1200 consecutive samples measured at the center of the 10kHz PWM over 1200 PWM periods. The PWM vector was kept constant during the test. The constant PWM vector produces constant phase voltage and DC current. The ENOB was calculated as follows:

$$ENOB = (20 \times \log_{10}(50A / noise_{RMS}) - 1.76) / 6.02 \quad (1)$$

where $noise_{RMS}$ equals the standard deviation of the 1200 measurements for a given OSR. Figure 4-3 shows the histograms for OSR 32, 64, 128, and 256 measured at a 3A DC current. The resulting ENOB as a function of OSR is shown in Figure 4-4.

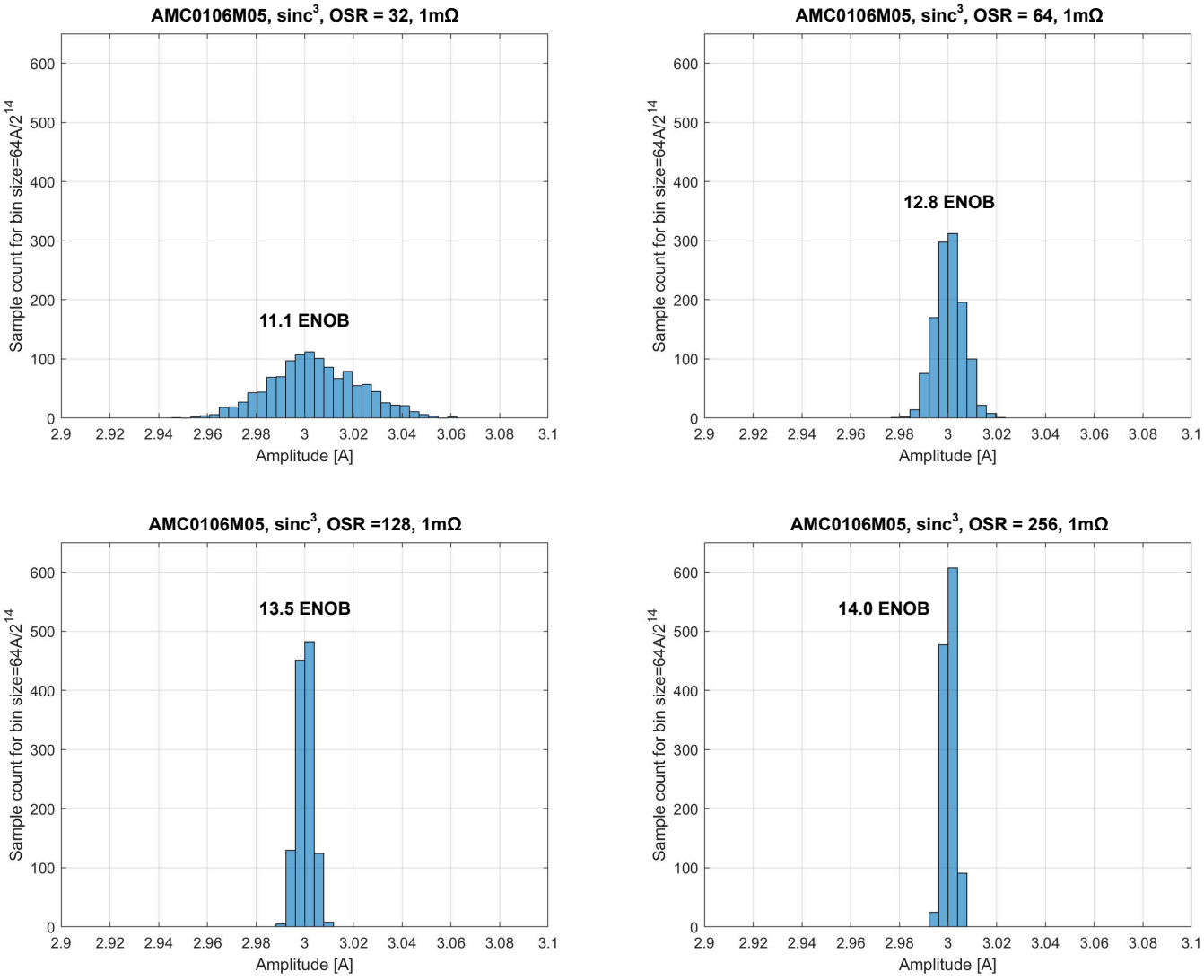


Figure 4-3. Phase Current Histograms for Different OSRs at 3A Phase Current

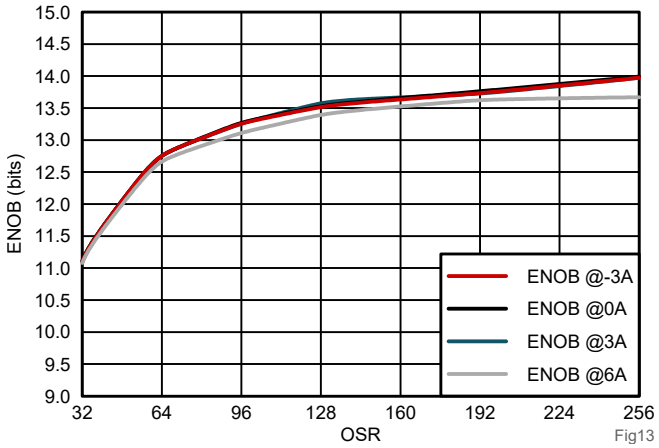


Figure 4-4. Phase Current ENOB vs. OSR

At OSR=32 the design already provides a resolution of 11.1 bit. There is no measurable difference between zero and 3A or 6A of current. As the OSR increases, the impact of system noise at larger phase currents becomes visible. For example, the ENOB at OSR 128 increases to 13.7 bit for smaller currents while slightly degrading to 13.5 bit at 6A. Table 4-1 summarizes the ENOB, noise, and latency measured at 3A with different OSRs.

Table 4-1. AMC0106M05 Measured Noise, ENOB and Latency vs OSR at 20MHz Modulator Clock

OSR	32	64	96	128	192	256
Noise(mA_{RMS})	18.4	5.93	4.14	3.46	2.94	2.51
ENOB (bit)	11.1	12.8	13.3	13.5	13.8	14
Latency (µs)	2.4	4.8	7.2	9.6	14.4	19.2

A sinusoidal phase current measurement is shown in the next chapter using a high 100kHz PWM frequency to demonstrate high measurement accuracy even during PWM switching.

4.4 PWM Rejection

A series of tests was performed to quantify the impact of common mode voltage transients during PWM switching on the measurement accuracy of the AMC0106M05.

4.4.1 DC Phase Current Measurement Over One PWM Cycle

For this test, the AMC0106M05 high-side supply (AVDD) was powered from the LMG2100R044 GaN-FET bootstrap supply which is the default configuration shown in Figure 3-4.

Figure 4-5 and Figure 4-6 show the PWM-switched phase voltage W at 3A phase current, measured with a current probe. The phase-W voltage equals the common mode voltage of the AMC0106M05 analog ground (AGND) versus the digital ground (DGND). The higher slew rate of 13V/ns during the transition from 0V to 48V is when the high-side GaN-FET is hard-switching, the lower slew rate of 2.7V/ns is during the transition from 48V to 0V, when the low-side GaN-FET is soft-switching (zero voltage switching). For more information on the switching characteristics of the GaN-FET, refer to the LMG2100R044 data sheet.

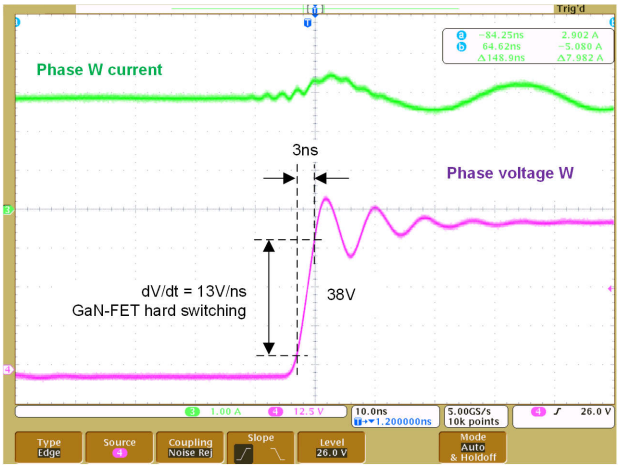


Figure 4-5. Phase W Voltage Rising Edge at 3A Current

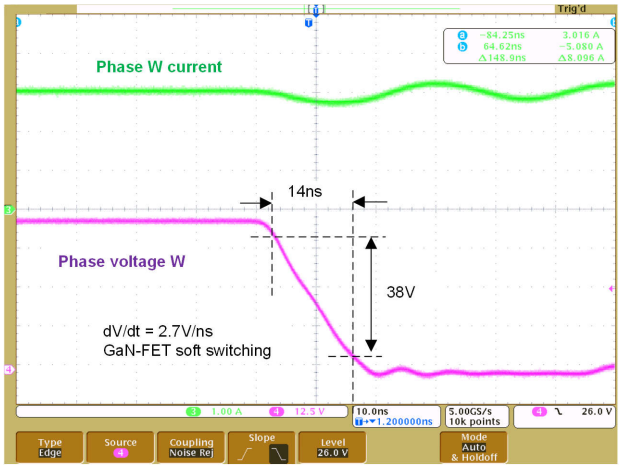


Figure 4-6. Phase W Voltage Falling Edge at 3A Current

Figure 4-7 shows a scope plot of the phase-W voltage, the phase current W (measured with a current probe) and the supply voltage AVDD for the AMC0106M05. The average phase-W current is 3A and the peak-to-peak current ripple is $0.4A_{PP}$, a function of the servo motor's stator time constant.

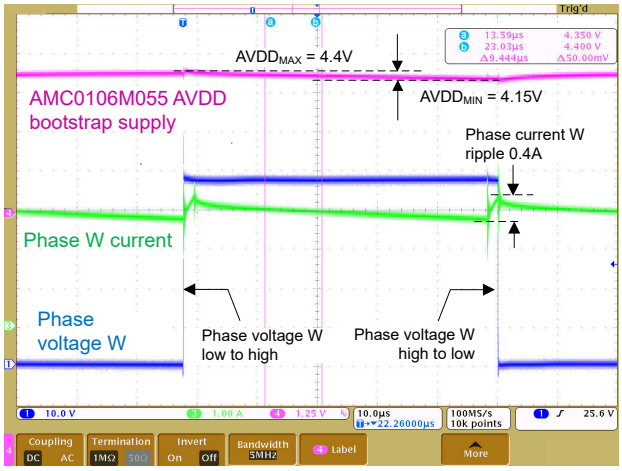


Figure 4-7. Phase W Voltage and Current Over One PWM Cycle

For the first test, a static 3-space vector PWM with a constant phase (330 degree) and voltage magnitude was impressed. The voltage magnitude was configured to force constant motor currents. For example, phase current W was set to I_W = 0A or 3A, while phase U and V currents were $I_U = I_V = –0.5 * I_W$.

To study the impact of PWM switching on the measurement accuracy of the AMC0106M05, the start of conversion of the $sinc^3$ filter was increased by 60ns for each new PWM period. The PWM frequency was 10kHz, the corresponding PWM period is 100µs. The effective sampling point of the first conversion started 14µs after the start of the first PWM cycle. For the seconds PWM cycle, the effective sampling point was 14.06µs. For the 600^{th} PWM period, the effective sampling point was 50µs (center aligned to the PWM). And the last sampling point, on the 1200^{th} PWM cycle, was set to 86µs. In a last step, the 1200 results were overlayed and plotted as a single PWM cycle.

The results for 3A phase current are shown in Figure 4-8. Results for 0A phase current are shown in Figure 4-9. In both cases the OSR was 32. Phase current is plotted on the left axis, phase voltage on the right axis.

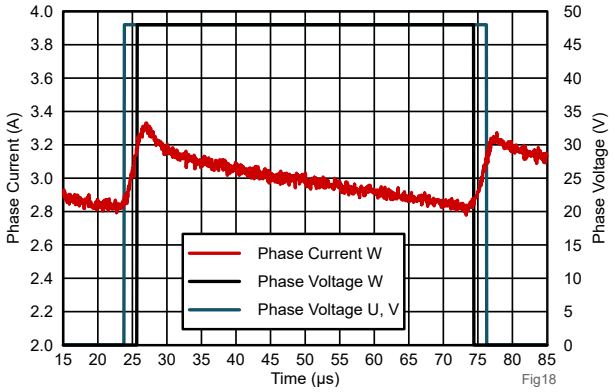


Figure 4-8. AMC0106M05 Phase Current I_W with OSR=32 at 3A Over one PWM Cycle

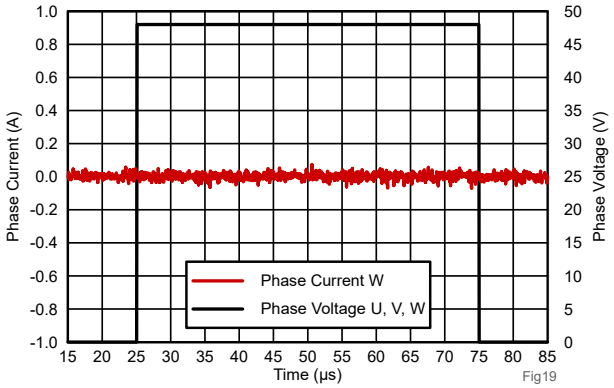


Figure 4-9. AMC0106M05 Phase Current I_W with OSR=32 at 0A Over one PWM cycle

At zero phase current there is no visible effect on the AMC0106M05 output signal during PWM switching of the phase. Neither the falling edge of the PWM with a low slew rate of 2.7V/ns, nor at the rising edge with a high slew rate of 13V/ns disturb the phase current measurement. This confirms the high common mode transient immunity (CMTI) of the AMC0106M05.

The AMC0106M05 phase current measurement was compared to a measurement with a current probe to validate the result. Both measurements are overlayed in Figure 4-10. Note that transient noise is seen with the current probe measurement (black trace), but not with the AMC0106M05 measurement (red trace).

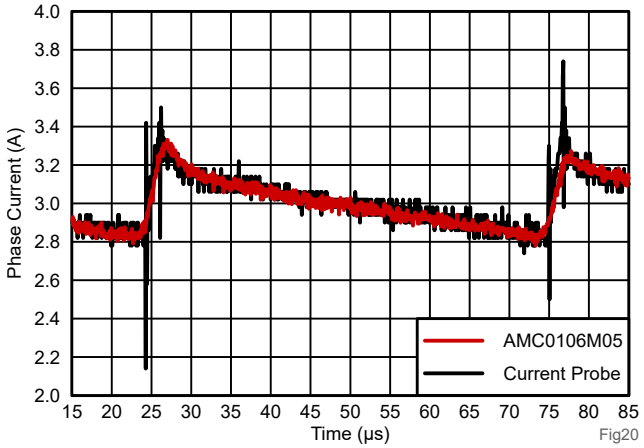


Figure 4-10. AMC0106M05 Phase Current I_W with OSR=32 at 3A versus Current Probe Measurement Over one PWM Cycle

The test was repeated with a 64-times oversampling ratio. As expected, the measurement noise with 64-times oversampling is significant lower. Even with this high-resolution measurement there is no effect visible of the PWM switching on the AMC0106M05 measurement accuracy.

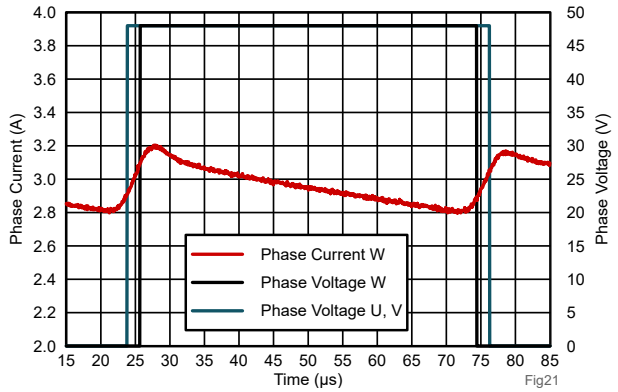


Figure 4-11. AMC0106M05 Phase Current I_W With OSR 64 at 3A Over one PWM Cycle

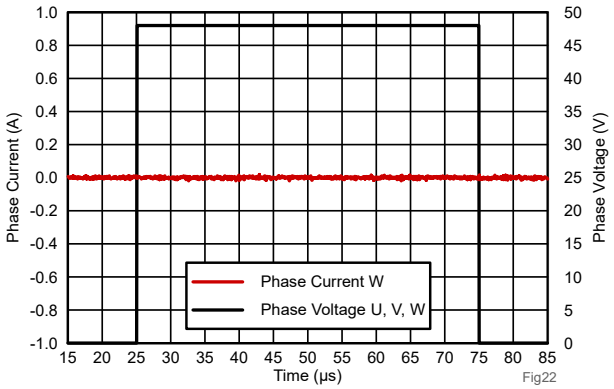


Figure 4-12. AMC0106M05 Phase Current I_W with OSR 64 at 0A Over one PWM Cycle

4.4.2 AC Phase Current Measurement at 100kHz PWM

For this test the PWM frequency was increased to 100kHz, with a corresponding PWM period of 10µs. A sinusoidal three-phase voltage with a frequency of 25Hz and a peak-to-peak PWM duty cycle of 10% was impressed, as shown in Figure 4-13. The phase-W voltage was measured with a pigtail voltage probe, the phase current with a current probe. The modulator clock frequency was 20MHz. The bitstream was filtered with a sync^3, OSR64 filter, which has a sampling window of 9.6µs. The sampling window of the delta-sigma modulator is almost as wide as the PWM period. Therefore PWM switching always occurs during the sampling time. Figure 4-14 shows the AMC0106M05 phase current measurement. Again, there is no effect of the PWM switching visible.

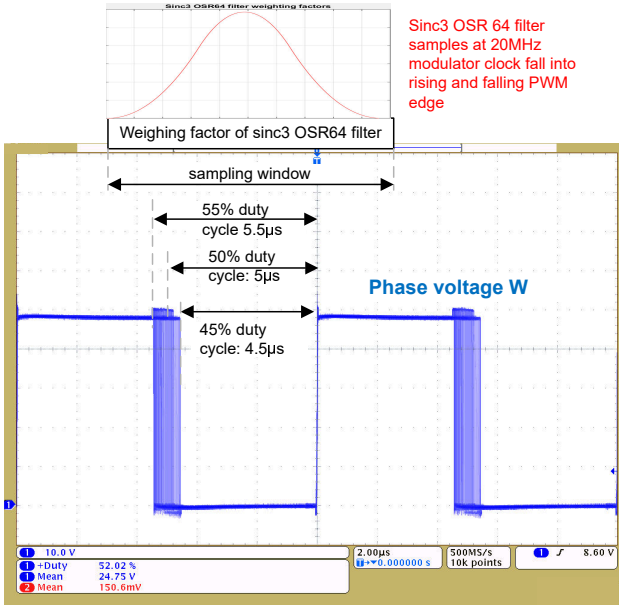


Figure 4-13. Scope Plot of Infinite Persistence Measurement of the Phase W Voltage

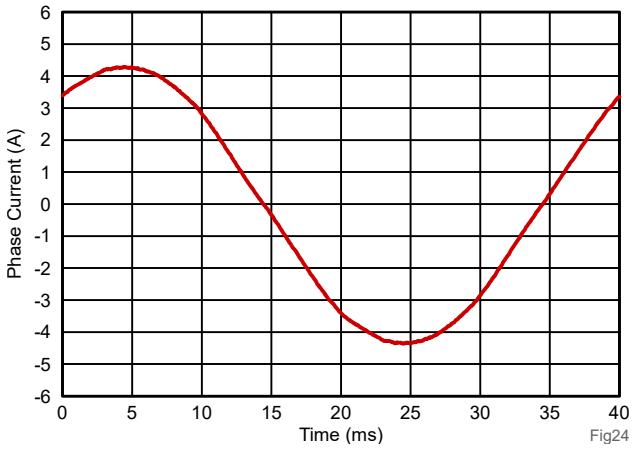


Figure 4-14. AMC0106M05 Phase Current I_W with OSR 64 at 100kHz PWM

4.5 Bootstrap Supply Validation and AVDD Ripple Rejection Tests

4.5.1 LMG2100R044 Bootstrap Supply With Low Voltage-Ripple

The following figures show the AVDD bootstrap supply voltage for a 10kHz and a 100kHz PWM at different PWM duty cycles. The bootstrap supply is implemented with the LMG2100R044 integrated bootstrap diode, the external bootstrap capacitors C41 (100nF), C40 (4.7µF) and the current limit resistor R15 (3Ω). The bootstrap supply drives the LMG2100R044 high-side GaN-FET, which has a typical gate charge of 7.3nC and supplies the AMC0106M05, which has a typical supply current of 6.5mA at 5V.

The bootstrap supply was tested at 10kHz and 100kHz PWM, at 50% duty cycle and constant 95% duty cycle as a worst-case condition.

Figure 4-15 and Figure 4-16 are generated from the csv files of the Tektronix MDO4104B-3 scope, using a TMDP0200 differential probe at a 75V sensitivity and 5MHz bandwidth.

The black trace shows the AVDD voltage referred to floating analog GND (AGND). The red trace shows the AGND common mode voltage in respect to system GND. System GND also equals logic GND (DGND) of the AMC0106M05 and the MCU GND.

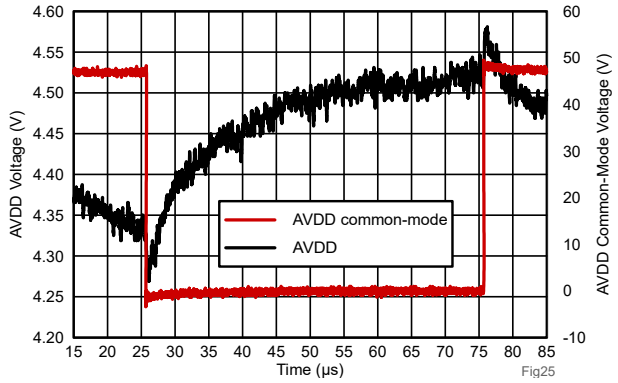


Figure 4-15. Bootstrap Voltage at 10kHz PWM, 50% Duty Cycle

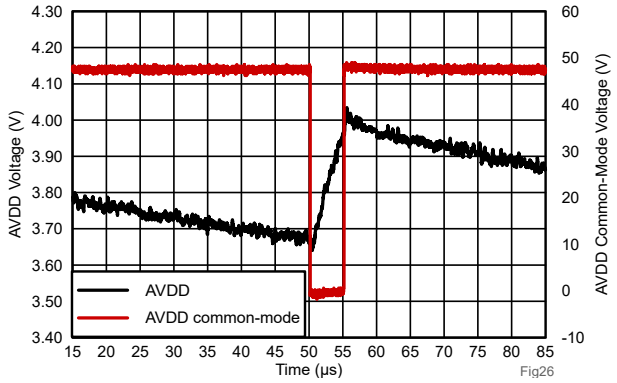


Figure 4-16. Bootstrap Voltage at 10kHz PWM, 95% Duty Cycle

Table 4-2. Bootstrap Voltage AVDD with R15 (3Ω),C57 (4.7µF) vs PWM Frequency and Duty Cycle

PWM Frequency (kHz)	Duty Cycle (%)	$AVDD_{MIN}$ (1) (V)	$AVDD_{MAX}$ (1) (V)	Δ_{AVDD} (V)	Mean (AVDD)(1) (V)
10	50	4.34	4.52	0.18	4.43
10	90	3.98	4.28	0.3	4.12
10	95	3.68	4	0.32	3.85
100	50	4.46	4.49	0.03	4.47
100	90	4.11	4.16	0.05	4.14
100	95	3.83	3.88	0.05	3.85

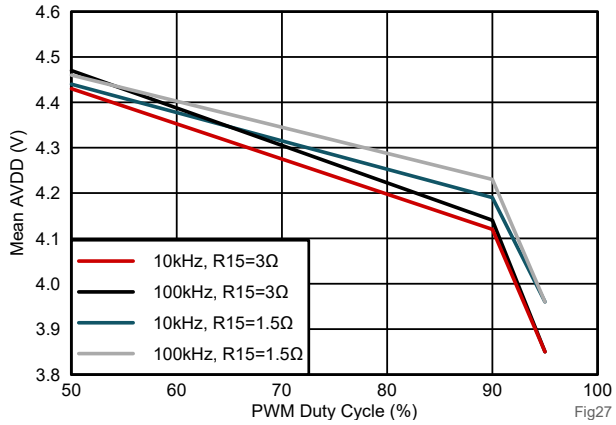


Figure 4-17. Mean AVDD Bootstrap Voltage

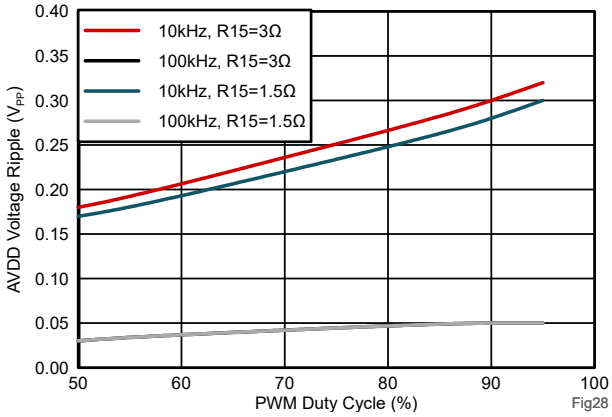


Figure 4-18. AVDD Bootstrap Voltage Ripple

Figure 4-17 shows that for a given current-limiting resistor (R15) the average bootstrap voltage decreases with lower PWM switching frequency. At lower PWM frequency, the boostrap capacitor has to support a longer ON-time of the high-side FET and, therefore, the average voltage decreases. At high duty cycles, meaning long ON-times of the high-side FET and short charging time of the bootstrap capacitor, the effect of R15 is visible. R15 limits the charging current of the boostrap capacitor. Therefore, at long duty cycles, the boostrap capacitor changes to a lower voltage. This effect can be compensated for by lowering the value of R15.

Figure 4-18 shows the peak-to-peak ripple voltage across the bootstrap capacitor as a function of duty cycle. Again, the ripple voltage increases with PWM duty cycle due to the longer ON-time of the high-side FET and the shorter refresh time of the bootstrap capacitor. For the calculation of mean bootstrap voltage the transient over-and undershoot was ignored. Over- and undershoots are caused by the limited common mode rejection of the differential voltage probe and not by the bootstrap supply.

The AMC0106M05 AVDD supply has a wide recommended operating range from 3V to 5.5V. Hence the bootstrap supply shown in above figures always meets the AMC0106M05 requirements. However, when operating from the LMG2100R044 GaN-FET bootstrap supply, the LMG2100R044 UVLO function has a maximum falling edge threshold 3.7V. The typical threshold is 3.0V. This needs to be considered for the desired PWM frequency and the corresponding maximum PWM cycle.

A smaller bootstrap resistor can be used to increase the minimum bootstrap voltage at high duty cycles. However, the bootstrap resistor has an impact on the peak charging currents. The LMG2100R044 internal bootstrap diode signal path has a dynamic resistance of 1.85Ω typical. The internal resistance has to be added to the external bootstrap resistance R15 to get the effective bootstrap resistance.

Table 4-3. Bootstrap Voltage AVDD with R15 (1.5Ω),C57 (4.7µF) vs PWM Frequency and Duty Cycle

PWM Frequency (kHz)	Duty Cycle (%)	$AVDD_{MIN}$ (1) (V)	$AVDD_{MAX}$ (1) (V)	Δ_{AVDD} (V)	Mean (AVDD)(1) (V)
10	50	4.35	4.51	0.17	4.44
10	90	4.05	4.33	0.28	4.19
10	95	3.83	4.13	0.3	3.96
100	50	4.44	4.48	0.04	4.46
100	90	4.2	4.25	0.05	4.23
100	95	3.93	3.98	0.05	3.96

(1) Does not include the transient undershoot and overshoot of 50mV during the falling edge of the phase-W voltage (bootstrap supply common mode voltage)

4.5.2 Discrete Bootstrap Supply With High Voltage-Ripple

For this test, the discrete bootstrap option, shown in Figure 4-19 was used. The default bootstrap supply was disconnected from the AMC0106M05 AVDD by removing R14. The discrete bootstrap supply consists of diode D1, the bootstrap resistor R34=3Ω, and the bootstrap capacitor C57=470pF. A very small value was intentionally chosen for C57 to generate a large bootstrap ripple voltage. The aim of the test was to evaluate how large AVDD supply voltage ripple affects the measurement accuracy of the AMC0106M05.

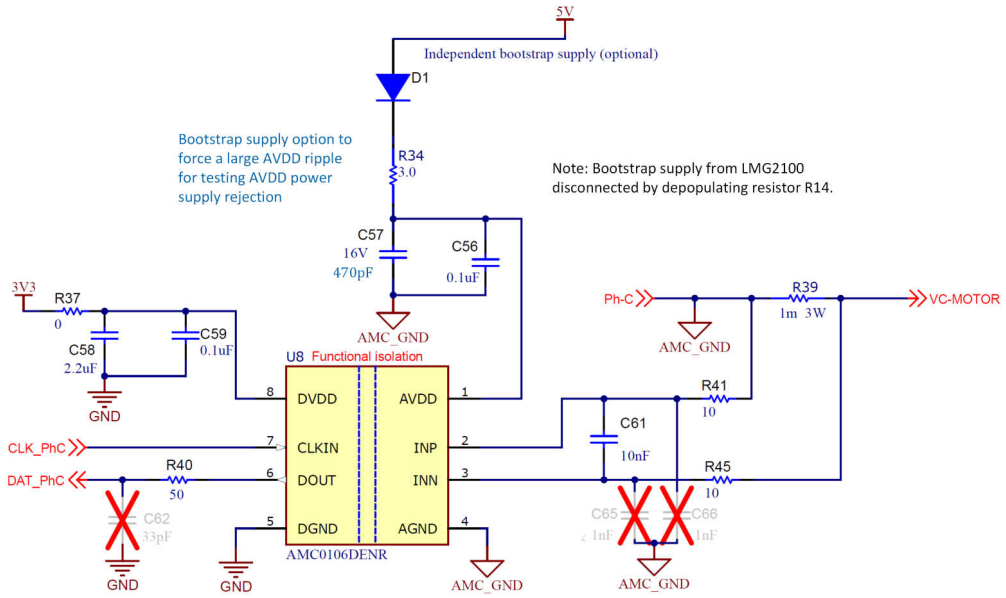


Figure 4-19. AMC0106M06 AVDD Bootstrap Configuration for This Test

Figure 4-20 shows the scope plot of the AVDD bootstrap supply voltage at a 10kHz PWM with 92.8% duty cycle. At this operating condition the off-time of the high-side GaN-FET, which equals the charging time of the bootstrap capacitor, was only 7.2µs.

The phase current measured with AMC0106M05 is identical to the measurement with the current probe. There is no performance degradation visible during the bootstrap charging time. The tolerance to high ripple voltage allows the use of smaller bootstrap capacitors, or, more importantly, operating at 100% duty cycle for longer periods of time.

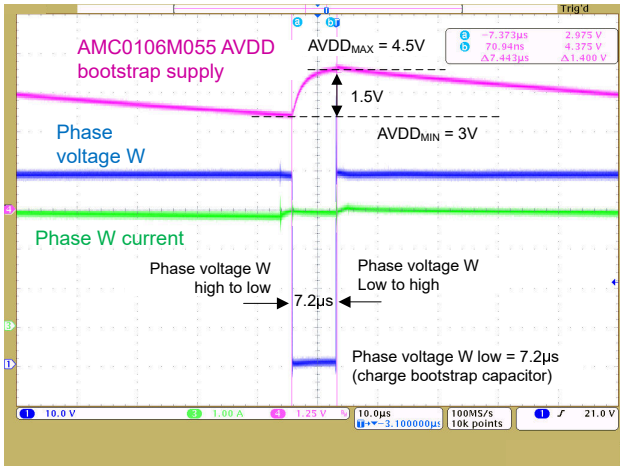


Figure 4-20. Phase W Voltage at 10kHz PWM with 92.8% Duty Cycle, Phase Current W and AMC0106M05 AVDD

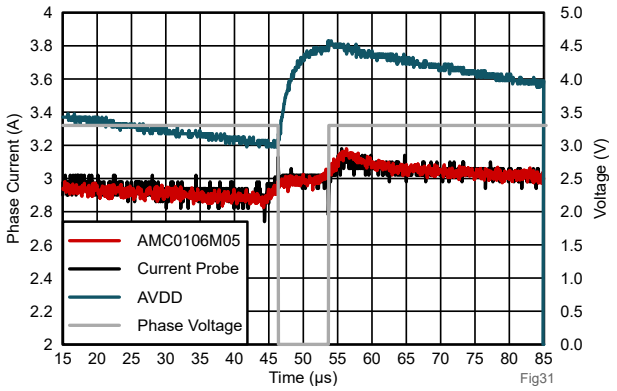


Figure 4-21. AMC0106M05 Measurement with OSR 32 at 3A vs Current Probe During Large AVDD Ripple

5 Summary

The newly released AMC0106Mxx family of functionally isolated modulators are the smallest, galvanically isolated modulators on the market today. The AMC0106Mxx come in a small, leadless package and enable high accuracy, low noise phase current sensing in a much smaller design size than what has been achievable so far. The AMC0106Mxx's high common mode voltage transient immunity, excellent power-supply rejection, digital interface to the MCU, and the inherent immunity to magnetic stray fields, make sure of accurate current measurement even during PWM switching. Supporting ambient operating temperature range up to 125°C, the AMC0106Mxx is an excellent choice for space constrained, motor-integrated, sub-60V three-phase inverter designs. Typical applications are 48V servo drives and collaborative or humanoid robots, where high performance, robust current measurement and a small form factor is important.

6 References

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3. Texas Instruments, *Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs*, application note.
4. Texas Instruments, C2000 Academy, *Sigma Delta Filter Module (SDFM)*
5. Texas Instruments, *48V/16A Small Form Factor Three-Phase GaN Inverter Reference Design for Integrated Motor Drives*, design guide.
6. Texas Instruments, Analog Design Journal, *Selecting Amplifiers for Shunt-Based Current Sensing in 3-Phase Motor Drives*, design guide.
7. Texas Instruments, *Designing a Bootstrap Charge-Pump Power Supply for an Isolated Amplifier*, application note.
8. Texas Instruments, *F28379D LaunchPad™ development kit for C2000™ Delfino™ MCU*
9. Texas Instruments, *C2000™ real-time MCU F28P65x LaunchPad™ Development kit*
10. Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity*, application note.

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