*Application Note*

# *TLV320ADCx140/PCMx140-Q1 Programmable Biquad Filter Configuration and Applications*

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**ABSTRACT**

The TLV320ADCx140/PCMx140-Q1 device family (TLV320ADC3140, TLV320ADC5140, TLV320ADC6140, and PCM3140-Q1, PCM5140-Q1, PCM6140-Q1) is a quad-channel, high-performance, analog-to-digital converter (ADC) for audio applications. This family of devices has an extensive set of features that includes the following:

- Multi-channel, multi-bit, high-performance delta-sigma ADC
- Configurable single-ended or differential audio inputs.
- A low-noise programmable microphone bias voltage output.
- An integrated low-jitter phase-locked loop (PLL)
- Linear phase or Low-latency decimation filters with sample rates up to 768 kHz
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable channel gain
- Digital volume control
- Digital channel mixer
- A programmable high-pass filter (HPF)
- A programmable Infinite Impulse Response Biquad filters
- Automatic Gain Controller (AGC)
- Dynamic Range Enhancer (DRE) support in TLV320ADC5140/PCM5140-Q1 and TLV320ADC6140/PCM6140-Q1.
- Pulse density modulation (PDM) digital microphone interface with high-performance decimation filters.

This application note describes how to configure the programmable Infinite Impulse Response (IIR) Digital Biquad Filters of the TLV320ADCx140/PCMx140-Q1 devices.

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## 1 Introduction

Each channel of the TLV320ADCx140/PCMx140-Q1 device follows the signal chain shown in Figure 1-1. In this signal chain, each channel supports an analog differential or single-ended signal or a digital pulse density modulation (PDM) digital microphone. In TLV320ADCx140/PCMx140-Q1 device families, the analog input signal is amplified by a Programmable Gain Amplifier (PGA) and then converted by a high-performance ADC into a digital signal. The PGA gains the input signal to match the full scale of the ADC. The digital signal has a programmable phase calibration to adjust the phase delay of each channel in steps of one modulator clock cycle. This allows the system to match the phase across different channels. The phase-calibrated digital signal is then decimated through a set of linear phase filters or low-latency filters. DC offset is removed from the decimated signal through a Digital High-Pass Filter (HPF) with three pre-set cutoff frequencies or a fully programmable cutoff frequency. Note that DC shifts are caused by mismatches in common-mode voltages. The output of the HPF is gain calibrated with 0.1-dB steps and summed with other channels. The gain calibration matches the gain across different channels, particularly if the channels have microphones with varying gain values. The output is then filtered by the Digital Biquad Filters and gained by the volume control.

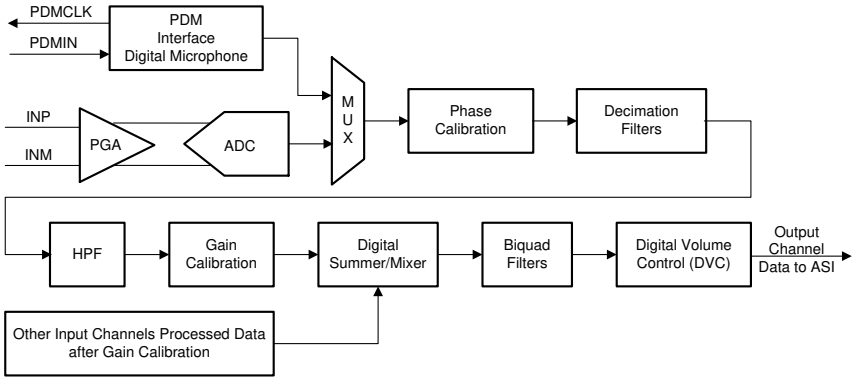


**Figure 1-1. TLV320ADCx140/PCMx140-Q1 Channel Signal Chain Processing Flow Chart**

This application note concentrates on how to configure the Digital Biquad Filters. The Digital Biquad Filters are digitally implemented as a set of IIR filters.

## 2 Infinite Impulse Response Filters

Equation 1 specifies the transfer function of infinite impulse response filters (IIR).

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + ... + b_M z^{-M}}{1 + a_1 z^{-1} + a_2 z^{-2} + ... + a_N z^{-N}} \quad (1)$$

When the coefficients of this transfer function are quantized for fixed point implementations, the resulting errors due to quantization and the recursive nature of the filter can significantly alter the desired filter characteristics and lead to instability. Partitioning this transfer function into a set of cascaded lower-order filters reduces the sensitivity to coefficient quantization. Cascaded Biquad IIR filter implementations have been proven to be effective in minimizing these effects.

### 2.1 Digital Biquad Filter

A Digital Biquad Filter is a second-order IIR filter with two poles and two zeros. *Biquad* is an abbreviation of *biquadratic*. Thus, a Digital Biquad Filter is an IIR filter whose transfer function is the ratio of two quadratic functions given by Equation 2 and the corresponding direct form II block diagram shown in Figure 2-1. In this equation, the coefficients are normalized so that $a_0 = 1$ through the division of all the coefficients by $a_0$.

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \quad (2)$$

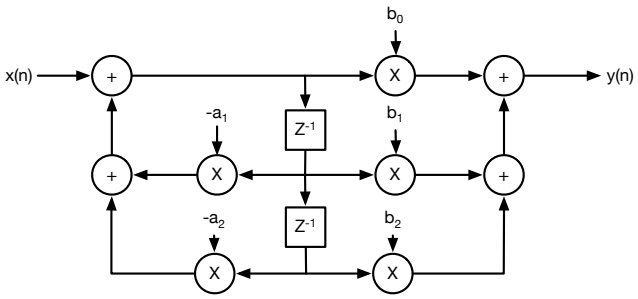


**Figure 2-1. Direct Form II Biquad Filter**

# 3 TLV320ADCx140/PCMx140-Q1 Digital Biquad Filters

The TLV320ADCx140/PCMx140-Q1 devices support up to three programmable Digital Biquad Filters in the signal chain of each channel shown in Figure 1-1. The programmable Biquad Filters lie between the Digital Summer and the Digital Volume Control blocks. The Biquad Filters allow for custom low-pass, high-pass, or any other desired frequency shaping of the signal. By default, the frequency response for each Biquad Filter is an all-pass filter, meaning a frequency response with flat gain of 0 dB. A host can override the frequency response of these Biquad filters by changing the programmable coefficients of each Biquad Filter. To change the coefficients, the host must write the Biquad Filters coefficients before powering any ADC channels.

Equation 3 shows the quantized 32-bit transfer function implemented in the TLV320ADCx140/PCMx140-Q1 . The coefficients of these biquad filters [$N_0$, $N_1$, $N_2$, $D_1$, and $D_2$] are each 32-bits wide, in 2s-complement format, and occupy four consecutive 8-bit registers in the TLV320ADCx140/PCMx140-Q1 register space. With the Q-point in the 31$^{st}$ bit location (Q31), the filter coefficients are in 1.31 format with a range from –1 (0x80000000) to 0.9999999995 (0x7FFFFFFF). In this notation, the decimal point is assumed to be between bit 30 and bit 31. Bit 31 contains the sign bit, while bits 30-0 contain the fractional bits as shown in Figure 3-1. With this notation, all coefficients are normalized to less than 1. To convert a floating point number less than one to Q31 format, multiply the floating point number by $2^{31}$ and truncate to the nearest integer. With this notation, the number 1, corresponding to $a_0$ in the denominator, becomes $2^{-31}$ (0x7FFFFFF). Note that the coefficients $N_1$ and $D_1$ are multiplied by two. Thus, when using a digital filter design package to calculate these coefficients, divide by 2 the $N_1$ and $D_1$ before writing these coefficient registers. Also, note that coefficients $D_1$ and $D_2$ have a negative sign. So, multiply by –1 before writing $D_1$ and $D_2$ to the coefficient registers when using a digital filter design package.

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} - D_2 z^{-2}} \quad (3)$$

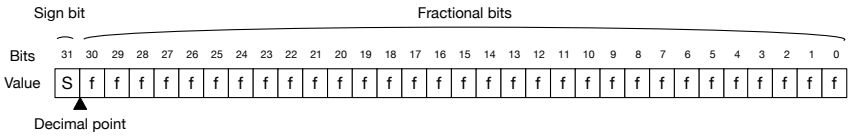


**Figure 3-1. Q-31 Format Representation**

## 3.1 Filter Design Using PurePath™ Console

To facilitate the use of the Digital Biquad Filters, the PurePath™ Console includes a graphical filter design section that plots the magnitude, phase, and group delay versus frequency. This filter design also generates the coefficients through several different filter design techniques filters. Equation 3 shows the available filter design options with a short description of the filter type. In Table 3-1, the cutoff frequency refers to the frequency when the response changes by 3 dB from the passband.

**Table 3-1. PurePath™ Console Digital Biquad Filter Options**

| FILTER TYPE | DESCRIPTION |
|---|---|
| Band Pass | Band-Pass filter at the specified center frequency and passband width (filter bandwidth) |
| Bass Shelf | Specified gain applied at the low frequency up to the specified cutoff frequency |
| Equalizer (Bandwidth) | Band-pass filters at the specified center frequency and passband width, with the specified gain |
| Equalizer (Q Factor) | Band-pass filter at the specified center frequency and quality factor, with the specified gain. The quality factor is the center frequency divided by the passband width. |
| Gain | All pass filter at the specified gain |
| High-Pass Butterworth 1 | First-order high-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –10 dB / decade slope. |
| High-Pass Butterworth 2 | Second-order high-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –20 dB / decade. |
| High-Pass Bessel 2 | Second-order high-pass filter with specified gain, specified cutoff frequency, maximally flat phase and constant group delay across passband. |

**Table 3-1. PurePath™ Console Digital Biquad Filter Options (continued)**

| FILTER TYPE | DESCRIPTION |
|---|---|
| High-Pass Linkwitz Riley 2 | Second-order high-pass filter composed of a Butterworth filter with –3 dB at the cutoff frequency. When cascading a low-pass and high-pass Linkwitz Riley filters, the overall gain at the crossover frequency is 0 dB. |
| High-Pass Variable Q 2 | Second-order high-pass filter at the specified center frequency, gain, and quality factor. The quality factor is the center frequency divided by the passband width. |
| High-Pass Chebyshev | High-pass filter with equiripple in the passband with maximally flat response in stopband |
| Low-Pass Butterworth 1 | First-order low-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –10 dB / decade slope. |
| Low-Pass Butterworth 2 | Second-order low-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –20 dB / decade. |
| Low-Pass Bessel 2 | Second-order low-pass filter with specified gain, specified cutoff frequency, maximally flat group delay across passband |
| Low-Pass Linkwitz Riley 2 | Second-order low-pass filter composed of a Butterworth filter with –3 dB at the cutoff frequency. When cascading a low-pass and high-pass Linkwitz Riley filters, the overall gain at the crossover frequency is 0 dB. |
| Low-Pass Variable Q 2 | Second-order low-pass filter at the specified center frequency, gain and quality factor. The quality factor is the center frequency divided by the passband width. |
| Low-Pass Chebyshev | Low-pass filter with equiripple in the passband with maximally flat response in stopband |
| Notch | Band stop filter at the specified center frequency and stopband width (filter bandwidth) |
| Phase Shift | All pass filter with 180 degree phase shift at the specified center frequency through the width given by the bandwidth |
| Treble Shelf | Specified gain applied at the high frequencies past the specified cutoff frequency |

### 3.1.1 Example Generating Programmable Biquad Coefficients Using PurePath™ Console

Figure 3-2 shows how to create a set of filters for 5-dB boost at 500 Hz with bandwidth of 400 Hz, cut –5 dB at 2 kHz with 3-kHz bandwidth, and a Notch filter at 60 Hz with 50-Hz bandwidth for channel 1. Note that each biquad filter is color coded. The cyan color refers to BQ1 500-Hz equalizer, light gray to BQ5 2 kHz, and brown to BQ9 Notch filter at 60 Hz. The overall response of all three filters is plotted in red. Note that cutoff or center frequencies are marked on the graph to allow you to drag and move the center frequencies of the filters. The graphical plots allows users to zoom in and out of the frequency response plot and choose logarithmic or linear frequency axis, plot gain, phase, group delay, or impulse response.


**Figure 3-2. PurePath™ Console Programmable Biquad Filter Example**

Clicking on the swivel arrow at each biquad shows the normalized floating point coefficients for $N_0$, $N_1$, $N_2$, $D_1$, and $D_2$ of Equation 3, as shown in Figure 3-3. Note the PurePath Console has computed the floating point coefficients $b_0$, $b_1$, $b_2$, $a_1$, and $a_2$ of Equation 2 and converted into the necessary values for $N_0$, $N_1$, $N_2$, $D_1$, and $D_2$. Clicking the **Apply** button transmits the coefficients through I2C to the TLV320ADCx140/PCMx140-Q1 devices on the EVM.


**Figure 3-3. PurePath™ Console Programmable Biquad Filter Example Showing the Computed Coefficients in Normalized Floating Point Format**

## 3.2 How to Generate $N_0$, $N_1$, $N_2$, $D_1$, and $D_2$ Coefficients with a Digital Filter Design Package

When using a Digital Filter Design Package, such as MatLab®, to generate an IIR biquad coefficients follow these steps:

1. Compute the coefficients [$b_0$, $b_1$, $b_2$, $a_0$, $a_1$, $a_2$] with a filter design function, such as the Matlab butter function to design a Butterworth filter with cutoff at 1 kHz of a system running at 48 kHz. Note that Matlab coefficients are normalized with $a_0 = 1$.

```
[b, a] = butter( 2, 1000 / (48000/2) )
```

2. Convert these coefficients to [$N_0$, $N_1$, $N_2$, $D_1$, $D_2$] by dividing:
   - $N_0 = b_0$
   - $N_1 = b_1 \div 2$
   - $N_2 = b_2$
   - $D_1 = -a_1 \div 2$
   - $D_2 = -a_2$
3. Convert the coefficients to Q31 by multiplying by $2^{31}$.
4. Round to nearest integer and convert to a 32-bit two's complement hexadecimal format:
   - For positive integers, convert to hexadecimal format.
   - For negative integers, take the absolute value of the coefficient, convert it to binary, negate it, add one, and convert to hex.

## 3.3 Avoid Overflow Conditions

When cascading several biquad filters that gain the signal, make sure the overall response of the system does not cause the system to overflow. The biquads are computed in 32-bit fixed point arithmetic. If the overall response of the system in conjunction with the input signal is too large, undesired results can result due to arithmetic saturation. If saturation or overflow occurs, scale the input signal or scale down the coefficients of one or more biquads to keep the overall response of the system from saturating or overflowing.

Note that the overall response of the system is dependent on all the enabled components of the signal chain. The Digital High-Pass filter changes the frequency response at the low frequencies in conjunction with the Digital Biquad Filter response since both of these filters are cascaded together.

## 3.4 Digital Biquad Filter Allocation to Output Channel

Table 3-2 shows the assignment of these biquad filters to a specific output channel based on the BIQUAD_CFG[1:0] register setting of DSP_CFG1 register. Setting BIQUAD_CFG[1:0] to 2'b00 disables the Digital Biquad Filters for all channels. Select this setting when no additional filtering is needed for the system application. Table 3-2 also shows the mapping of the biquad filter coefficients in the TLV320ADCx140/PCMx140-Q1 register space.

**Table 3-2. Biquad Filter Allocation to the Record Output Channel**

| Programmable Biquad Filter | Record Output Channel Allocation Using DSP_CFG1 Register Setting | | |
|---|---|---|---|
| | BIQUAD_CFG[1:0] = 2'b01 (1 Biquad per Channel) | BIQUAD_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel) | BIQUAD_CFG[1:0] = 2'b11 (3 Biquads per Channel) |
| | Supports all 8 Channels | Supports up to 6 Channels | Supports up to 4 Channels |
| Biquad filter 1 | Allocated to output channel 1 | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 2 | Allocated to output channel 2 | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 3 | Allocated to output channel 3 | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 4 | Allocated to output channel 4 | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 5 | Not used | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 6 | Not used | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 7 | Not used | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 8 | Not used | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 9 | Allocated to output channel 5 | Allocated to output channel 5 | Allocated to output channel 1 |
| Biquad filter 10 | Allocated to output channel 6 | Allocated to output channel 6 | Allocated to output channel 2 |
| Biquad filter 11 | Allocated to output channel 7 | Allocated to output channel 5 | Allocated to output channel 3 |
| Biquad filter 12 | Allocated to output channel 8 | Allocated to output channel 6 | Allocated to output channel 4 |

Table 3-3 shows the biquad filter coefficients mapping to the register space.

**Table 3-3. Biquad Filter Coefficients Register Mapping**

| Programmable Biquad Filter | Biquad Filter Coefficients Register Mapping | Programmable Biquad Filter | Biquad Filter Coefficients Register Mapping |
|---|---|---|---|
| Biquad filter 1 | P2_R8-R27 | Biquad filter 7 | P3_R8-R27 |
| Biquad filter 2 | P2_R28-R47 | Biquad filter 8 | P3_R28-R47 |
| Biquad filter 3 | P2_R48-R67 | Biquad filter 9 | P3_R48-R67 |
| Biquad filter 4 | P2_R68-R87 | Biquad filter 10 | P3_R68-R87 |
| Biquad filter 5 | P2_R88-R107 | Biquad filter 11 | P3_R88-R107 |
| Biquad filter 6 | P2_R108-R127 | Biquad filter 12 | P3_R108-R127 |

The DSP_CFG1 Register also determines the number of biquads used through the BIQUAD_CFG bit field shown in Table 3-4 and Table 3-5.

**Table 3-4. TLV320ADC3140 DSP_CFG1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DVOL_GANG | BIQUAD_CFG[1:0] | | DISABLE_ SOFT_STEP | AGC_SEL | Reserved | | |
| R/W-0h | R/W-2h | | R/W-0h | R/W-0h | R/W-0h | | |

**Table 3-5. TLV320ADC5140 and TLV320ADC6140 DSP_CFG1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DVOL_GANG | BIQUAD_CFG[1:0] | | DISABLE_ SOFT_STEP | AGC_ DRE_AGC_SEL | Reserved | | |
| R/W-0h | R/W-2h | | R/W-0h | R/W-0h | R/W-0h | | |

**Table 3-6. DSP_CFG1 Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | DVOL_GANG | R/W | 0h | DVOL control ganged across channels<br>0d = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits<br>1d = All active channels must use the channel 1 DVOL setting (CH1_DVOL) irrespective of whether channel 1 is turned on or not |
| 6-5 | BIQUAD_CFG[1:0] | R/W | 2h | Number of biquads per channel configuration<br>0d = No biquads per channel; biquads are all disabled<br>1d = 1 biquad per channel<br>2d = 2 biquads per channel<br>3d = 3 biquads per channel |
| 4 | DISABLE_SOFT_STEP | R/W | 0h | Soft-stepping disable during DVOL change, mute, and unmute<br>0d = Soft-stepping enabled<br>1d = Soft-stepping disabled |
| 3 | AGC_SEL (TLV320ADC3140) | R/W | 0h | AGC selection when is enabled for any channel.<br>0d = AGC is not selected<br>1d = AGC is selected |
| | DRE_AGC_SEL (TLV320ADC5140 and TLV320ADC6140) | | | DRE or AGC selection when is enabled for any channel.<br>0d = DRE is selected<br>1d = AGC is selected |
| 2-0 | Reserved | R/W | 0h | Reserved |

## 3.5 Programmable Coefficient Registers for Digital Biquad Filters 1–6

Table 3-7 shows the programmable coefficient registers for the biquad filters 1 through 6 in Page 2 of the TLV320ADCx140/PCMx140-Q1 registers.

**Table 3-7. Page 0x02 Programmable Coefficient Registers for Biquad Filters 1–6**

| Page 0x2 Address | Register | Reset Value | Biquad Filter | Coefficient | Description |
|---|---|---|---|---|---|
| 0x00 | PAGE[7:0] | 0x00 | | | Device Page Register |
| 0x08 | BQ1_N0_BYT1[7:0] | 0x7F | Programmable Biquad 1 | N0 | Biquad 1, N0 coefficient byte[31:24] |
| 0x09 | BQ1_N0_BYT2[7:0] | 0xFF | | | biquad 1, N0 coefficient byte[23:16] |
| 0x0A | BQ1_N0_BYT3[7:0] | 0xFF | | | biquad 1, N0 coefficient byte[15:8] |
| 0x0B | BQ1_N0_BYT4[7:0] | 0xFF | | | biquad 1, N0 coefficient byte[7:0] |
| 0x0C | BQ1_N1_BYT1[7:0] | 0x00 | | N1 | biquad 1, N1 coefficient byte[31:24] |
| 0x0D | BQ1_N1_BYT2[7:0] | 0x00 | | | Biquad 1, N1 coefficient byte[23:16] |
| 0x0E | BQ1_N1_BYT3[7:0] | 0x00 | | | Biquad 1, N1 coefficient byte[15:8] |
| 0x0F | BQ1_N1_BYT4[7:0] | 0x00 | | | Biquad 1, N1 coefficient byte[7:0] |
| 0x10 | BQ1_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 1, N2 coefficient byte[31:24] |
| 0x11 | BQ1_N2_BYT2[7:0] | 0x00 | | | Biquad 1, N2 coefficient byte[23:16] |
| 0x12 | BQ1_N2_BYT3[7:0] | 0x00 | | | Biquad 1, N2 coefficient byte[15:8] |
| 0x13 | BQ1_N2_BYT4[7:0] | 0x00 | | | Biquad 1, N2 coefficient byte[7:0] |
| 0x14 | BQ1_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 1, D1 coefficient byte[31:24] |
| 0x15 | BQ1_D1_BYT2[7:0] | 0x00 | | | Biquad 1, D1 coefficient byte[23:16] |
| 0x16 | BQ1_D1_BYT3[7:0] | 0x00 | | | Biquad 1, D1 coefficient byte[15:8] |
| 0x17 | BQ1_D1_BYT4[7:0] | 0x00 | | | Biquad 1, D1 coefficient byte[7:0] |
| 0x18 | BQ1_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 1, D2 coefficient byte[31:24] |
| 0x19 | BQ1_D2_BYT2[7:0] | 0x00 | | | Biquad 1, D2 coefficient byte[23:16] |
| 0x1A | BQ1_D2_BYT3[7:0] | 0x00 | | | Biquad 1, D2 coefficient byte[15:8] |
| 0x1B | BQ1_D2_BYT4[7:0] | 0x00 | | | Biquad 1, D2 coefficient byte[7:0] |
| 0x1C | BQ2_N0_BYT1[7:0] | 0x7F | Programmable Biquad 2 | N0 | Biquad 2, N0 coefficient byte[31:24] |
| 0x1D | BQ2_N0_BYT2[7:0] | 0xFF | | | Biquad 2, N0 coefficient byte[23:16] |
| 0x1E | BQ2_N0_BYT3[7:0] | 0xFF | | | Biquad 2, N0 coefficient byte[15:8] |
| 0x1F | BQ2_N0_BYT4[7:0] | 0xFF | | | Biquad 2, N0 coefficient byte[7:0] |
| 0x20 | BQ2_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 2, N1 coefficient byte[31:24] |
| 0x21 | BQ2_N1_BYT2[7:0] | 0x00 | | | Biquad 2, N1 coefficient byte[23:16] |
| 0x22 | BQ2_N1_BYT3[7:0] | 0x00 | | | Biquad 2, N1 coefficient byte[15:8] |
| 0x23 | BQ2_N1_BYT4[7:0] | 0x00 | | | Biquad 2, N1 coefficient byte[7:0] |
| 0x24 | BQ2_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 2, N2 coefficient byte[31:24] |
| 0x25 | BQ2_N2_BYT2[7:0] | 0x00 | | | Biquad 2, N2 coefficient byte[23:16] |
| 0x26 | BQ2_N2_BYT3[7:0] | 0x00 | | | Biquad 2, N2 coefficient byte[15:8] |
| 0x27 | BQ2_N2_BYT4[7:0] | 0x00 | | | Biquad 2, N2 coefficient byte[7:0] |
| 0x28 | BQ2_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 2, D1 coefficient byte[31:24] |
| 0x29 | BQ2_D1_BYT2[7:0] | 0x00 | | | Biquad 2, D1 coefficient byte[23:16] |
| 0x2A | BQ2_D1_BYT3[7:0] | 0x00 | | | Biquad 2, D1 coefficient byte[15:8] |
| 0x2B | BQ2_D1_BYT4[7:0] | 0x00 | | | Biquad 2, D1 coefficient byte[7:0] |
| 0x2C | BQ2_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 2, D2 coefficient byte[31:24] |
| 0x2D | BQ2_D2_BYT2[7:0] | 0x00 | | | Biquad 2, D2 coefficient byte[23:16] |
| 0x2E | BQ2_D2_BYT3[7:0] | 0x00 | | | Biquad 2, D2 coefficient byte[15:8] |
| 0x2F | BQ2_D2_BYT4[7:0] | 0x00 | | | Biquad 2, D2 coefficient byte[7:0] |

**Table 3-7. Page 0x02 Programmable Coefficient Registers for Biquad Filters 1–6 (continued)**

| Page 0x2 Address | Register | Reset Value | Biquad Filter | Coefficient | Description |
|---|---|---|---|---|---|
| 0x30 | BQ3_N0_BYT1[7:0] | 0x7F | Programmable Biquad 3 | N0 | Biquad 3, N0 coefficient byte[31:24] |
| 0x31 | BQ3_N0_BYT2[7:0] | 0xFF | | | Biquad 3, N0 coefficient byte[23:16] |
| 0x32 | BQ3_N0_BYT3[7:0] | 0xFF | | | Biquad 3, N0 coefficient byte[15:8] |
| 0x33 | BQ3_N0_BYT4[7:0] | 0xFF | | | Biquad 3, N0 coefficient byte[7:0] |
| 0x34 | BQ3_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 3, N1 coefficient byte[31:24] |
| 0x35 | BQ3_N1_BYT2[7:0] | 0x00 | | | Biquad 3, N1 coefficient byte[23:16] |
| 0x36 | BQ3_N1_BYT3[7:0] | 0x00 | | | Biquad 3, N1 coefficient byte[15:8] |
| 0x37 | BQ3_N1_BYT4[7:0] | 0x00 | | | Biquad 3, N1 coefficient byte[7:0] |
| 0x38 | BQ3_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 3, N2 coefficient byte[31:24] |
| 0x39 | BQ3_N2_BYT2[7:0] | 0x00 | | | Biquad 3, N2 coefficient byte[23:16] |
| 0x3A | BQ3_N2_BYT3[7:0] | 0x00 | | | Biquad 3, N2 coefficient byte[15:8] |
| 0x3B | BQ3_N2_BYT4[7:0] | 0x00 | | | Biquad 3, N2 coefficient byte[7:0] |
| 0x3C | BQ3_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 3, D1 coefficient byte[31:24] |
| 0x3D | BQ3_D1_BYT2[7:0] | 0x00 | | | Biquad 3, D1 coefficient byte[23:16] |
| 0x3E | BQ3_D1_BYT3[7:0] | 0x00 | | | Biquad 3, D1 coefficient byte[15:8] |
| 0x3F | BQ3_D1_BYT4[7:0] | 0x00 | | | Biquad 3, D1 coefficient byte[7:0] |
| 0x40 | BQ3_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 3, D2 coefficient byte[31:24] |
| 0x41 | BQ3_D2_BYT2[7:0] | 0x00 | | | Biquad 3, D2 coefficient byte[23:16] |
| 0x42 | BQ3_D2_BYT3[7:0] | 0x00 | | | Biquad 3, D2 coefficient byte[15:8] |
| 0x43 | BQ3_D2_BYT4[7:0] | 0x00 | | | Biquad 3, D2 coefficient byte[7:0] |
| 0x44 | BQ4_N0_BYT1[7:0] | 0x7F | Programmable Biquad 4 | N0 | Biquad 4, N0 coefficient byte[31:24] |
| 0x45 | BQ4_N0_BYT2[7:0] | 0xFF | | | Biquad 4, N0 coefficient byte[23:16] |
| 0x46 | BQ4_N0_BYT3[7:0] | 0xFF | | | Biquad 4, N0 coefficient byte[15:8] |
| 0x47 | BQ4_N0_BYT4[7:0] | 0xFF | | | Biquad 4, N0 coefficient byte[7:0] |
| 0x48 | BQ4_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 4, N1 coefficient byte[31:24] |
| 0x49 | BQ4_N1_BYT2[7:0] | 0x00 | | | Biquad 4, N1 coefficient byte[23:16] |
| 0x4A | BQ4_N1_BYT3[7:0] | 0x00 | | | Biquad 4, N1 coefficient byte[15:8] |
| 0x4B | BQ4_N1_BYT4[7:0] | 0x00 | | | Biquad 4, N1 coefficient byte[7:0] |
| 0x4C | BQ4_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 4, N2 coefficient byte[31:24] |
| 0x4D | BQ4_N2_BYT2[7:0] | 0x00 | | | Biquad 4, N2 coefficient byte[23:16] |
| 0x4E | BQ4_N2_BYT3[7:0] | 0x00 | | | Biquad 4, N2 coefficient byte[15:8] |
| 0x4F | BQ4_N2_BYT4[7:0] | 0x00 | | | Biquad 4, N2 coefficient byte[7:0] |
| 0x50 | BQ4_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 4, D1 coefficient byte[31:24] |
| 0x51 | BQ4_D1_BYT2[7:0] | 0x00 | | | Biquad 4, D1 coefficient byte[23:16] |
| 0x52 | BQ4_D1_BYT3[7:0] | 0x00 | | | Biquad 4, D1 coefficient byte[15:8] |
| 0x53 | BQ4_D1_BYT4[7:0] | 0x00 | | | Biquad 4, D1 coefficient byte[7:0] |
| 0x54 | BQ4_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 4, D2 coefficient byte[31:24] |
| 0x55 | BQ4_D2_BYT2[7:0] | 0x00 | | | Biquad 4, D2 coefficient byte[23:16] |
| 0x56 | BQ4_D2_BYT3[7:0] | 0x00 | | | Biquad 4, D2 coefficient byte[15:8] |
| 0x57 | BQ4_D2_BYT4[7:0] | 0x00 | | | Biquad 4, D2 coefficient byte[7:0] |

**Table 3-7. Page 0x02 Programmable Coefficient Registers for Biquad Filters 1–6 (continued)**

| Page 0x2 Address | Register | Reset Value | Biquad Filter | Coefficient | Description |
|---|---|---|---|---|---|
| 0x58 | BQ5_N0_BYT1[7:0] | 0x7F | Programmable Biquad 5 | N0 | Biquad 5, N0 coefficient byte[31:24] |
| 0x59 | BQ5_N0_BYT2[7:0] | 0xFF | | | Biquad 5, N0 coefficient byte[23:16] |
| 0x5A | BQ5_N0_BYT3[7:0] | 0xFF | | | Biquad 5, N0 coefficient byte[15:8] |
| 0x5B | BQ5_N0_BYT4[7:0] | 0xFF | | | Biquad 5, N0 coefficient byte[7:0] |
| 0x5C | BQ5_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 5, N1 coefficient byte[31:24] |
| 0x5D | BQ5_N1_BYT2[7:0] | 0x00 | | | Biquad 5, N1 coefficient byte[23:16] |
| 0x5E | BQ5_N1_BYT3[7:0] | 0x00 | | | Biquad 5, N1 coefficient byte[15:8] |
| 0x5F | BQ5_N1_BYT4[7:0] | 0x00 | | | Biquad 5, N1 coefficient byte[7:0] |
| 0x60 | BQ5_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 5, N2 coefficient byte[31:24] |
| 0x61 | BQ5_N2_BYT2[7:0] | 0x00 | | | Biquad 5, N2 coefficient byte[23:16] |
| 0x62 | BQ5_N2_BYT3[7:0] | 0x00 | | | Biquad 5, N2 coefficient byte[15:8] |
| 0x63 | BQ5_N2_BYT4[7:0] | 0x00 | | | Biquad 5, N2 coefficient byte[7:0] |
| 0x64 | BQ5_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 5, D1 coefficient byte[31:24] |
| 0x65 | BQ5_D1_BYT2[7:0] | 0x00 | | | Biquad 5, D1 coefficient byte[23:16] |
| 0x66 | BQ5_D1_BYT3[7:0] | 0x00 | | | Biquad 5, D1 coefficient byte[15:8] |
| 0x67 | BQ5_D1_BYT4[7:0] | 0x00 | | | Biquad 5, D1 coefficient byte[7:0] |
| 0x68 | BQ5_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 5, D2 coefficient byte[31:24] |
| 0x69 | BQ5_D2_BYT2[7:0] | 0x00 | | | Biquad 5, D2 coefficient byte[23:16] |
| 0x6A | BQ5_D2_BYT3[7:0] | 0x00 | | | Biquad 5, D2 coefficient byte[15:8] |
| 0x6B | BQ5_D2_BYT4[7:0] | 0x00 | | | Biquad 5, D2 coefficient byte[7:0] |
| 0x6C | BQ6_N0_BYT1[7:0] | 0x7F | Programmable Biquad 6 | N0 | Biquad 6, N0 coefficient byte[31:24] |
| 0x6D | BQ6_N0_BYT2[7:0] | 0xFF | | | Biquad 6, N0 coefficient byte[23:16] |
| 0x6E | BQ6_N0_BYT3[7:0] | 0xFF | | | Biquad 6, N0 coefficient byte[15:8] |
| 0x6F | BQ6_N0_BYT4[7:0] | 0xFF | | | Biquad 6, N0 coefficient byte[7:0] |
| 0x70 | BQ6_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 6, N1 coefficient byte[31:24] |
| 0x71 | BQ6_N1_BYT2[7:0] | 0x00 | | | Biquad 6, N1 coefficient byte[23:16] |
| 0x72 | BQ6_N1_BYT3[7:0] | 0x00 | | | Biquad 6, N1 coefficient byte[15:8] |
| 0x73 | BQ6_N1_BYT4[7:0] | 0x00 | | | Biquad 6, N1 coefficient byte[7:0] |
| 0x74 | BQ6_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 6, N2 coefficient byte[31:24] |
| 0x75 | BQ6_N2_BYT2[7:0] | 0x00 | | | Biquad 6, N2 coefficient byte[23:16] |
| 0x76 | BQ6_N2_BYT3[7:0] | 0x00 | | | Biquad 6, N2 coefficient byte[15:8] |
| 0x77 | BQ6_N2_BYT4[7:0] | 0x00 | | | Biquad 6, N2 coefficient byte[7:0] |
| 0x78 | BQ6_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 6, D1 coefficient byte[31:24] |
| 0x79 | BQ6_D1_BYT2[7:0] | 0x00 | | | Biquad 6, D1 coefficient byte[23:16] |
| 0x7A | BQ6_D1_BYT3[7:0] | 0x00 | | | Biquad 6, D1 coefficient byte[15:8] |
| 0x7B | BQ6_D1_BYT4[7:0] | 0x00 | | | Biquad 6, D1 coefficient byte[7:0] |
| 0x7C | BQ6_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 6, D2 coefficient byte[31:24] |
| 0x7D | BQ6_D2_BYT2[7:0] | 0x00 | | | Biquad 6, D2 coefficient byte[23:16] |
| 0x7E | BQ6_D2_BYT3[7:0] | 0x00 | | | Biquad 6, D2 coefficient byte[15:8] |
| 0x7F | BQ6_D2_BYT4[7:0] | 0x00 | | | Biquad 6, D2 coefficient byte[7:0] |

## 3.6 Programmable Coefficient Registers for Digital Biquad Filters 7–12

Table 3-8 shows the programmable coefficient registers for the biquad filters 7 through 12 in Page 3 of the TLV320ADCx140/PCMx140-Q1 registers.

**Table 3-8. Page 0x03 Programmable Coefficient Registers for Biquad Filters 7–12**

| Page 0x3 Address | Register | Reset | Biquad Filter | Coefficient | Description |
|---|---|---|---|---|---|
| 0x00 | PAGE[7:0] | 0x00 | | | Device Page Register |
| 0x08 | BQ7_N0_BYT1[7:0] | 0x7F | Programmable Biquad 7 | N0 | Programmable biquad 7, N0 coefficient byte[31:24] |
| 0x09 | BQ7_N0_BYT2[7:0] | 0xFF | | | Biquad 7, N0 coefficient byte[23:16] |
| 0x0A | BQ7_N0_BYT3[7:0] | 0xFF | | | Biquad 7, N0 coefficient byte[15:8] |
| 0x0B | BQ7_N0_BYT4[7:0] | 0xFF | | | Biquad 7, N0 coefficient byte[7:0] |
| 0x0C | BQ7_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 7, N1 coefficient byte[31:24] |
| 0x0D | BQ7_N1_BYT2[7:0] | 0x00 | | | Biquad 7, N1 coefficient byte[23:16] |
| 0x0E | BQ7_N1_BYT3[7:0] | 0x00 | | | Biquad 7, N1 coefficient byte[15:8] |
| 0x0F | BQ7_N1_BYT4[7:0] | 0x00 | | | Biquad 7, N1 coefficient byte[7:0] |
| 0x10 | BQ7_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 7, N2 coefficient byte[31:24] |
| 0x11 | BQ7_N2_BYT2[7:0] | 0x00 | | | Biquad 7, N2 coefficient byte[23:16] |
| 0x12 | BQ7_N2_BYT3[7:0] | 0x00 | | | Biquad 7, N2 coefficient byte[15:8] |
| 0x13 | BQ7_N2_BYT4[7:0] | 0x00 | | | Biquad 7, N2 coefficient byte[7:0] |
| 0x14 | BQ7_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 7, D1 coefficient byte[31:24] |
| 0x15 | BQ7_D1_BYT2[7:0] | 0x00 | | | Biquad 7, D1 coefficient byte[23:16] |
| 0x16 | BQ7_D1_BYT3[7:0] | 0x00 | | | Biquad 7, D1 coefficient byte[15:8] |
| 0x17 | BQ7_D1_BYT4[7:0] | 0x00 | | | Biquad 7, D1 coefficient byte[7:0] |
| 0x18 | BQ7_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 7, D2 coefficient byte[31:24] |
| 0x19 | BQ7_D2_BYT2[7:0] | 0x00 | | | Biquad 7, D2 coefficient byte[23:16] |
| 0x1A | BQ7_D2_BYT3[7:0] | 0x00 | | | Biquad 7, D2 coefficient byte[15:8] |
| 0x1B | BQ7_D2_BYT4[7:0] | 0x00 | | | Biquad 7, D2 coefficient byte[7:0] |
| 0x1C | BQ8_N0_BYT1[7:0] | 0x7F | Programmable Biquad 8 | N0 | Biquad 8, N0 coefficient byte[31:24] |
| 0x1D | BQ8_N0_BYT2[7:0] | 0xFF | | | Biquad 8, N0 coefficient byte[23:16] |
| 0x1E | BQ8_N0_BYT3[7:0] | 0xFF | | | Biquad 8, N0 coefficient byte[15:8] |
| 0x1F | BQ8_N0_BYT4[7:0] | 0xFF | | | Biquad 8, N0 coefficient byte[7:0] |
| 0x20 | BQ8_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 8, N1 coefficient byte[31:24] |
| 0x21 | BQ8_N1_BYT2[7:0] | 0x00 | | | Biquad 8, N1 coefficient byte[23:16] |
| 0x22 | BQ8_N1_BYT3[7:0] | 0x00 | | | Biquad 8, N1 coefficient byte[15:8] |
| 0x23 | BQ8_N1_BYT4[7:0] | 0x00 | | | Biquad 8, N1 coefficient byte[7:0] |
| 0x24 | BQ8_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 8, N2 coefficient byte[31:24] |
| 0x25 | BQ8_N2_BYT2[7:0] | 0x00 | | | Biquad 8, N2 coefficient byte[23:16] |
| 0x26 | BQ8_N2_BYT3[7:0] | 0x00 | | | Biquad 8, N2 coefficient byte[15:8] |
| 0x27 | BQ8_N2_BYT4[7:0] | 0x00 | | | Biquad 8, N2 coefficient byte[7:0] |
| 0x28 | BQ8_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 8, D1 coefficient byte[31:24] |
| 0x29 | BQ8_D1_BYT2[7:0] | 0x00 | | | Biquad 8, D1 coefficient byte[23:16] |
| 0x2A | BQ8_D1_BYT3[7:0] | 0x00 | | | Biquad 8, D1 coefficient byte[15:8] |
| 0x2B | BQ8_D1_BYT4[7:0] | 0x00 | | | Biquad 8, D1 coefficient byte[7:0] |
| 0x2C | BQ8_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 8, D2 coefficient byte[31:24] |
| 0x2D | BQ8_D2_BYT2[7:0] | 0x00 | | | Biquad 8, D2 coefficient byte[23:16] |
| 0x2E | BQ8_D2_BYT3[7:0] | 0x00 | | | Biquad 8, D2 coefficient byte[15:8] |
| 0x2F | BQ8_D2_BYT4[7:0] | 0x00 | | | Biquad 8, D2 coefficient byte[7:0] |

**Table 3-8. Page 0x03 Programmable Coefficient Registers for Biquad Filters 7–12 (continued)**

| Page 0x3 Address | Register | Reset | Biquad Filter | Coefficient | Description |
|---|---|---|---|---|---|
| 0x30 | BQ9_N0_BYT1[7:0] | 0x7F | Programmable Biquad 9 | N0 | Biquad 9, N0 coefficient byte[31:24] |
| 0x31 | BQ9_N0_BYT2[7:0] | 0xFF | | | Biquad 9, N0 coefficient byte[23:16] |
| 0x32 | BQ9_N0_BYT3[7:0] | 0xFF | | | Biquad 9, N0 coefficient byte[15:8] |
| 0x33 | BQ9_N0_BYT4[7:0] | 0xFF | | | Biquad 9, N0 coefficient byte[7:0] |
| 0x34 | BQ9_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 9, N1 coefficient byte[31:24] |
| 0x35 | BQ9_N1_BYT2[7:0] | 0x00 | | | Biquad 9, N1 coefficient byte[23:16] |
| 0x36 | BQ9_N1_BYT3[7:0] | 0x00 | | | Biquad 9, N1 coefficient byte[15:8] |
| 0x37 | BQ9_N1_BYT4[7:0] | 0x00 | | | Biquad 9, N1 coefficient byte[7:0] |
| 0x38 | BQ9_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 9, N2 coefficient byte[31:24] |
| 0x39 | BQ9_N2_BYT2[7:0] | 0x00 | | | Biquad 9, N2 coefficient byte[23:16] |
| 0x3A | BQ9_N2_BYT3[7:0] | 0x00 | | | Biquad 9, N2 coefficient byte[15:8] |
| 0x3B | BQ9_N2_BYT4[7:0] | 0x00 | | | Biquad 9, N2 coefficient byte[7:0] |
| 0x3C | BQ9_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 9, D1 coefficient byte[31:24] |
| 0x3D | BQ9_D1_BYT2[7:0] | 0x00 | | | Biquad 9, D1 coefficient byte[23:16] |
| 0x3E | BQ9_D1_BYT3[7:0] | 0x00 | | | Biquad 9, D1 coefficient byte[15:8] |
| 0x3F | BQ9_D1_BYT4[7:0] | 0x00 | | | Biquad 9, D1 coefficient byte[7:0] |
| 0x40 | BQ9_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 9, D2 coefficient byte[31:24] |
| 0x41 | BQ9_D2_BYT2[7:0] | 0x00 | | | Biquad 9, D2 coefficient byte[23:16] |
| 0x42 | BQ9_D2_BYT3[7:0] | 0x00 | | | Biquad 9, D2 coefficient byte[15:8] |
| 0x43 | BQ9_D2_BYT4[7:0] | 0x00 | | | Biquad 9, D2 coefficient byte[7:0] |
| 0x44 | BQ10_N0_BYT1[7:0] | 0x7F | Programmable Biquad 10 | N0 | Biquad 10, N0 coefficient byte[31:24] |
| 0x45 | BQ10_N0_BYT2[7:0] | 0xFF | | | Biquad 10, N0 coefficient byte[23:16] |
| 0x46 | BQ10_N0_BYT3[7:0] | 0xFF | | | Biquad 10, N0 coefficient byte[15:8] |
| 0x47 | BQ10_N0_BYT4[7:0] | 0xFF | | | Biquad 10, N0 coefficient byte[7:0] |
| 0x48 | BQ10_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 10, N1 coefficient byte[31:24] |
| 0x49 | BQ10_N1_BYT2[7:0] | 0x00 | | | Biquad 10, N1 coefficient byte[23:16] |
| 0x4A | BQ10_N1_BYT3[7:0] | 0x00 | | | Biquad 10, N1 coefficient byte[15:8] |
| 0x4B | BQ10_N1_BYT4[7:0] | 0x00 | | | Biquad 10, N1 coefficient byte[7:0] |
| 0x4C | BQ10_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 10, N2 coefficient byte[31:24] |
| 0x4D | BQ10_N2_BYT2[7:0] | 0x00 | | | Biquad 10, N2 coefficient byte[23:16] |
| 0x4E | BQ10_N2_BYT3[7:0] | 0x00 | | | Biquad 10, N2 coefficient byte[15:8] |
| 0x4F | BQ10_N2_BYT4[7:0] | 0x00 | | | Biquad 10, N2 coefficient byte[7:0] |
| 0x50 | BQ10_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 10, D1 coefficient byte[31:24] |
| 0x51 | BQ10_D1_BYT2[7:0] | 0x00 | | | Biquad 10, D1 coefficient byte[23:16] |
| 0x52 | BQ10_D1_BYT3[7:0] | 0x00 | | | Biquad 10, D1 coefficient byte[15:8] |
| 0x53 | BQ10_D1_BYT4[7:0] | 0x00 | | | Biquad 10, D1 coefficient byte[7:0] |
| 0x54 | BQ10_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 10, D2 coefficient byte[31:24] |
| 0x55 | BQ10_D2_BYT2[7:0] | 0x00 | | | Biquad 10, D2 coefficient byte[23:16] |
| 0x56 | BQ10_D2_BYT3[7:0] | 0x00 | | | Biquad 10, D2 coefficient byte[15:8] |
| 0x57 | BQ10_D2_BYT4[7:0] | 0x00 | | | Biquad 10, D2 coefficient byte[7:0] |

**Table 3-8. Page 0x03 Programmable Coefficient Registers for Biquad Filters 7–12 (continued)**

| Page 0x3 Address | Register | Reset | Biquad Filter | Coefficient | Description |
|---|---|---|---|---|---|
| 0x58 | BQ11_N0_BYT1[7:0] | 0x7F | Programmable Biquad 11 | N0 | Biquad 11, N0 coefficient byte[31:24] |
| 0x59 | BQ11_N0_BYT2[7:0] | 0xFF | | | Biquad 11, N0 coefficient byte[23:16] |
| 0x5A | BQ11_N0_BYT3[7:0] | 0xFF | | | Biquad 11, N0 coefficient byte[15:8] |
| 0x5B | BQ11_N0_BYT4[7:0] | 0xFF | | | Biquad 11, N0 coefficient byte[7:0] |
| 0x5C | BQ11_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 11, N1 coefficient byte[31:24] |
| 0x5D | BQ11_N1_BYT2[7:0] | 0x00 | | | Biquad 11, N1 coefficient byte[23:16] |
| 0x5E | BQ11_N1_BYT3[7:0] | 0x00 | | | Biquad 11, N1 coefficient byte[15:8] |
| 0x5F | BQ11_N1_BYT4[7:0] | 0x00 | | | Biquad 11, N1 coefficient byte[7:0] |
| 0x60 | BQ11_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 11, N2 coefficient byte[31:24] |
| 0x61 | BQ11_N2_BYT2[7:0] | 0x00 | | | Biquad 11, N2 coefficient byte[23:16] |
| 0x62 | BQ11_N2_BYT3[7:0] | 0x00 | | | Biquad 11, N2 coefficient byte[15:8] |
| 0x63 | BQ11_N2_BYT4[7:0] | 0x00 | | | Biquad 11, N2 coefficient byte[7:0] |
| 0x64 | BQ11_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 11, D1 coefficient byte[31:24] |
| 0x65 | BQ11_D1_BYT2[7:0] | 0x00 | | | Biquad 11, D1 coefficient byte[23:16] |
| 0x66 | BQ11_D1_BYT3[7:0] | 0x00 | | | Biquad 11, D1 coefficient byte[15:8] |
| 0x67 | BQ11_D1_BYT4[7:0] | 0x00 | | | Biquad 11, D1 coefficient byte[7:0] |
| 0x68 | BQ11_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 11, D2 coefficient byte[31:24] |
| 0x69 | BQ11_D2_BYT2[7:0] | 0x00 | | | Biquad 11, D2 coefficient byte[23:16] |
| 0x6A | BQ11_D2_BYT3[7:0] | 0x00 | | | Biquad 11, D2 coefficient byte[15:8] |
| 0x6B | BQ11_D2_BYT4[7:0] | 0x00 | | | Biquad 11, D2 coefficient byte[7:0] |
| 0x6C | BQ12_N0_BYT1[7:0] | 0x7F | Programmable Biquad 12 | N0 | Biquad 12, N0 coefficient byte[31:24] |
| 0x6D | BQ12_N0_BYT2[7:0] | 0xFF | | | Biquad 12, N0 coefficient byte[23:16] |
| 0x6E | BQ12_N0_BYT3[7:0] | 0xFF | | | Biquad 12, N0 coefficient byte[15:8] |
| 0x6F | BQ12_N0_BYT4[7:0] | 0xFF | | | Biquad 12, N0 coefficient byte[7:0] |
| 0x70 | BQ12_N1_BYT1[7:0] | 0x00 | | N1 | Biquad 12, N1 coefficient byte[31:24] |
| 0x71 | BQ12_N1_BYT2[7:0] | 0x00 | | | Biquad 12, N1 coefficient byte[23:16] |
| 0x72 | BQ12_N1_BYT3[7:0] | 0x00 | | | Biquad 12, N1 coefficient byte[15:8] |
| 0x73 | BQ12_N1_BYT4[7:0] | 0x00 | | | Biquad 12, N1 coefficient byte[7:0] |
| 0x74 | BQ12_N2_BYT1[7:0] | 0x00 | | N2 | Biquad 12, N2 coefficient byte[31:24] |
| 0x75 | BQ12_N2_BYT2[7:0] | 0x00 | | | Biquad 12, N2 coefficient byte[23:16] |
| 0x76 | BQ12_N2_BYT3[7:0] | 0x00 | | | Biquad 12, N2 coefficient byte[15:8] |
| 0x77 | BQ12_N2_BYT4[7:0] | 0x00 | | | Biquad 12, N2 coefficient byte[7:0] |
| 0x78 | BQ12_D1_BYT1[7:0] | 0x00 | | D1 | Biquad 12, D1 coefficient byte[31:24] |
| 0x79 | BQ12_D1_BYT2[7:0] | 0x00 | | | Biquad 12, D1 coefficient byte[23:16] |
| 0x7A | BQ12_D1_BYT3[7:0] | 0x00 | | | Biquad 12, D1 coefficient byte[15:8] |
| 0x7B | BQ12_D1_BYT4[7:0] | 0x00 | | | Biquad 12, D1 coefficient byte[7:0] |
| 0x7C | BQ12_D2_BYT1[7:0] | 0x00 | | D2 | Biquad 12, D2 coefficient byte[31:24] |
| 0x7D | BQ12_D2_BYT2[7:0] | 0x00 | | | Biquad 12, D2 coefficient byte[23:16] |
| 0x7E | BQ12_D2_BYT3[7:0] | 0x00 | | | Biquad 12, D2 coefficient byte[15:8] |
| 0x7F | BQ12_D2_BYT4[7:0] | 0x00 | | | Biquad 12, D2 coefficient byte[7:0] |

# 4 How to Program the Digital Biquad Filters on TLV320ADCx140/PCMx140-Q1

Coefficients of Digital Biquad Filters can be implemented by running a command script to send an I2C command to the EVM. The following script segment shows how to program the coefficients for a set of filters for 5-dB boost at 500 Hz with bandwidth of 400 Hz, cut –5 dB at 2 kHz with 3-kHz bandwidth, and a Notch filter at 60 Hz with 50-Hz bandwidth for channel 1.

```
# Select Page 2
w 98 00 02
# Write Coefficient N0, N1, N2, D1, D2 for Biquad Filter 1
w 98 08 7f ff ff ff 85 dc e2 7d 74 cc 68 8f 7c 77 a7 18 86 87 f4 ee
# Write Coefficient N0, N1, N2, D1, D2 for Biquad Filter 5
w 98 58 71 80 7d b6 a4 5b f4 41 4c 3e c3 29 5b a4 0b bf c2 40 bf 20
# Select Page 3
w 98 00 03
# Write Coefficient N0, N1, N2, D1, D2 for Biquad Filter 9
w 98 30 7f 95 1d c9 80 6b e4 18 7f 95 1d c9 7f 94 1b e8 80 d5 c4 6d
```

# 5 Typical Audio Applications for Biquad Filtering

In audio systems, biquad filters offer flexible frequency response filters for the following applications:

- Parametric Equalizers
- Crossover Networks
- Voice boost
- Bass boost
- Removing 50 Hz–60 Hz hum with notch filers

## 5.1 Parametric Equalizers

Cascading several parametric equalizers provide frequency shaping control of the input signal with three control settings: gain, center frequency, and bandwidth or Q-factor. Parametric equalizers control the tone and sound to flatten or match different input sources during mixing or provide particular effect to the input signal. Equalization usually compensates for the physical response of microphones or speakers, balances the tone of several instruments, or changes the timbre of an instrument since these filers provide very selective frequency adjustment during mixing or a specific range effect during recording. For example, small earbud headphones might not be able to reproduce low.

# 6 Crossover Networks

Crossover networks separate or join together several specific frequency bands. They are typically used in speaker systems to separate the low-, mid-, and high-range frequencies to respective drive woofers, midrange, or tweeter drivers. These filters protect the drivers from wasteful, noise inducing, or harmful frequencies that the driver is not designed to handle. For example, there is no need to send high frequency to a woofer. The woofer is not able to reproduce high frequencies and just adds distortion. A tweeter can be damaged by strong low frequencies, thus it is best to filter these before sending the signal to these drivers. Linkwitz Riley implementations are tailored to produce an overall gain of 0 dB at the crossover frequency when their low-pass and high-pass filters combine together so the overall musical tone is not changed during reproduction.

# 7 Voice Boost

Human speech has a usable frequency range of 200 Hz–8 kHz. Male speech bandwidth is roughly 200 Hz–6 kHz while female speech bandwidth is roughly 400 Hz–8 kHz. To improve speech intelligibility, a bandpass filters or parametric equalizer boosts the voiceband frequencies while suppressing other frequencies to lower background noise or other musical instruments.

# 8 Bass Boost

Simple Bass shelf filters provide a bass boost. These are typically used to compensate for speakers that have difficulty reproducing low frequencies. For example, small speakers might require a bass boost to improve low-frequency reproduction.

# 9 Removing 50 Hz–60 Hz Hum With Notch Filters

Notch filters cut a specific single frequency. These filters are highly efficient for removing 50 Hz or 60 Hz power line hum, transformer hum, room resonance, acoustic feedback, and any undesired specific frequency component introduced by the room acoustics or recording equipment.

## 10 Revision History

| Changes from Revision A (November 2014) to Revision B (December 2023) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |

| Changes from Revision * (April 2019) to Revision A (November 2019) | Page |
|---|---|
| • Added PCMx140-Q1PCM6xx0 throughout the document | 1 |
| • Added missing information to the Abstract | 1 |
| • Added missing Linkwitz Riley equations | 18 |
| • Corrected low pass butterworth equations | 18 |

# 11 Digital Filter Design Techniques

## 11.1 Analog Filters

PurePath Console Digital Filter design uses analog filter design techniques and transposes them to the digital domain. The analog filters are represented in the S-domain. Through the bilinear transformation, these analog filters are converted from the S-domain to the digital Z-domain. In these filters, each pole of the filter provides a –6 dB per octave or –10 dB per decade slope in the frequency response. Each zero of the filter provides a +6 dB per octave or +10 dB per decade slope in the frequency response. Table 11-1 shows the S-domain transfer function of the PurePath Console filter design. Note that Q = $f_c$ / Bandwidth, where $f_c$ is the center frequency.

**Table 11-1. PurePath™ Console Filter Transfer Function**

| FILTER TYPE | TRANSFER FUNCTION | WHEN TO USE |
|---|---|---|
| Band Pass | $H(s) = \frac{\frac{w_c}{Q}s}{s^2 + \frac{w_c}{Q}s + w_c^2}$ | Filters a set of frequencies given by bandwidth and center frequency |
| Bass Shelf | $H(s) = \frac{w_c^2}{s^2 + w_c s + w_c^2}$ | Applies the specified gain at low frequency up to the specified cutoff frequency |
| Equalizer (Bandwidth) | $H(s) = \frac{\frac{w_c}{Q}s}{s^2 + \frac{w_c}{Q}s + w_c^2}$ | Band-pass filter at the specified center frequency and passband width, with the specified gain |
| Equalizer (Q Factor) | | Band-pass filter at the specified center frequency and quality factor, with the specified gain. The quality factor is the center frequency divided by the passband width. |
| Gain | $H(s) = \frac{s^2 - \frac{w_c}{Q}s + w_c^2}{s^2 + \frac{w_c}{Q}s + w_c^2}$ | All pass filter at the specified gain |
| High-Pass Butterworth 1 | $H(s) = \frac{s^2}{s^2 + \sqrt{2}w_c s + w_c^2}$ | Flat passband and stopband response with a –10 dB / decade slope past the cutoff frequency |
| High-Pass Butterworth 2 | | Flat passband and stopband response with a –20 dB / decade past the cutoff frequency |
| High-Pass Bessel 2 | $H(s) = \frac{s^2}{s^2 + \sqrt{3}w_c s + w_c^2}$ | Maximally flat magnitude and phase in passband with constant group delay at the expense of the greatest transition band |
| High-Pass Linkwitz Riley 2 | $H(s) = \frac{(w_c s)^2}{(1 + w_c s)^2}$ | Use in crossover systems with the same cutoff frequency for low pass and high pass. These filters overall gain is 0 dB at the crossover point. |
| High-Pass Variable Q 2 | $H(s) = \frac{s^2}{s^2 + \frac{w_c}{Q}s + w_c^2}$ | Second-order high-pass filter at the specified center frequency, gain and quality factor. The quality factor is the center frequency divided by the passband width. |
| High-Pass Chebyshev | $H(s) = \frac{s^2}{\sqrt{2}s^2 + 0.911w_c s + w_c^2}$ | Sharper transition band than Butterworth at the expense of ripple in the passband. |
| Low-Pass Butterworth 1 | $H(s) = \frac{w_c^2}{s^2 + \sqrt{2}w_c s + w_c^2}$ | Flat passband and stopband response with a –10 dB / decade slope up to the cutoff frequency |
| Low-Pass Butterworth 2 | | Flat passband and stopband response with a –20 dB / decade up to the cutoff frequency |
| Low-Pass Bessel 2 | $H(s) = \frac{w_c^2}{s^2 + \sqrt{3}w_c s + w_c^2}$ | Maximally flat magnitude and phase in passband with constant group delay at the expense of the greatest transition band |
| Low-Pass Linkwitz Riley 2 | $H(s) = \frac{1}{(1 + w_c s)^2}$ | Use in crossover systems with the same cutoff frequency for low pass and high pass. These filters overall gain is 0 dB at the crossover point. |

**Table 11-1. PurePath™ Console Filter Transfer Function (continued)**

| FILTER TYPE | TRANSFER FUNCTION | WHEN TO USE |
|---|---|---|
| Low-Pass Variable Q 2 | $H(s) = \frac{w_c^2}{s^2 + \frac{w_c}{Q}s + w_c^2}$ | Second-order low-pass filter at the specified center frequency, gain and quality factor. The quality factor is the center frequency divided by the passband width. |
| Low-Pass Chebyshev | $H(s) = \frac{w_c^2}{\sqrt{2}s^2 + 0.911w_cs + w_c^2}$ | Sharper transition band than Butterworth at the expense of ripple in the passband |
| Notch | $H(s) = \frac{s^2 + w_c^2}{s^2 + \frac{w_c}{Q}s + w_c^2}$ | Filter or null a specific frequency |
| Phase Shift | $H(s) = \frac{1 - s/w_c}{1 + s/w_c}$ | Change the phase of a signal |
| Treble Shelf | $H(s) = \frac{s^2}{s^2 + w_cs + w_c^2}$ | Applies the specified gain at the high frequency past the specified cutoff frequency |

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