Single-Event Effects Characterization of TI ADS1282-SP High-Resolution ADC

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ABSTRACT

The single-event effects behavior of the ADS1282-SP, a high dynamic range analog-to-digital converter (ADC), is presented. No latch-up events were detected up to a linear energy transfer (LET) of 50.5 MeV·cm^2/mg at 85°C and 125°C, nor were any latch-up events detected up to an LET of 60.4 MeV·cm^2/mg at 85°C. The device exhibits a single event transient (SET) saturated cross-section of 3.7 × 10^{-4} cm^2. For register upsets, the device exhibited a saturated cross-section of 1.3 × 10^{-5} cm^2.

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1 Overview

High-resolution analog-to-digital converters (ADCs) play a critical role in signal conditioning for sensors with wide dynamic range. Examples of such applications include monitoring thermocouples, accelerometers, and precision instrumentation. However, the lack of space-grade high-dynamic range analog-to-digital converters has often been cited as an impediment to developing important space applications [1].

The ADS1282-SP is a high-resolution delta-sigma ADC for space applications. It offers up to 122-dB SNR with a total harmonic distortion of –102 dB, and integral nonlinearity (INL) of 0.5 ppm [2]. The block diagram shown in Figure 1 includes a front-end programmable gain amplifier (PGA) with a gain range up to 64×, to fully exploit the wide dynamic range available in the ADC. The fast-responding overrange detection circuit provides indication if the differential input voltage exceeds the ADC full scale. Programmable digital filters include user-selectable Sinc filter, FIR, and an IIR filter. The output is available through an SPI interface.

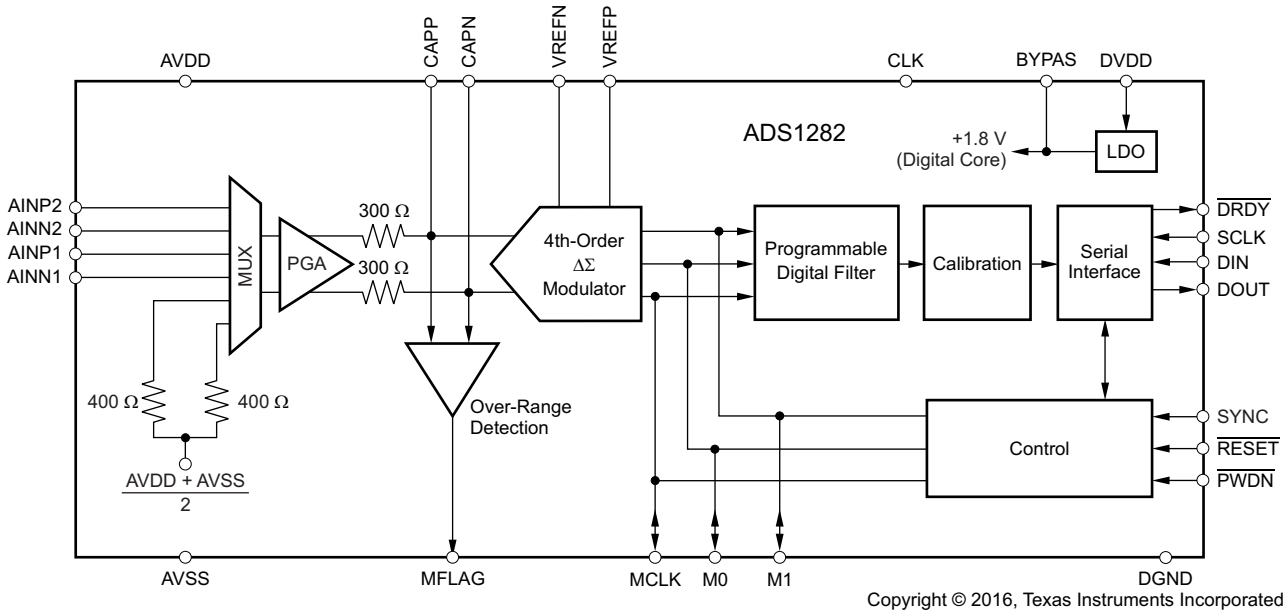

Figure 1. ADS1282-SP Block Diagram

There are two power supplies on the ADS1282-SP: AVDD, and DVDD. The supplies can be powered up in any sequence. The device requires a clock input to be supplied on the CLK pin. A 4-MHz clock is used for the testing described in this paper.

2 SEE Mechanisms

This paper presents an overview of the single event effect (SEE) testing and a summary of the observed results. Testing for single-event latch-up (SEL), single-event functional interrupt (SEFI) and single-event transient (SET) events was performed at the Cyclotron Institute [3] at Texas A&M University using the K500 Cyclotron and the 15 MeV/n beam. The ASTM F1192 [4] and EIA/JESD57 [5] standards were used as reference for this testing. The test plan was outlined by Texas Instruments and the task was contracted to Aeroflex RAD [6].

The SEL testing was performed to determine the threshold for latch-up under worst-case temperature and voltage operating conditions, up to a LET of 80 MeV·cm^2/mg. Maximum fluence of 10^7 ions/cm^2 was used to irradiate at temperatures of 85°C and 125°C. The SEU rates were characterized for a given LET range between 2 MeV·cm^2/mg and 80 MeV·cm^2/mg at a maximum fluence of 10^6 ions/cm^2 or until 100 SET's were recorded. Since the ADS1282-SP has configuration registers, the register SEU rates were characterized in addition to the data conversion SEU rates.

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Table 1. Overview Information(1)

DESCRIPTION	DEVICE INFORMATION
TI Part Number	ADS1282-SP
SMD Number	5962-14231
Device Function	Analog-to-digital conversion
Technology	50HPA07
Exposure Facility	Radiation Effects Facility, Cyclotron, Texas A&M University
Heavy Ion Fluence per run	10^6 ions/cm^2 to 10^7 ions/cm^2
Irradiation Temperature	85°C, and 125°C (for SEL testing)

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Since the ADS1282-SP device does not operate at high voltages or high currents, single-event burn-out (SEB) and single-event gate-rupture (SEGR) events are not expected to be an issue. The primary single-event effect (SEE) events of interest in the ADS1282-SP are SEL, SEFI, and SET.

From a risk and impact point-of-view, the occurrence of an SEL is potentially the most disruptive SEE event and the biggest concern for space applications. In mixed technologies such as BiCMOS HPA07 250-nm process used for the ADS1282-SP, the CMOS circuitry introduces a potential SEL susceptibility. SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-substrate and n-well and n+ and p+ contacts) [7], [8]. The parasitic bipolar structure creates a high-conductance path (creating a steady-state current that is typically orders-of-magnitude higher than the normal operating current) between power and ground that persists (is “latched”) until power is removed or until the device is destroyed by the high-current state. For the design of the ADS1282-SP, SEL-susceptibility was reduced by maximizing the number of well and substrate ties in the CMOS portions of the layout. The design techniques applied for latch-up mitigation were sufficient as the ADS1282-SP exhibited no signs of SEL with heavy-ions of LET_{eff} = 50.5 MeV·cm^2/mg at a fluence of 10^7 ions/cm^2 and a chip temperature of 125°C nor were any latch-up events detected up to an LET_{eff} = 60.4 MeV·cm^2/mg at 85°C.

In devices like the ADS1282-SP delta-sigma ADC single events large enough to effect a circuit is expected to manifest either as an upset in the control logic or the signal chain itself causing either a system reset or misoperation, or, more likely, an error in the ADC output. SEFIs might occur if sequential circuits in the control logic, calibration or serial interface are upset by a single-event. Single-events occurring in the signal chain, preamplifier, modulator, LDO are likely to cause a short-lived error on output samples (a single sample or a small set of contiguous samples) with no other operational changes in the device performance.

3 Test Device and Evaluation Board

The ADS1282-SP is packaged in a 28-pin dual ceramic flat-pack (HKV) package. The pinout of this device is shown in Figure 2. Photographs of the device with and without the lid are shown in Figure 3. The test board used for the SEE testing is shown in Figure 4. The schematics of the device under test (DUT) test-board configurations are shown in Figure 5, Figure 6, and Figure 7.

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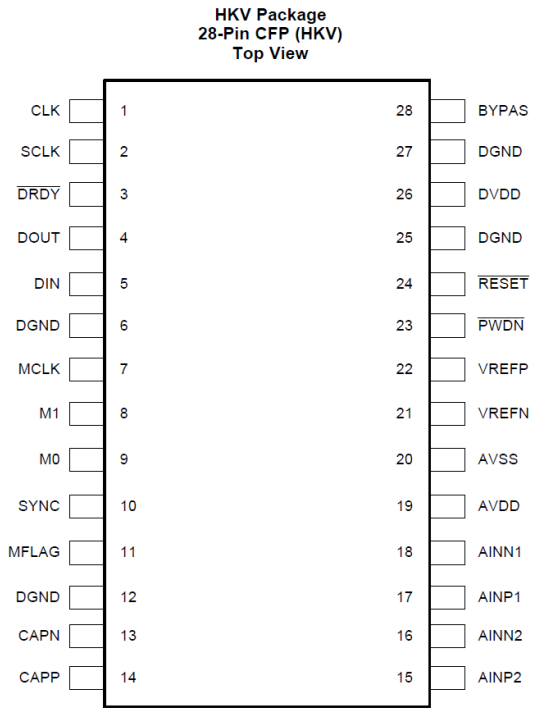

Figure 2. ADS1282-SP Pinout Diagram

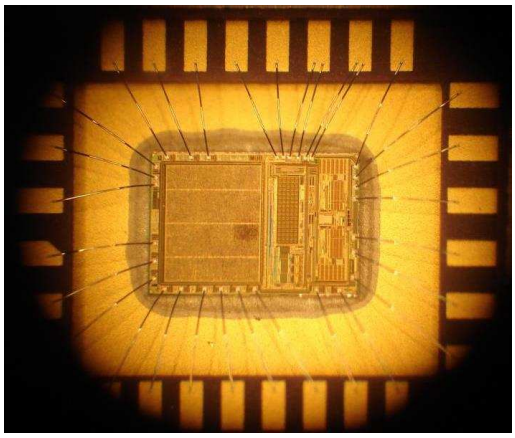

Figure A-1. De-processed ADS1282 DUT

Figure A-2. Received ADS1282 DUTs

Figure 3. Device Under Test (DUT) With and Without Lid

Figure 4. DUT Test Board

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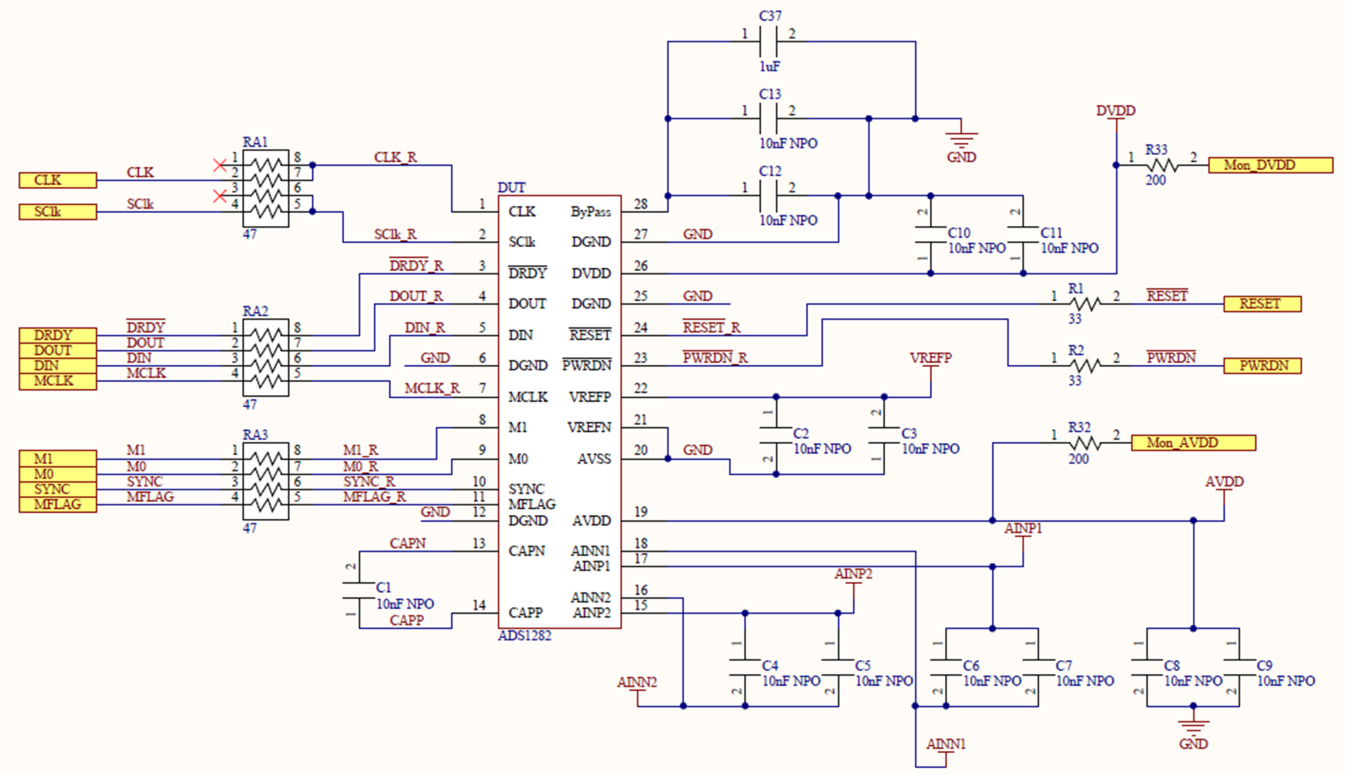

Figure 5. DUT Schematic, DVDD > 2.25 V

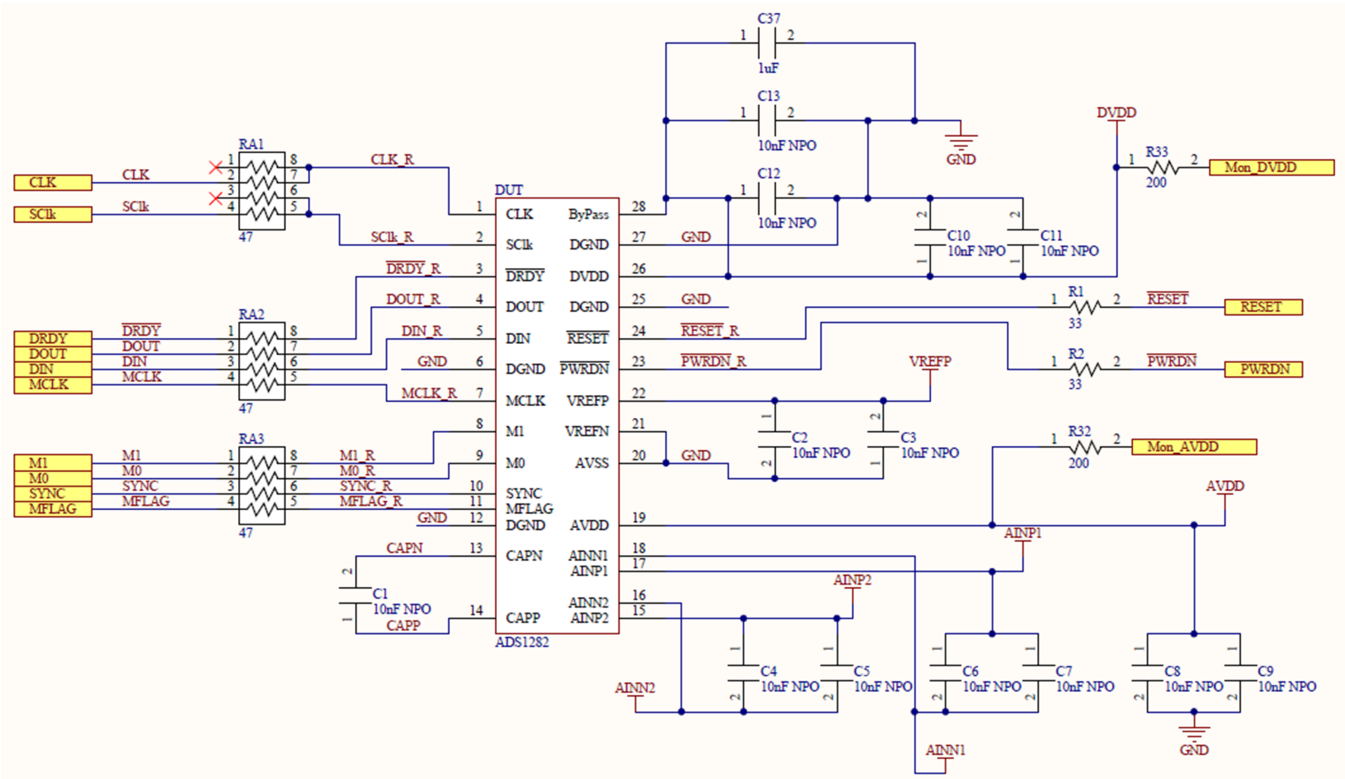

Figure 6. DUT Schematic, DVDD < 2.25 V

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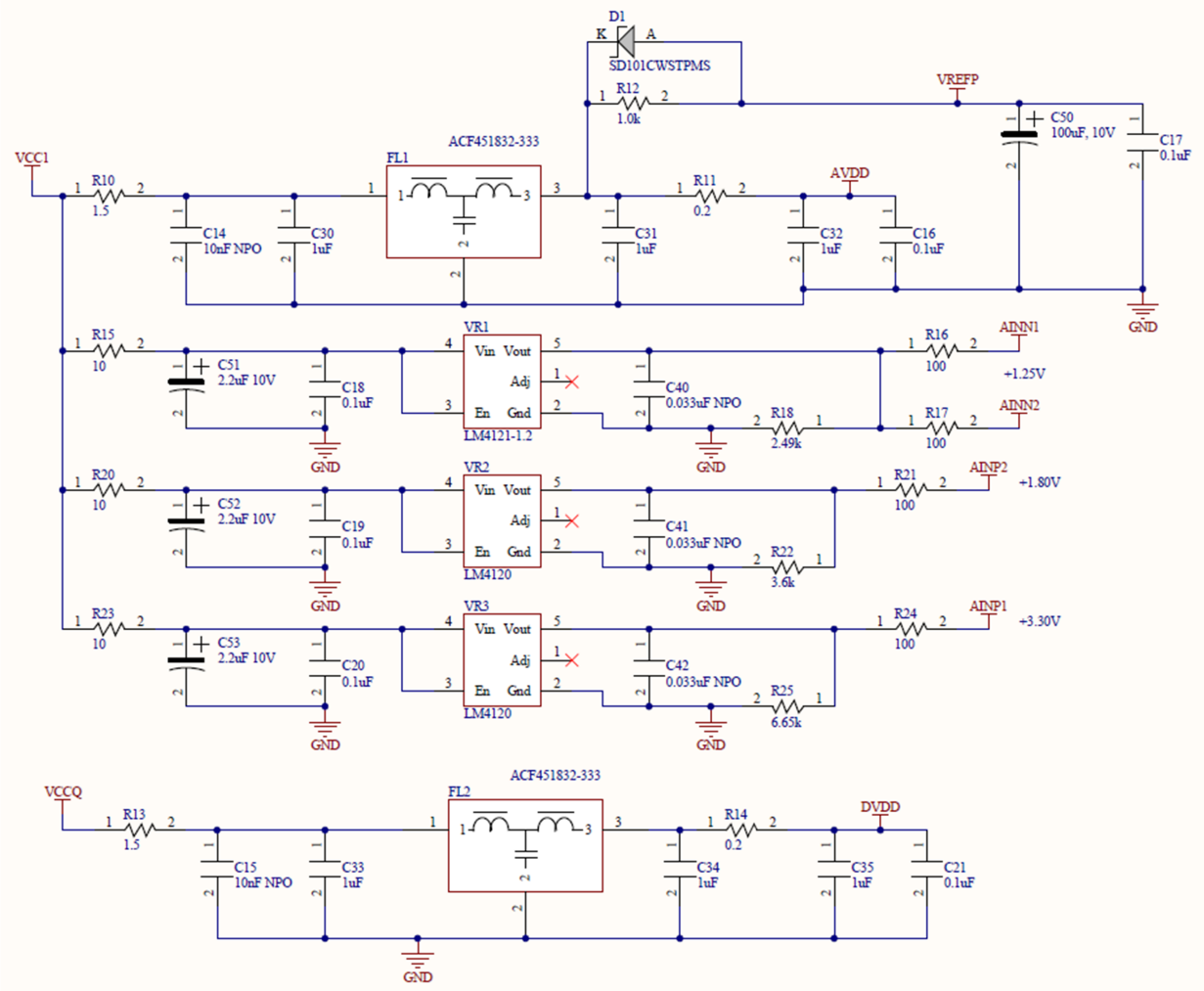

Figure 7. Input Power Circuit

4 Irradiation Facility and Setup

The SEE testing described in this test report was performed at the Cyclotron Institute at Texas A&M University (TAMU) using their K500 Cyclotron. The testing was performed in air using the 15 MeV/n beam. When necessary, beam degraders were inserted into the beam line to achieve the desired LET and a wider LET range for a given ion. The beam characteristics and dosimetry were provided by the Texas A&M heavy ion test facility. TAMU delivered the beam with a high degree of uniformity over a 1-in diameter circular cross sectional area using the in-air test system. Uniformity was achieved by magnetic defocusing and by thin foil scattering. The beam uniformity and flux are determined using an array of five plastic scintillators coupled to photo multiplier tubes, located in the diagnostic chamber adjacent to and upstream from the target. Four of the five detectors are fixed in position and set up to measure beam particle counting rates continuously at four characteristic points 1.64 inches (41.7 mm) away from the beam axis center. The fifth scintillator is inserted to measure the beam particle counting rate right at the beam axis and was removed to provide an unobstructed beam during testing. The control software determines the beam uniformity (ranging from 0% to 100%), axial gain (%), and beam flux (in particles/cm^2/s) based on the scintillator counting rates. The parameters are displayed on the computer screen in the control room and are updated about once every second. For all beam experiments the air gap between the die surface and the ion port window was 40 mm.

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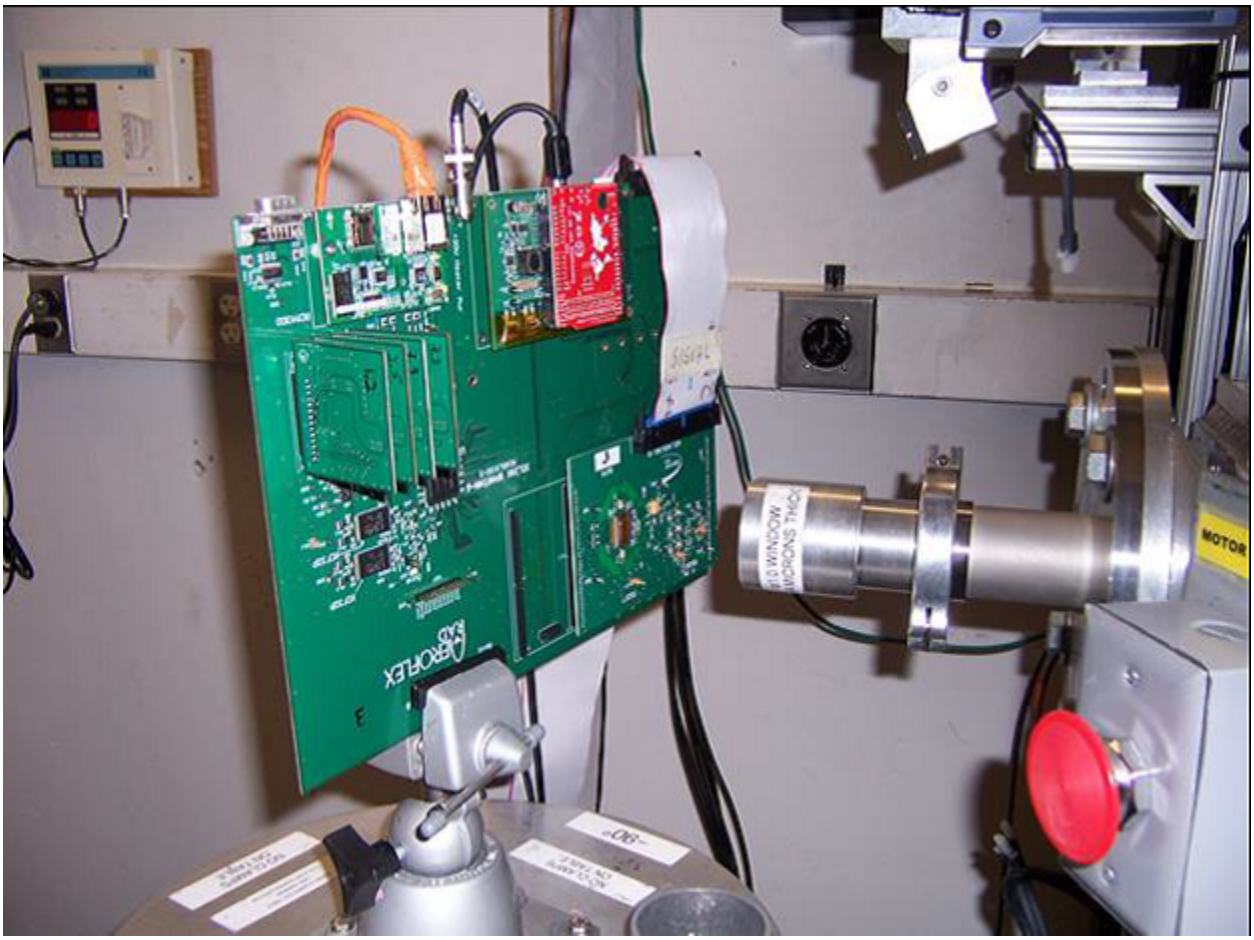

Figure 8. Test Fixture for SEE Testing

Figure 8 shows a photograph of the test fixture used for SEE testing. All DUT were de-lidded prior to testing and all exposures took place from the top surface providing a distance to the active layer in silicon, through the passivation and metallization layers of approximately 10 µm.

4.1 Depth, Range, and LET_{eff} Calculation

The ADS1282-SP is fabricated in the Texas Instruments high-performance analog 130-nm BiCMOS process (HPA07) with a back-end-of-line (BEOL) stack consisting of X levels of standard thickness aluminum metal on a Y-µm pitch, and a fourth level of thick aluminum. The total stack height from the surface of the passivation to the silicon surface is 10 µm, based on nominal layer thickness as shown in Figure 9. No polyimide or other coating was present so the uppermost layer was the nitride passivation layer (PON). Accounting for energy loss through the 1-mil thick Aramica (Kevlar®) beam port window, the 40-mm air gap, and the BEOL stack over the ADS1282-SP, the effective LET (LET_{eff}) at the surface of the substrate and the depth and ion range was determined with the custom RADsim-IONS application (custom tool developed at Texas Instruments based on SRIM 2013 [9]) simulations for the two primary ions used for the experiments. The results are shown in Table 2. The stack was modeled as a homogeneous layer of silicon dioxide.

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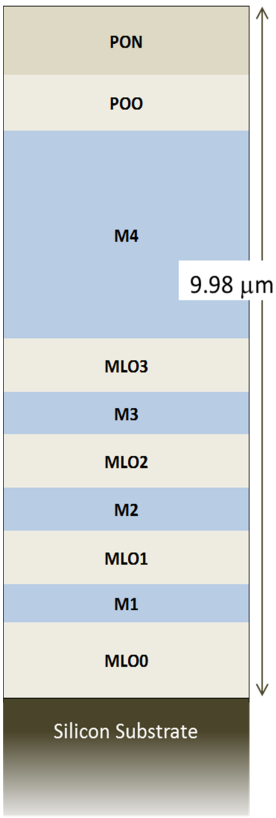

Figure 9. HPA07 Technology BEOL Stack Cross-Section on the ADS1282-SP

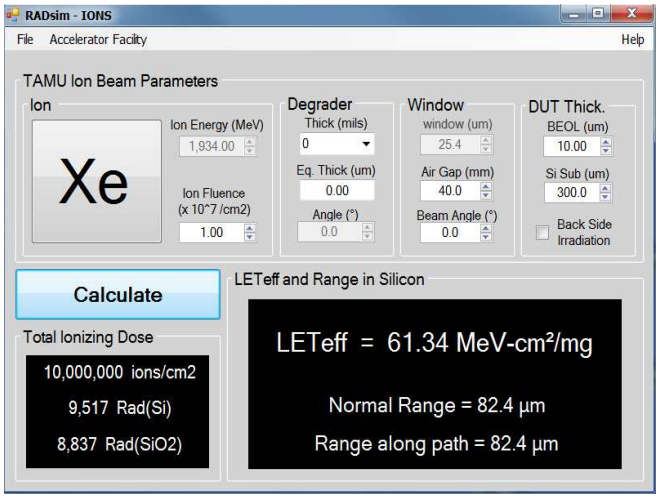

Figure 10. RADsim-IONS Application GUI

Generalized cross-section (left) of the HPA07 technology BEOL stack on the ADS1282-SP. GUI of RADsim-IONS application (right) used to determine key ion parameters: LET_{eff}, depth, and range for a given ion type, energy, and stack.

Table 2. Ions and Angles Used in SEE Experiments

ION TYPE	ANGLE OF INCIDENCE	DEPTH IN SILICON (µm)	RANGE IN SILICON (µm)	LET_{eff} (MeV-cm^2/mg)
Ne	0°	250.1	250.1	2.80
Ar	0°	169.5	169.5	8.71
Kr	0°	106.8	106.8	30.96
Ag	0°	87.8	87.8	48.47
Ag	32°	72.9	72.9	57.63
Xe	0°	82.4	82.4	61.34
Xe	30°	70.0	70.0	71.29
Xe	45°	55.3	55.3	88.13
Xe	50°	49.3	49.3	97.38

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5 Test Setup and Procedures

Figure 11 shows the test circuit that was used. The positive voltage reference, VREFP, and the analog power supply, AVDD, are driven by a filtered VCC1 power supply. The VCC1 power supply also provides input power to three voltage regulators: 3.3 V, 1.25 V, and 1.8 V. The VCCQ1 power supply is filtered and provides the input power for the digital power supply, DVDD.

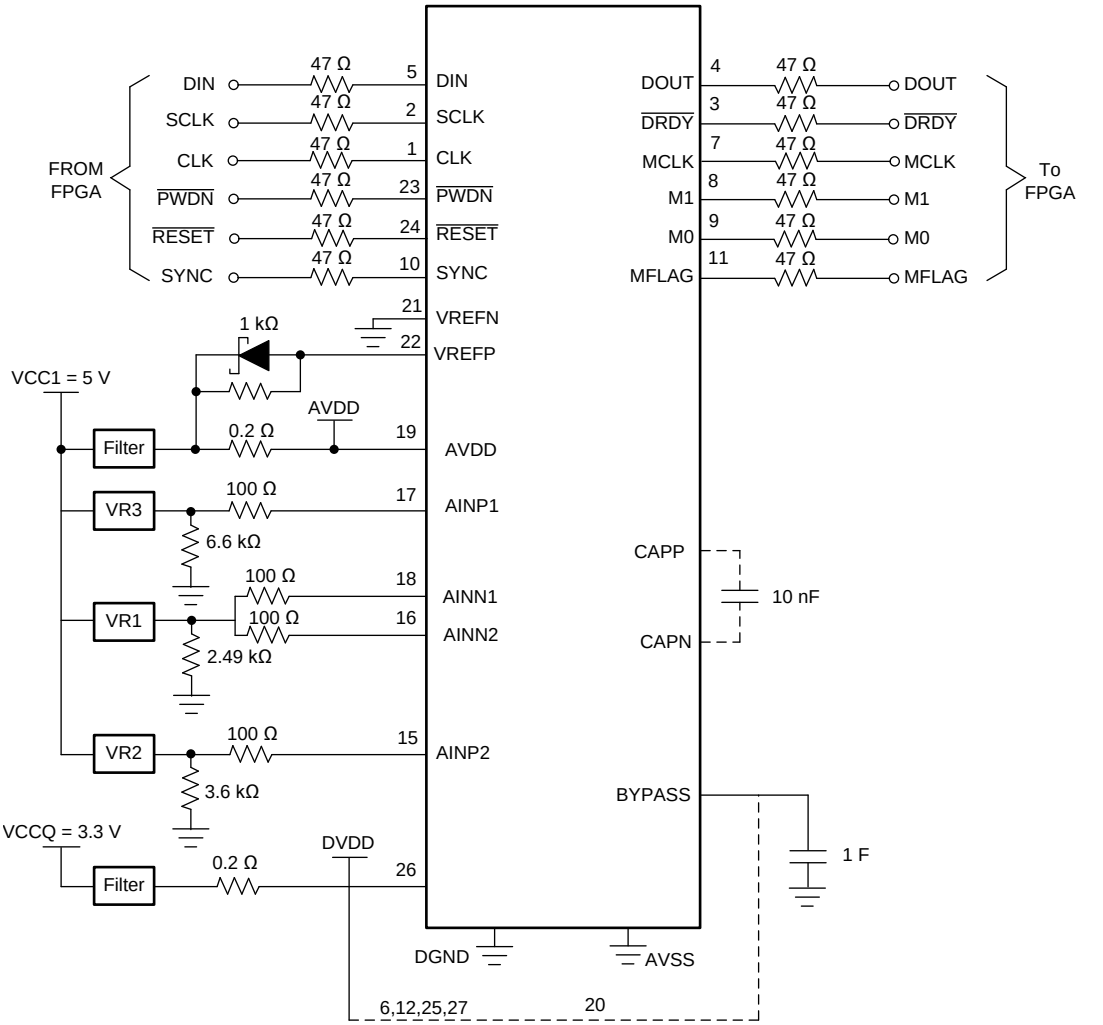

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Figure 11. Test Circuit

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5.1 SEE Testing Block Diagram

Figure 12 shows a block diagram of the test setup used for SEE testing. The inputs to the ADS1282-SP (DIN, SCLK, PWRDN_N, RESET_N, and SYNC) are connected to I/O pins on a Spartan 6 FPGA. The CLK operates at 4 MHz and the SCLK operates at 2 MHz. The outputs of the ADS1282-SP (DOUT, DRDY_N, MCLK, M1, M0, and MFLAG) are also connected to I/O pins on the FPGA. The FPGA sends commands to the ADS1282-SP and executes reading and writing to ADS1282-SP registers.

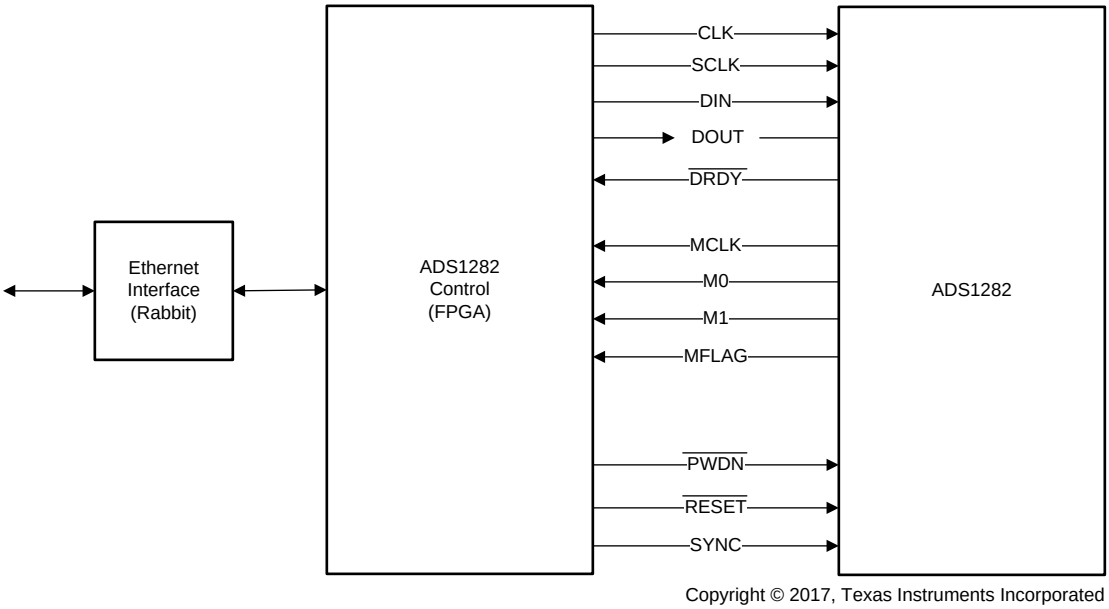

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Figure 12. SEE Testing Block Diagram

The SEE Test Setup for the TI ADS1282-SP is shown in Figure 13. Each TI ADS1282-SP is mounted on an individual DUT board that interfaces to the Memory Test Board. The Keithley 2425-C and 2420 Source Meters provide the DUT AVDD and DUT DVDD voltages and measures the associated currents. The Housekeeping Power Supply provides the ±5 V and +24 V for the Memory Test Board. The Agilent 34970A Data Acquisition Unit and Agilent 34901A Multiplexer Plug-in provide the capability to measure the DUT AVDD, DUT DVDD and +3.3-V voltages at the DUT board. The Shutter Status Monitor records the beam shutter position. The laptop personal computer (PC) controls the test equipment and records the test data [6].

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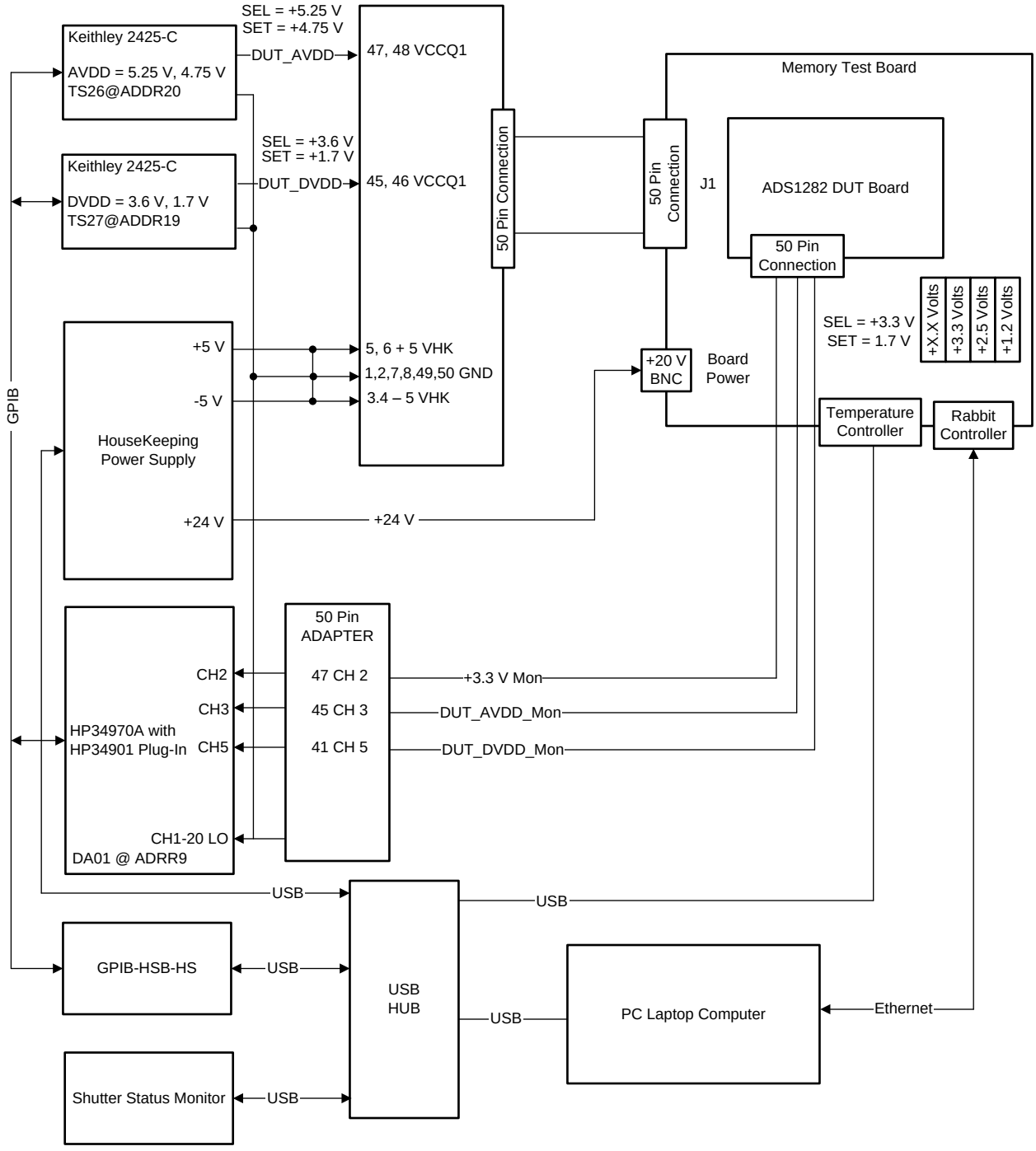

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Figure 13. SEE Test Circuit

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5.2 Test Parameters

The following parameters were measured during SEL and SET testing at approximately 1-second intervals:

- DUT temperature
- AVDD voltage and AVDD current
- DVDD voltage and DVDD current
- 3.3-V supply on the memory test board
- Beam shutter status

Table 3 lists the settings used for various parameters of the DUT and ion beam. Additionally, data conversion output was measured for SET testing.

Table 3. Settings Used for See Testing Parameters

PARAMETER	SEL	SET
DUT temperature	85°C and 125°C	Ambient
AVDD	+5.25 V	+4.75 V
DVDD	+3.6 V	+1.7 V
Maximum fluence	10^7 ions/cm^2	10^6 ions/cm^2 or 100 events

5.3 Test Conditions

The register configuration for the ADS1282-SP used the default settings with the exception of the MUX Select bits in the Configuration 1 Register, and the Digital Filter Select bits in the Configuration 0 Register. For SEL testing, the MUX Select was configured to the default value of AINP1 and AINN1. For SET testing, the MUX Select was configured for the default value of AINP1 and AINN1, AINP2 and AINN2, and Internal Short via 400 Ω as required [6].

For SEL testing, the Digital Filter Select was configured for the default value of Sinc + LPF Filter Blocks. For SET testing, the Digital Filter Select was configured for the default value of Sinc + LPF Filter Blocks and On-Chip Bypassed, Modulator Output Mode, as required [6].

Since SEE testing is performed in a noisy environment, a number of bits of conversion data were masked until no error events occurred without irradiating the ADS1282-SP [6]. The signals monitored during the test were routed to the control room (approximately 20-feet away) using shielded coaxial cable. Table 4 lists the ions, angles, and LETs used to characterize the SEE response of the ADS1282-SP devices.

Table 4. Ions Used for SEL Characterization

ION	ANGLE	LET (MeV·cm^2/mg)
Ne	0°	2.7
Ar	0°	8.4
Kr	0°	28.3
Ag	0°	42.8
Ag	32°	50.5
Xe	0°	52.3
Xe	30°	60.4
Xe	45°	74
Xe	50°	81

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6 SET Test Results

A SET event is defined as the duration when the absolute value of the (sample – reference) is greater than the mask threshold [6]. As an example, if ten consecutive samples exceed the reference sample by greater than the mask threshold, then this is one error event and ten errors. The number of error events were used to determine the number of transients collected until the run is stopped [6].

SET testing was performed with AVDD set to 4.75 V and DVDD set to 1.7 V. Figure 14 shows the cross-section for register upsets. Weibull fit parameters are shown in Table 5.

Table 5. Weibull Fit Parameters for Register Upsets

PARAMETER	VALUE
LET_{th} (MeV·cm^2/mg)	1.4
σ sat (cm^2)	1.3E–05
Width, W (MeV·cm^2/mg)	15
Exponent, s	1.4

Table 6 lists the runs and test conditions as well as the result of the runs for DUT serial numbers 11 and 14. Note: the DUT board with serial number 14 was configured with the bypass pin connected directly to DVDD.

Table 6. SET Run Log

Run	SN	Ion	Effective LET (MeV·cm^2/mg)	Effective Fluence (ion/cm^2)	AVDD (Volts)	DVDD (Volts)	Config	Errors	Error Events	DRDY_N Errors	Comments
26	11	Ag@0°	42.8	9.65E+05	4.75	3	AIN1	6306	400	2455	
27	11	Ag@0°	42.8	9.75E+05	4.75	3	AIN2				Configuration Registers Reset
28	11	Ag@0°	42.8	1.02E+06	5.25	3	AIN1	5593	183	1661	
29	11	Ag@0°	42.8	9.44E+05	5.25	3	AIN2				Configuration Registers Reset
38	11	Xe@0°	52.3	1.03E+06	5.25	3	AIN1	6679	222	1323	
49	14	Xe@0°	52.3	1.05E+06	4.75	1.7	AIN1	4288	176	4308	
50	14	Xe@0°	52.3	9.85E+05	4.75	1.7	AIN2				Configuration Registers Reset
51	14	Ar@0°	8.4	9.67E+05	4.75	1.7	AIN1	6269	58	134	
52	14	Ar@0°	8.4	1.06E+06	4.75	1.7	AIN2				Configuration Registers Reset
53	14	Ne@0°	2.7	1.02E+06	4.75	1.7	AIN1	1	1	0	
54	14	Ne@0°	2.7	1.03E+06	4.75	1.7	AIN2	4	4	0	No Configuration Registers Reset
55	14	Kr@0°	28.3	1.00E+06	4.75	1.7	AIN1	3746	364	1010	
56	14	Kr@0°	28.3	1.01E+06	4.75	1.7	AIN2				Configuration Registers Reset

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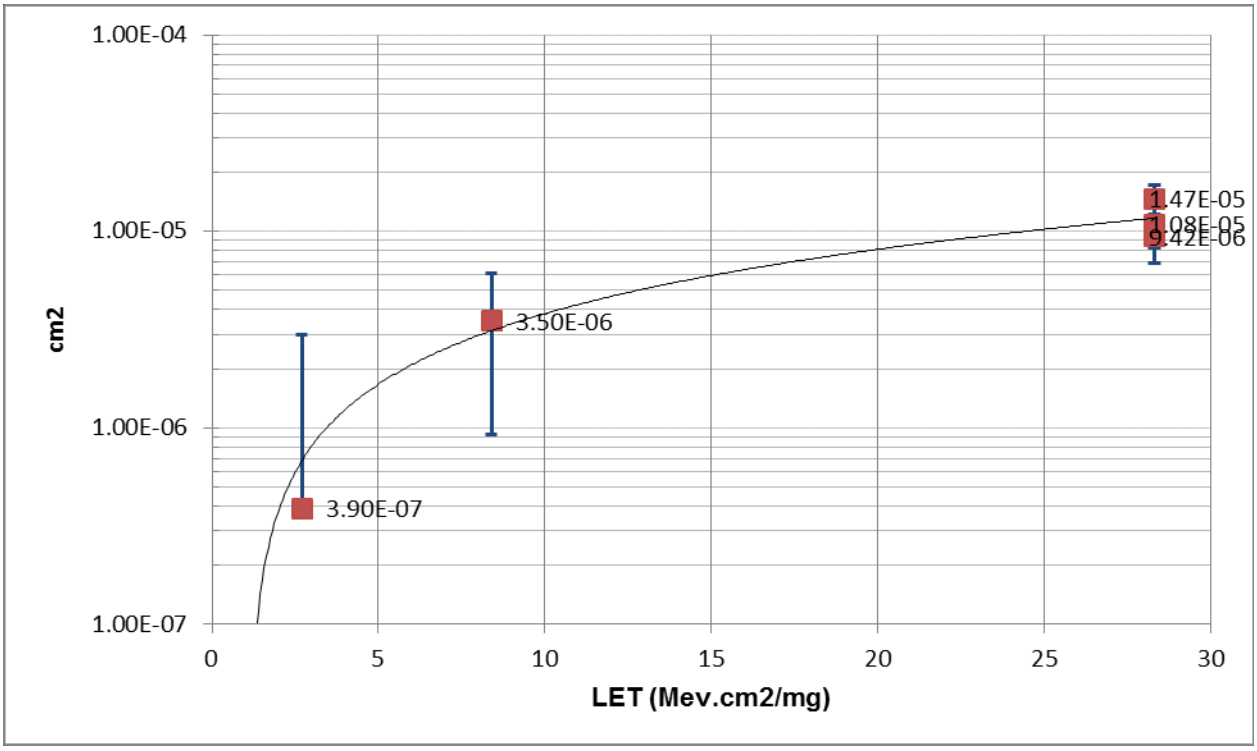

Figure 14. Cross-Section for Register Upsets

To disambiguate noise from bit errors, the least significant bits of the data conversion output were masked until no error events were observed under no irradiation. The ion beam was subsequently turned on, and the output was observed until the specified number of transients were recorded or the fluence reached 10^6 ions/cm^2.

During SEL testing and during some of the SET runs, single-event functional interrupts (SEFI) were observed, which required the device to be reset to restore functionality. Cross-section data on this error mode cannot be calculated with any confidence as the device reset under irradiation and some SEFI may clear before they are detected. At the same time, runs that exhibited a SEFI mode would inhibit the collection of further SET and thus will underestimate the error cross section [6].

To avoid confounding of multiple error sources, the test runs in which register SEU's were observed were excluded when calculating the SET cross section. Figure 15 shows the resulting cross section, and the Weibull fit parameters are listed in Table 7.

Table 7. Weibull Fit Parameters

PARAMETER	VALUE
LET_{th} (MeV·cm^2/mg)	2.7
σ sat (cm^2)	3.7E–04
Width, W (MeV·cm^2/mg)	27
Exponent, s	0.9

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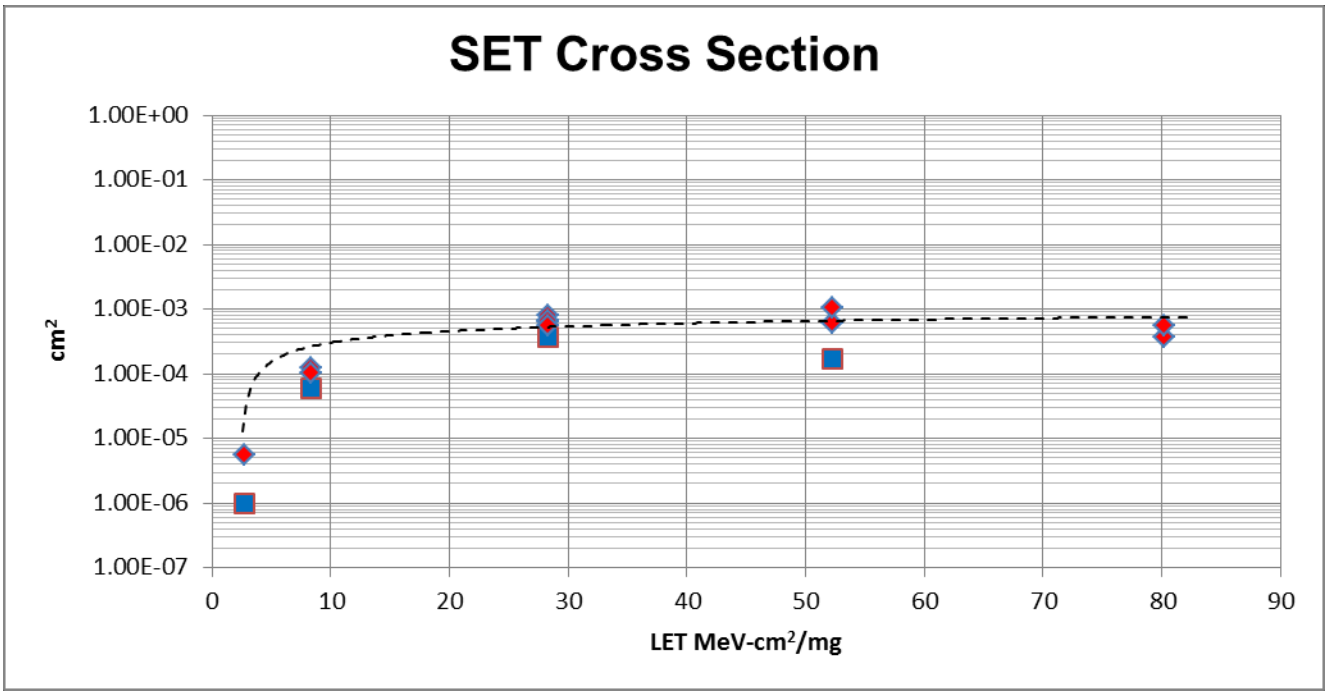

Figure 15. SET Cross Section

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7 SEL Test Results

The device is SEL-free up to 50.5 MeV·cm^2/mg at 125°C. At 85°C, the device did not exhibit latch-up up to 60.4 MeV·cm^2/mg.

Table 8 lists the runs and test conditions as well as the result of the runs for DUT serial numbers 11, 12, and 13. The SEL runs for serial numbers 11, 12, and 13 indicate the ADS1282-SP is latch-up immune to an LET of 50.5 MeV·cm^2/mg at temperatures of 85°C and 125°C.

Table 8. SEL Run Log

Run	SN	Ion	Effective LET (MeV·cm^2/mg)	Effective Fluence (ion/cm^2)	Temp (°C)	Result
30	11	Ag@0°	42.8	1.00E+07	85	No Latch-up.
31	11	Ag@32°	50.5	9.97E+06	85	No Latch-up
32	12	Ag@32°	50.5	9.95E+06	85	No Latch-up
33	13	Ag@32°	50.5	9.99E+06	85	No Latch-up
34	13	Ag@0°	42.8	1.00E+07	125	No Latch-up. AVDD Current changed from 7.8 mA to 8.6 mA and the data output was 0x7FFFFFFF. After reset, the AVDD Current returned to normal and there was no degradation to the device.
35	13	Ag@32°	50.5	9.96E+06	125	No Latch-up
36	12	Ag@32°	50.5	1.00E+07	125	No Latch-up
37	11	Ag@32°	50.5	9.96E+06	125	No Latch-up

For SEL testing, the analog power supply, AVDD was set to 5.25 V, and the digital power supply, DVDD, was set to 3.6 V. Testing was performed at 85°C and 125°C with a control tolerance of ±5°C. In one run at a LET of 52.3 MeV and temperature of 125°C, a high-current state was observed on the AVDD supply. After remaining at 180 mA for 60 seconds, the device returned to nominal current mode without power cycling. After cycling power, it was observed that the output codes of the ADC were in error by 20% greater than actual [6].

In a different test run, a second device was irradiated at a LET of 80 MeV and temperature of 85°C. In addition, a 100-mA current limit was applied to the power supply. Under this condition, the device entered high-current state. Upon power cycling, an increase in nominal AVDD current from 7.8 mA to 10.4 mA was observed. In addition, the conversion values were found to be in error by 20% greater than actual.

The observed results indicate that the ADS1282-SP is immune to latch-up to a LET of 50.5 MeV·cm^2/mg at a temperature of 125°C and up to 60.4 MeV·cm^2/mg at a temperature of 85°C.

Figure 16 and Figure 17 illustrate representative SEL current measurements for a run without event, and a run with an event.

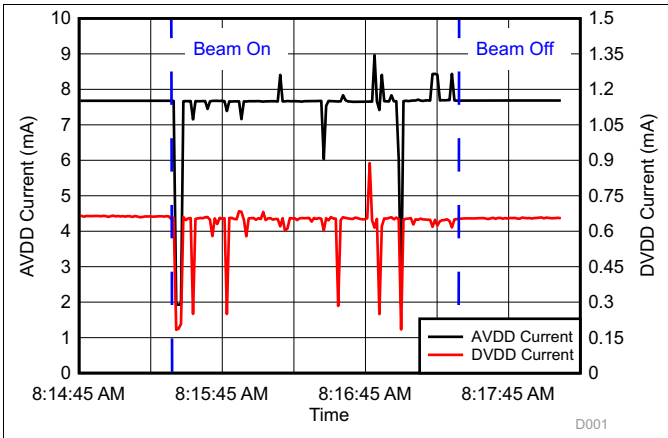

Figure 16. Representative SEL Current Measurements Without Event

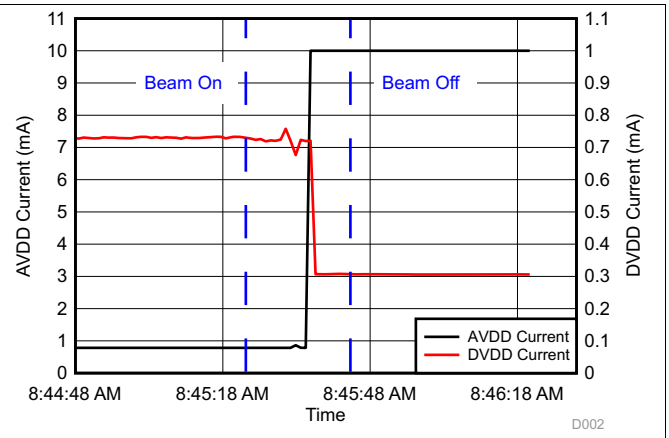

Figure 17. Representative SEL Current Measurements With Event

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8 Conclusions

TI's ADS1282-SP was tested for single-event effects. No latch-up was detected up to a LET of 50.5 MeV·cm^2/mg and temperatures of 85°C and 125°C. The device exhibited single-event upsets in the data converter output with a threshold of 2.6 MeV·cm^2/mg, and the saturated cross section was 3.7E–4 cm^2.

9 Acknowledgment

The tests described in this paper were performed by Aeroflex RAD, Inc. The results from their testing are summarized in a report (see [6]), serving as the basis for the material reported in this application report.

10 References

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