

# ***Band-Pass Filter Design Techniques for High-Speed ADCs***

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## **ABSTRACT**

Several well-known methods exist for designing passive inductor-capacitor (LC) filters with resistive load terminations. However, when LC filters are used to drive the analog input pins of a high-speed analog-to-digital converter (ADC), special consideration must be given to the ADC input impedance. Not accounting for the ADC input impedance often results in a filter design that does not meet the original target specifications. This discrepancy is especially true with wide bandwidth filter designs, which are becoming increasingly common in wireless communication infrastructure applications.

This application note describes the methodology to absorb the ADC input impedance into the filter design so that the original filter specifications are met up-front, resulting in a first-pass filter design.

## **Contents**

1	Introduction .....	2
2	Step 1: Getting Key Filter Specifications .....	3
3	Step 2: Designing the Filter With a Resistive Load (Using Generic Tools) .....	3
4	Step 3: Designing the Filter with the ADC Input Model (Using the TI-TINA Tool) .....	5
5	Conclusion .....	9

## **List of Figures**

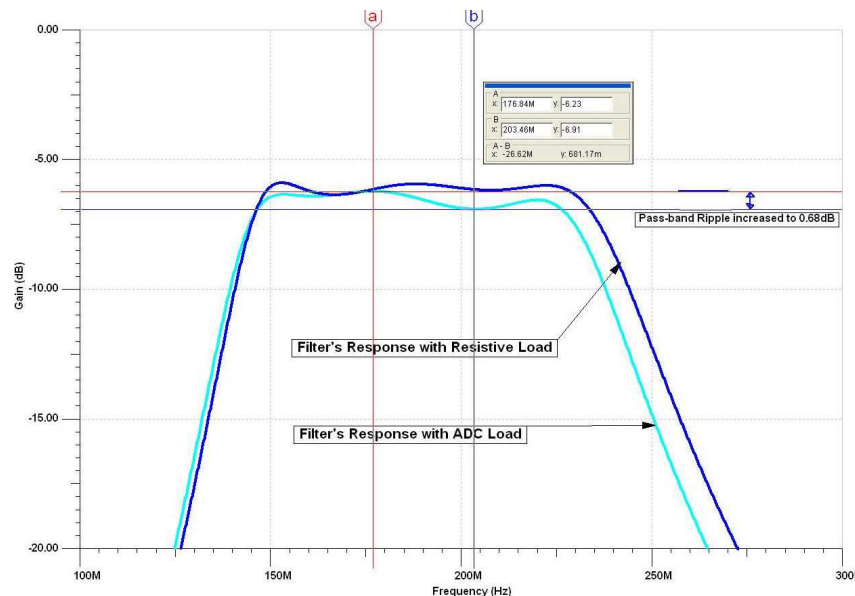
1	Example Filter Response .....	2
2	Filter Specifications .....	3
3	Filter Model .....	3
4	Single-Ended and Differential Filters .....	5
5	Single-Ended and Differential ADC Models .....	5
6	Capacitance vs Frequency .....	6
7	Resistance vs Frequency .....	6
8	AC Analysis .....	7
9	BPF Designed for 60-MHz Band at 184-MHz Center Frequency .....	8
10	BPF with Modified Last Shunt Arm and ADC Load .....	8
11	Frequency Response With and Without ADC Load .....	9

## 1 Introduction

The methodology for designing LC filters with resistive load terminations is quite well-known. However, when LC filters are used to drive the analog input pins of a high-speed ADC, special consideration must be given to the ADC input impedance. Not accounting for the ADC input impedance often results in a filter design that does not meet the original target specifications.

In this following example, the requirement is to design a filter for driving the ADS41B49 analog inputs. The target specifications for the filter are pass band = 60 MHz and center frequency = 184 MHz, with the pass-band ripple less than 0.5 dB.

The filter was designed using a commonly-available design tool using a resistive load. The filter frequency response is shown in the [Figure 1](#) and meets the target specifications. However, when the same filter is connected to the ADS41B49 input pins, it is discovered that the frequency response has changed. The pass-band ripple increases to 0.68 dB, and exceeds the target specification.



**Figure 1. Example Filter Response**

The following sections describe a methodology to design the filter while taking into account the effect of ADC input impedance.

The procedure consists of the following steps:

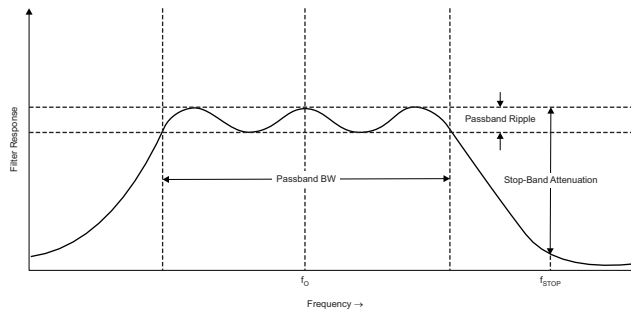
- [Step 1](#) and [Step 2](#) consist of the filter design using conventional and well-known methods.
- [Step 3](#) describes the modification required to include the effect of the ADC input impedance.

## 2 Step 1: Getting Key Filter Specifications

First, decide the main specifications of the filter:

- Width of the passband and center frequency
- Passband ripple
- Stop-band frequency and attenuation
- Source and load termination (determined by the driving amplifier and ADC termination requirements)

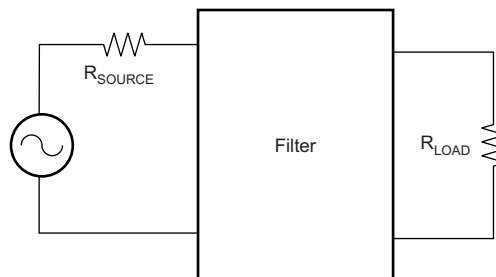
An example of filter specifications is shown in [Figure 2](#).



**Figure 2. Filter Specifications**

## 3 Step 2: Designing the Filter With a Resistive Load (Using Generic Tools)

Several filter design tools are available to design a filter for the given specifications. For example, freeware tools such as AADE, RF Design, or Circuit Sage that are available on the internet. These tools allow the user to choose the topology and the order of the filter that meets the required specifications. An example filter model is shown in [Figure 3](#).



**Figure 3. Filter Model**

### 3.1 Selecting Filter Topology

The user can choose from various filter topologies such as Butterworth, Chebyshev, or Elliptic. Additionally, the structure of the filter must be decided ( $\pi$ -type or T-type). In most cases, the  $\pi$ -type structure works best because the last shunt arm of the filter can be conveniently modified to absorb the ADC input impedance model (as described in the following sections). TI high-speed ADC data sheets (such as the [ADS58C20](#), [ADS41B49](#), and [ADS61B49](#)) provide an equivalent model of the ADC input impedance.

For example:

- For the ADS41B49, a differential model is provided consisting of a combination of a shunt resistor and a shunt capacitor.
- In the case of the ADS58C20, which provides the impedance as a series combination, it is easy to derive an equivalent shunt combination.

Once the topology and structure is identified, the filter can be designed for the given load impedance and other specifications using ideal components.

### 3.2 Designing the Filter

Using the above information, the filter tool creates a design that meets the desired specifications and also provides the required values of the inductors and capacitors.

### 3.3 Redesigning the Filter with Non-ideal (Finite-Q) Inductors

The filter designed in the previous section uses ideal components and must be modified to account for real-world components. In most cases, it is necessary to consider the effect of finite-Q inductors on the frequency response of the filter. Q values can be obtained from the inductor manufacturer data sheet. All inductors in the ideal design should be modified with the respective finite-Q values.

Rerun the tool to ensure that the design meets desired specifications, even with finite-Q.

## 4 Step 3: Designing the Filter with the ADC Input Model (Using the TI-TINA Tool)

### 4.1 Generating a Differential Filter Model

Most filter tools generate a single-ended circuit representation of the design, as shown in Figure 4a. This representation should be converted into a differential network (as shown in Figure 4b), to enable differential analysis.

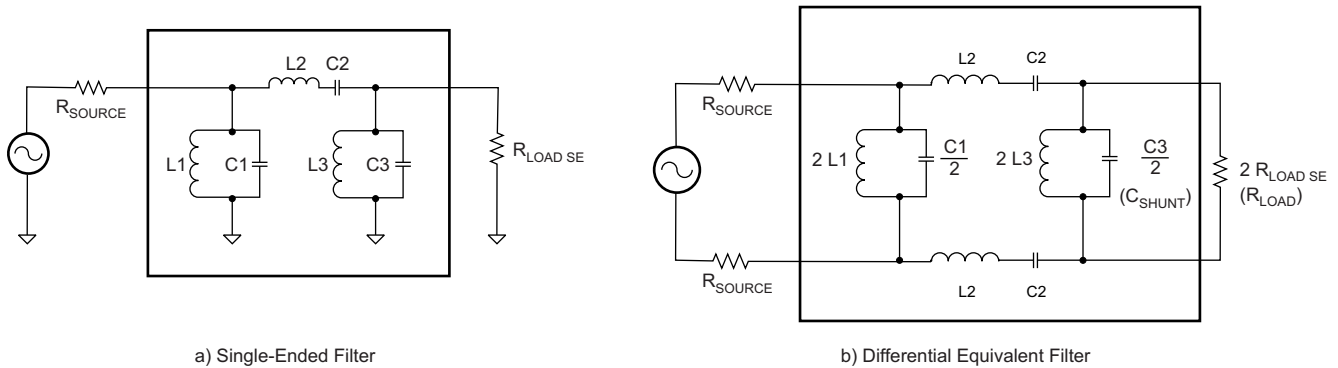


Figure 4. Single-Ended and Differential Filters

Any single-ended structure in the ADC input impedance model (as shown in Figure 5a) must also be converted to its equivalent differential value, as shown in Figure 5b. This conversion is required for differential ac analysis using TI-TINA.

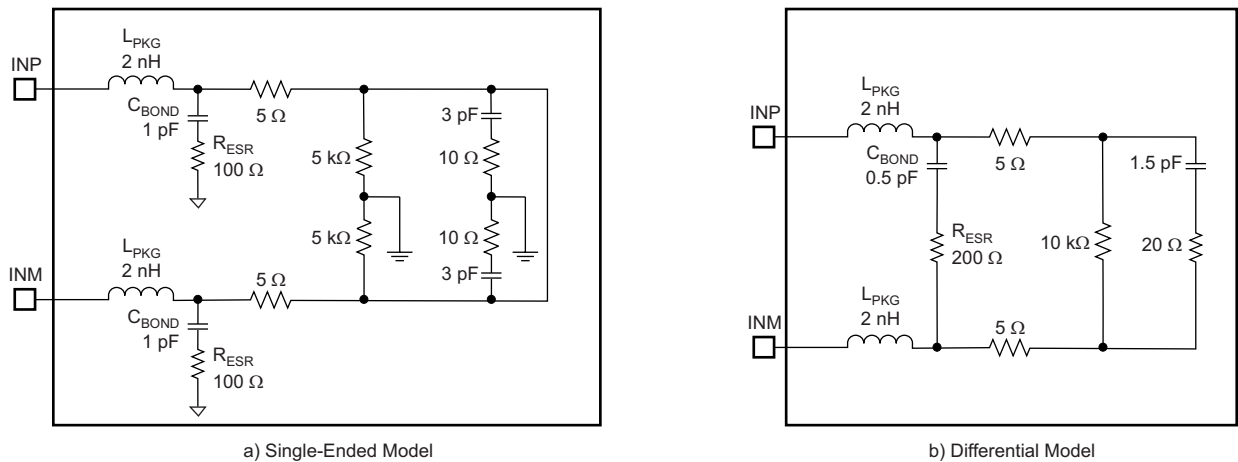


Figure 5. Single-Ended and Differential ADC Models

## 4.2 Absorbing the ADC Impedance in the Filter Design

In the next step, the filter performance must be verified with the ADC input model. For this, it is necessary to absorb the ADC equivalent input impedance in the last shunt arm of the filter.

The components used in the shunt arm can be modified using [Equation 1](#) and [Equation 2](#). This process is described as:

- Replace  $R_{LOAD}$  with  $R_{LOAD\_NEW}$ :

$$R_{LOAD\_NEW} = \frac{R_{IN} - R_{LOAD}}{R_{IN}} \times R_{LOAD} \quad (1)$$

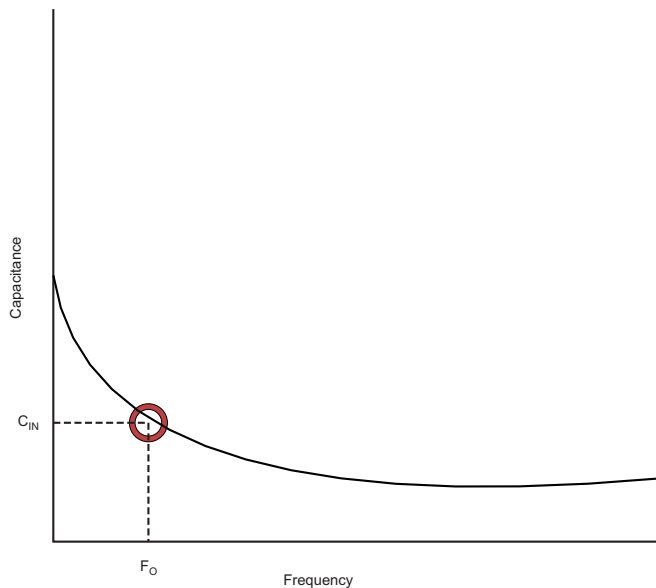
- Modify  $C_{SHUNT}$  of the filter to  $C_{SHUNT\_NEW}$ :

$$C_{SHUNT\_NEW} = C_{SHUNT} - C_{IN} \quad (2)$$

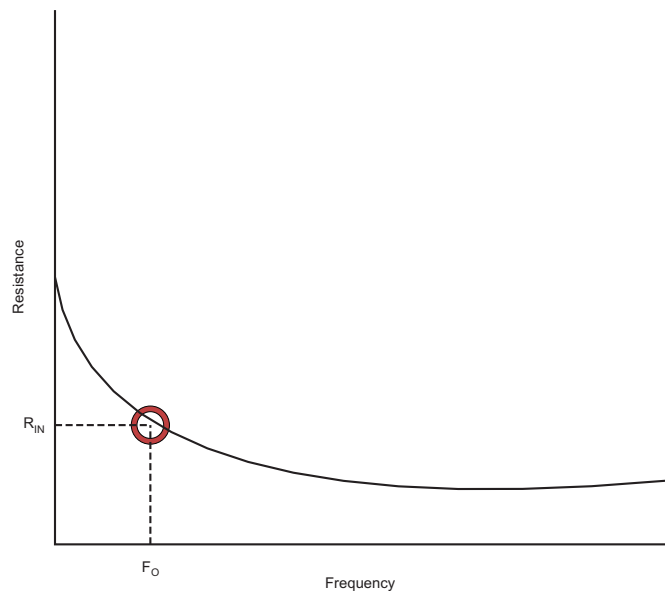
Where:

$C_{IN}$  is the equivalent ADC input capacitance between INP and INM at the passband center frequency (from the  $C_{IN}$  vs frequency curve, [Figure 6](#)).

$R_{IN}$  is the equivalent ADC input resistance between INP and INM at the passband center frequency (from the  $R_{IN}$  vs frequency curve, [Figure 7](#)).



**Figure 6. Capacitance vs Frequency**



**Figure 7. Resistance vs Frequency**

### 4.3 TI-TINA Setup

A TI-TINA project can be setup as shown in Figure 8. An ac analysis can be run to plot the filter transfer function with the ADC load. Note that the filter output must be measured at the ADC input pins, INP and INM (shown by the voltmeter Vadc\_input in Figure 8). Set up the equation for the transfer function of the filter using the node names for the input and output pins.

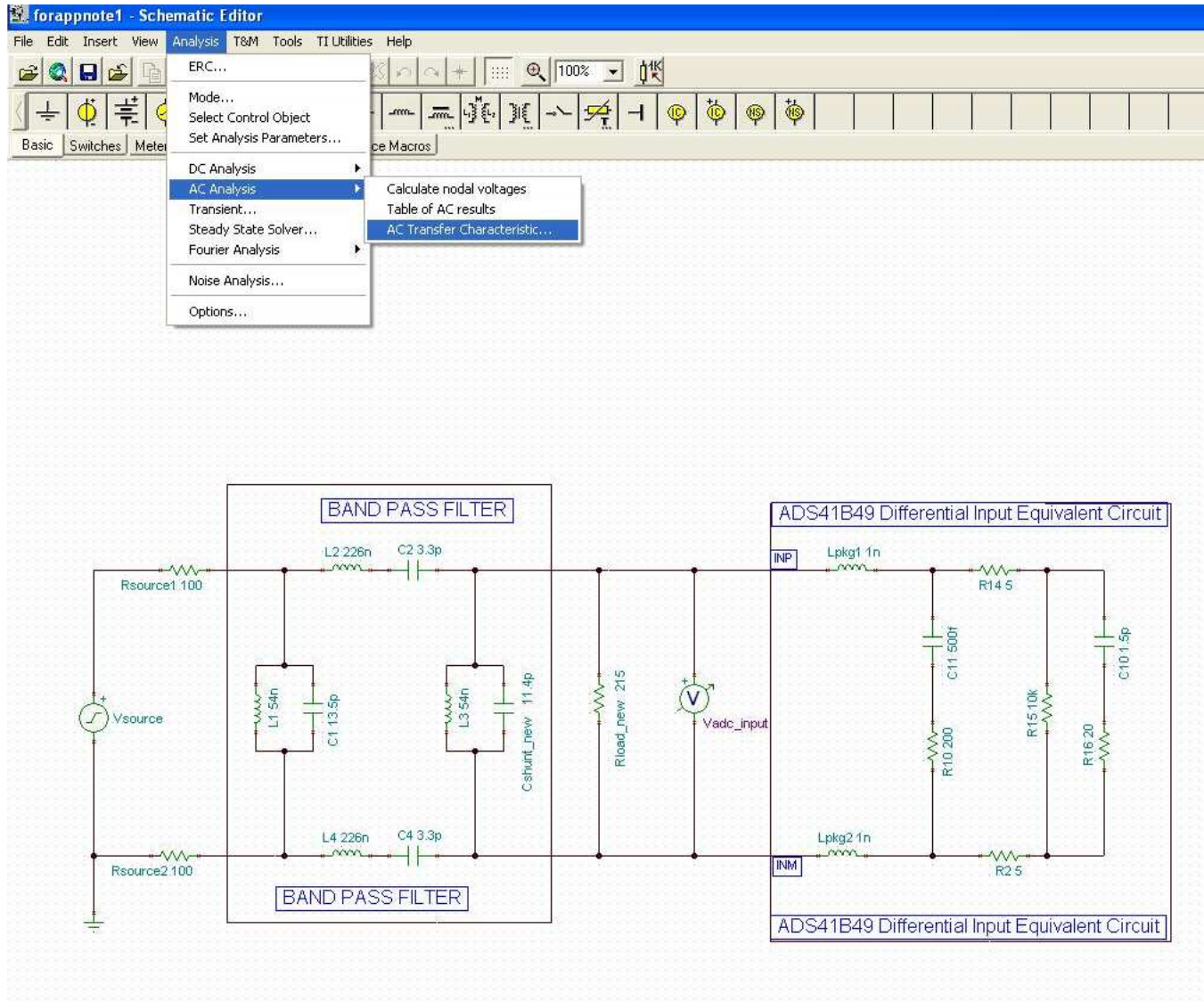


Figure 8. AC Analysis

Check the frequency response of the filter with the ADC load to see if it meets the target specifications.

Note that the last shunt arm of the filter must be modified using the value of the ADC equivalent capacitor at the center frequency of the passband. Because of this modification, when the ac analysis is run over the entire frequency range, some variation in the frequency response is expected when compared to the case with the resistive load only. Verify if the achieved response meets the desired specifications.

### 4.3.1 Example Filter Design

Consider the following band-pass filter design as an example. This filter has a pass band of 60 MHz, centered at 184 MHz with a pass-band ripple better than 0.5 dB. Using the filter design tool and following the previously mentioned steps, we arrive at the band-pass filter (BPF) circuit shown in the TI-TINA schematic of Figure 9.

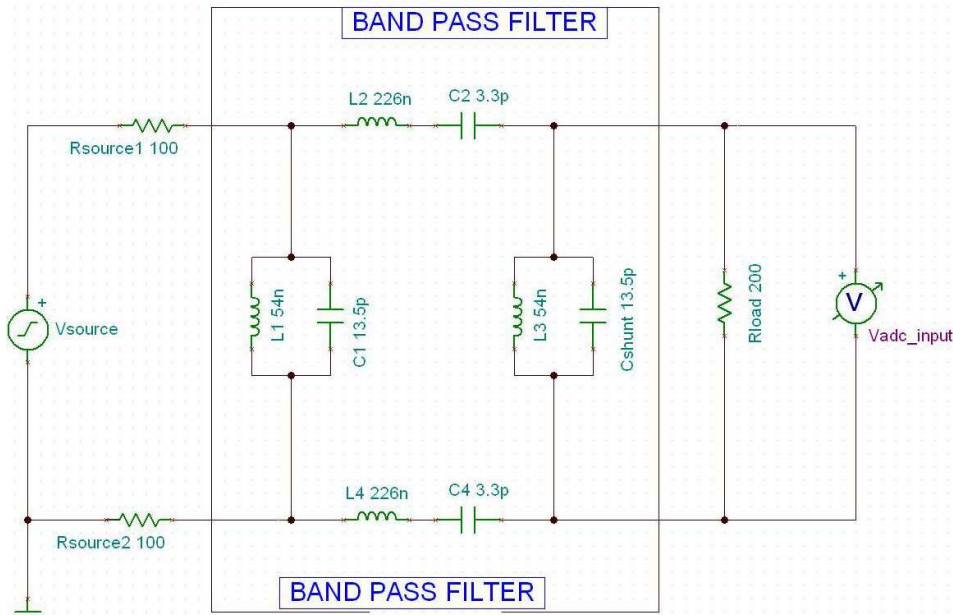


Figure 9. BPF Designed for 60-MHz Band at 184-MHz Center Frequency

When the ADC load is connected, the transfer function of the filter gets modified. We can minimize the effect of the ADC load by absorbing the ADC equivalent input resistance and capacitance in the last shunt arm of the filter as shown in the TI-TINA schematic of Figure 10.

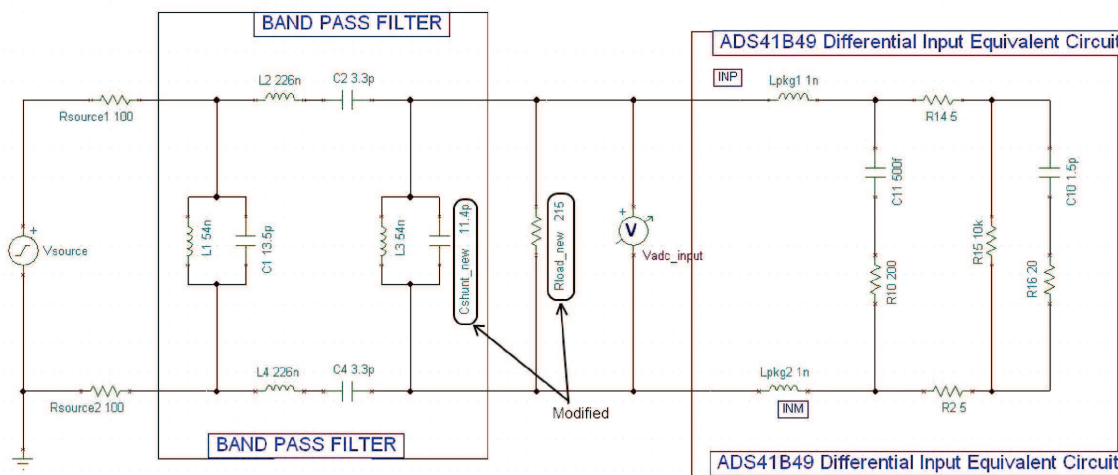


Figure 10. BPF with Modified Last Shunt Arm and ADC Load



To absorb ADC load impedance, the capacitance in the last shunt arm of the filter is modified to 11.4 pF from the original value of 13.5 pF, using the value of the ADC equivalent capacitor ( $C_{IN}$ ) at the center frequency of 184 MHz (which is 2.1 pF). Similarly,  $R_{LOAD}$  is modified to 215  $\Omega$  from the original value of 200  $\Omega$ , using the ADC equivalent resistor ( $R_{IN}$ ) at the center frequency of 184 MHz (which is 3000  $\Omega$ ). The filter response with and without ADC load is shown in Figure 11.

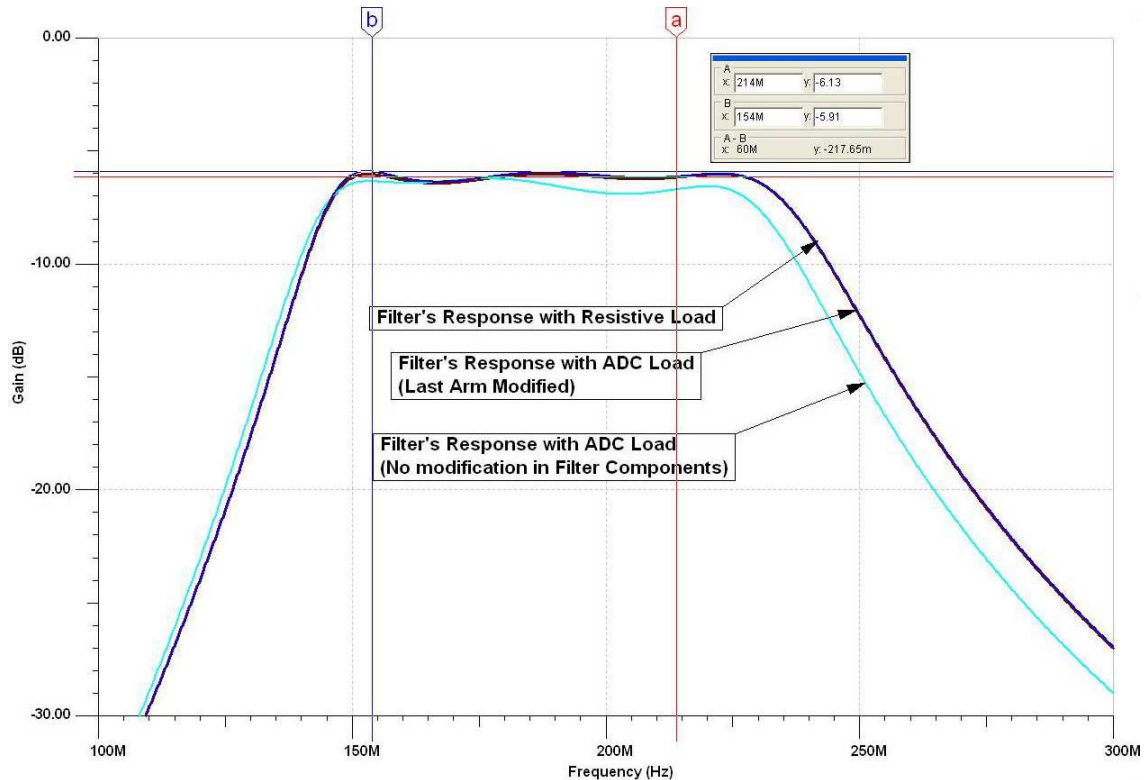


Figure 11. Frequency Response With and Without ADC Load

The curve labeled *Filter's Response with Resistive Load* is the filter response with no ADC load connected. When the ADC load is connected, the filter response deviates from its designed value, and is shown by the curve labeled as *Filter's Response with ADC Load (No modification in Filter Components)*. After absorbing the ADC input impedance in the last shunt arm of the filter, its response becomes very much similar to its designed value, as shown by the curve labeled *Filter's Response with ADC Load (Last Arm Modified)*.

The last step is to replace the component values used in the filter with the standard values of the capacitors and inductors. A parallel or series combination of standard components can be used to realize the required values. Re-run the ac analysis with TI-TINA and make sure the final frequency response is within the acceptable range of specifications.

## 5 Conclusion

Designing LC filters (that drive a high-speed ADC) without accounting for the ADC input impedance often results in a design that does not meet the target specifications. In this application note, a methodology was described to absorb the ADC input impedance into the filter design. The initial steps in the method make use of existing well-known techniques for filter design with a resistive load. We then described how to modify this filter design to absorb the ADC input impedance.

The final result is a design that meets the original specifications targeted for the filter when used with the ADC. The steps outlined here allow users to come up with a nearly first-pass filter design by minimizing iterations.

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