参考資料

Design Guide: TIDA-060033

ブートストラップ高出力電圧拡張リファレンス・デザイン

概要

このリファレンス・デザインは、3 個の THS3491 高速高電圧電流帰還型アンプを使用して、1MHz で 50Vpp の出力正弦波電圧スイングを実現すると同時に、20Vpp の出力で 100MHz の大信号帯域幅 (BW) を維持します。高出力電圧スイングは、ブートストラップと呼ばれる手法を使用して、出力に対するアンプ電源電圧を変調することで実現されます。この技術は、常に推奨動作条件を維持しながら、アンプの使用可能な電源範囲を効果的に拡張します。

リソース

TIDA-060033	デザイン・フォルダ
THS3491	プロダクト・フォルダ

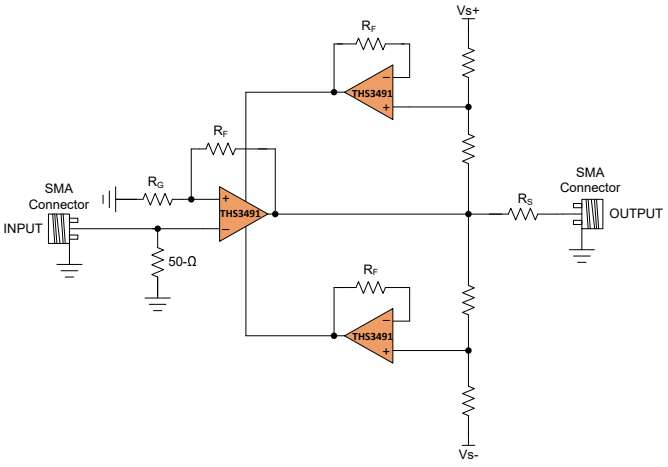
Ask our TI E2E™ support experts

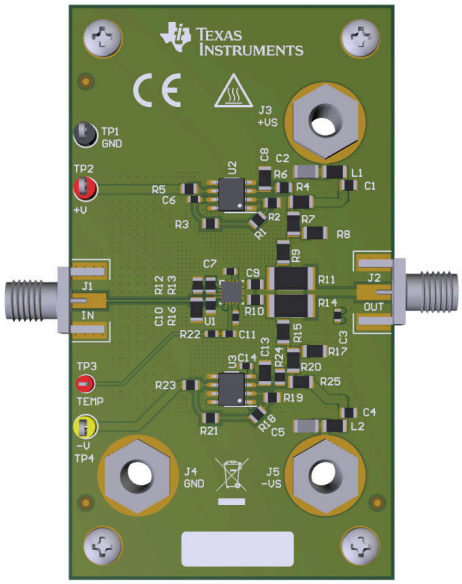
特長

- 高出力電圧スイング 1MHz で 50 V_{pp} 以上
- 最大電源電圧:±32V
- 大きな容量性負荷ドライブ:100pF～1000pF
- 大信号ゲイン BW:20V_{pp} で 100MHz 複数のサブシステムに対応するスケーラブルな小型フォーム・ファクタ

アプリケーション

- 任意波形ジェネレータ (AWG)
- LCD および LED テスタ
- 半導体試験装置
- 実験室およびフィールド用計測機器
- 超音波スキャナ
- LCR メータの電力出力ドライバ
- レーザー距離計





English Document: TIDUEW8

1 System Description

This design guide describes the use of three THS3491 current-feedback amplifiers in a bootstrapped power supply configuration to achieve 50-Vpp output swing capability at 1 MHz with ultra-low harmonic distortion and > 200-mA output current drive capability.

High-frequency and large-signal applications require high slew rate amplifiers for minimal signal distortion. In the case of a large capacitive load, high-output current drive is also desired. These requirements are common in applications such as an LCD and LED tester, arbitrary waveform generator, CCD panel driver, function generator, semiconductor test equipment, lab instrumentation, laser driver, LCR meter power output driver, and so forth.

The THS3491 features a class AB output stage offering low-distortion and high output current, with output headroom requirements of 1.5 V (typical) to each supply. With a maximum supply range of 32 V (±16 V), the THS3491 can drive an output voltage swing up to 29 Vpp in the typical case. This is quite high, yet in the case of an LCD tester for example, it may be desirable to extend the output swing even higher. To achieve this, two additional THS3491 are used in a supply modulation loop to extend the power supply range of the overall circuit up to 64V (±32 V). This approach allows generation of the desired 50 Vpp output pulse that is capable of driving capacitive loads seen in LCD tester applications.

The THS3491 VQFN-16 (RGT) package is chosen for the driver amplifier to attain the best large-signal bandwidth, distortion, and thermal performance possible.

1.1 Key System Specifications

表 1-1 lists key specifications for this design.

表 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Supply voltage	±32 V	See セクション 2.3.1.1
Output load type	100 Ω	See セクション 3.2
	1 nF (Riso = 50 Ω)	
Target bandwidth (BW)	f = 100 MHz at 20 Vpp	See セクション 3.3
	f = 1 MHz at 50 Vpp	See セクション 3.3
HD2, HD3	< –75 dBc at 1 MHz (Vo = 50 Vpp)	See セクション 3.3
Steady-state or quiescent current consumption	About 50 mA for three amplifiers on a ±16-V supply	See the THS3491 data sheet
Maximum operating temperature	Maximum operating temperature dependent upon the internal device power dissipation to limit $T_{J(MAX)}$< 150°C	See セクション 2.3.3
Form factor	85 mm × 48 mm	See セクション 4

2 System Overview

2.1 Schematic Diagram

図 2-1 shows a simplified schematic of the TIDA-060033 high-voltage extension circuit.

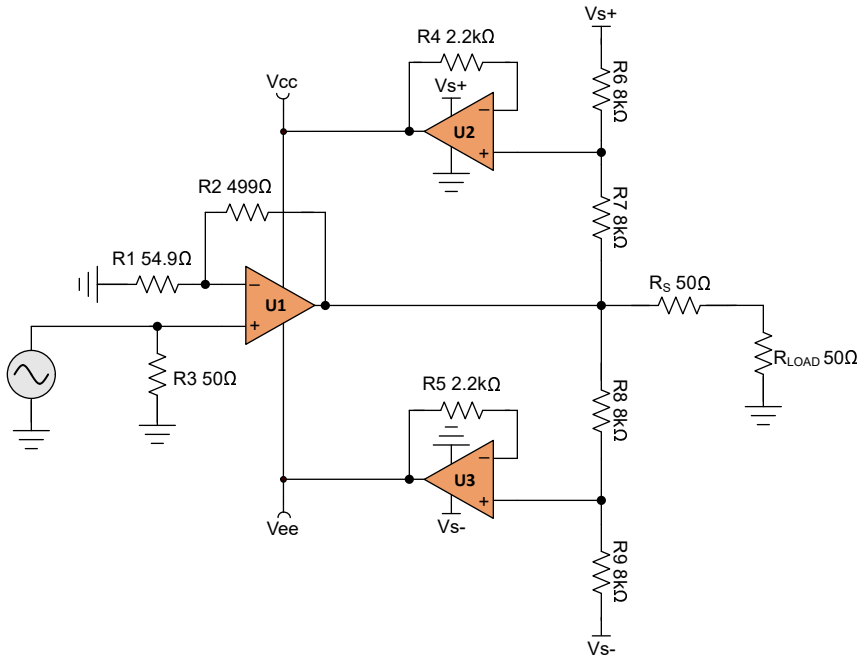


図 2-1. Bootstrapped High-Output Voltage Extension Circuit (Simplified)

2.2 Highlighted Products

2.2.1 THS3491 Current Feedback Amplifier Specifications

- Bandwidth:
  - 900 MHz (V_O = 2 V_{PP}, A_V = 5 V/V)
  - 320 MHz (V_O = 10 V_{PP}, A_V = 5 V/V)
- Slew rate: 8000 V/µs (V_O = 20 V_{PP})
- Input voltage noise: 1.7 nV/√Hz
- Bipolar supply range: ±7 V to ±16 V
- Single supply range: 14 V to 32 V
- Output swing: 28 V_{PP} (±16-V supplies, 100-Ω load)
- Linear output current: ±420 mA (Typical)
- 16.8-mA Trimmed supply current (low temperature coefficient)
- HD2, HD3: Less than –75 dBc (50 MHz, V_O = 10 V_{PP}, 100-Ωload)
- Rise and fall time: 1.3 ns (10-V Step)
- Overshoot: 1.5% (10-V step, A_V = 5 V/V)
- Current limit and thermal shutdown protection
- Power-down feature

2.3 System Design Theory

2.3.1 Theory of Operation

This section discusses the various elements for operating this system design.

2.3.1.1 Concept of Power Supply Range Extension

From the schematic diagram, op amp U1, a THS3491 current feedback amplifier, is the signal path amplifier which will drive up to 50 Vpp output based on the input signal provided by signal source VG1. This amplifier is configured in a non-inverting gain of 10 V/V. This closed-loop gain is established from the simple relationship Av = 1 + (R2 / R1). Of course, 50 Vpp exceeds the THS3491 recommended maximum supply rating of 32 V, as well as the absolute maximum (fault condition) supply rating of 33 V. Note that these ratings apply to the *differential* voltage across the supply pins and not the absolute magnitude relative to ground.

Hence, the role of the other two THS3491 op amps U2 and U3, is to track the output of U1 and shift its supply voltages up and down alongside the output voltage. This technique allows a wider output swing, while keeping the supply rails safe within the recommended *differential* rating at all times.

Vs+ and Vs– are the two main power supplies of the board, and are recommended to operate at +32 V and –32 V, respectively. 図 2-2 shows how THS3491 op amps U2 and U3 are connected to either Vs+ or Vs– and ground in a single-supply configuration. Vcc and Vee are used to designate the bootstrapped power supply pins of the signal amplifier (U1), as these supplies are variable with respect to the output voltage swing.

The output pins of U2 and U3 actively drive the Vcc and Vee supply pins of U1, supplying its quiescent current, as well as the current delivered to its load. U2 and U3 are both connected as voltage followers with a gain of 1 V/V. The input voltages of U2 and U3 are determined by the varying output voltage of U1, resistive voltage dividers R6, R7 and R8, R9, and the supply pins Vs– and Vs+ respectively. The voltage dividers are connected between the main supply pins and the output, such that the inputs to the supply modulating amplifiers (VinU2, VinU3) can be derived from following equations:

$$VinU2 = \frac{1}{2}\left(V_{OUT} + V_{S+}\right) \quad (1)$$

$$VinU3 = \frac{1}{2}\left(V_{OUT} + V_{S-}\right) \quad (2)$$

These same equations are used to determine the U1 supply voltages at any time, as U2 and U3 are configured as non-inverting buffers to drive the power supplies of U1 as shown in 式 3 and 式 4.

$$Vcc = \frac{1}{2}\left(V_{OUT} + V_{S+}\right) \quad (3)$$

$$Vee = \frac{1}{2}\left(V_{OUT} + V_{S-}\right) \quad (4)$$

In practice, the values derived from 式 1 through 式 4 will differ slightly due to the tolerance of resistors making up the voltage divider, and the THS3491 offset voltage. The difference is relatively small as 1% resistors are used and the typical offset voltage is only 1 mV, so for simplicity these errors are not considered. Additionally, The THS3491 has a high power-supply rejection ratio (PSRR) of about 80 dB, which helps minimize output referred voltage offset changes as the supply voltages of U1 follow its output voltage.

図 2-2 shows the DC voltages occurring at various nodes in the design. The Vs+ and Vs– supplies are set to ±32 V respectively, and the input applied to U1 is 0 V, in this case. The output of U1 is nearly 0 V, deviating by the output referred voltage offset (Voso) generated by U1 in a gain of 10 V/V. The difference between the respective Vs+ and Vs– power supplies and the 0-V output, divided by 2 via the resistive dividers, establishes VinU2 as 16 V and Vin U3 as –16 V. From the buffer configuration, the output of U2 is 16 V and the output of U3 is –16 V, a difference of +32 V between them. That is the voltage that appears across the supply pins of U1 (Vcc – Vee).

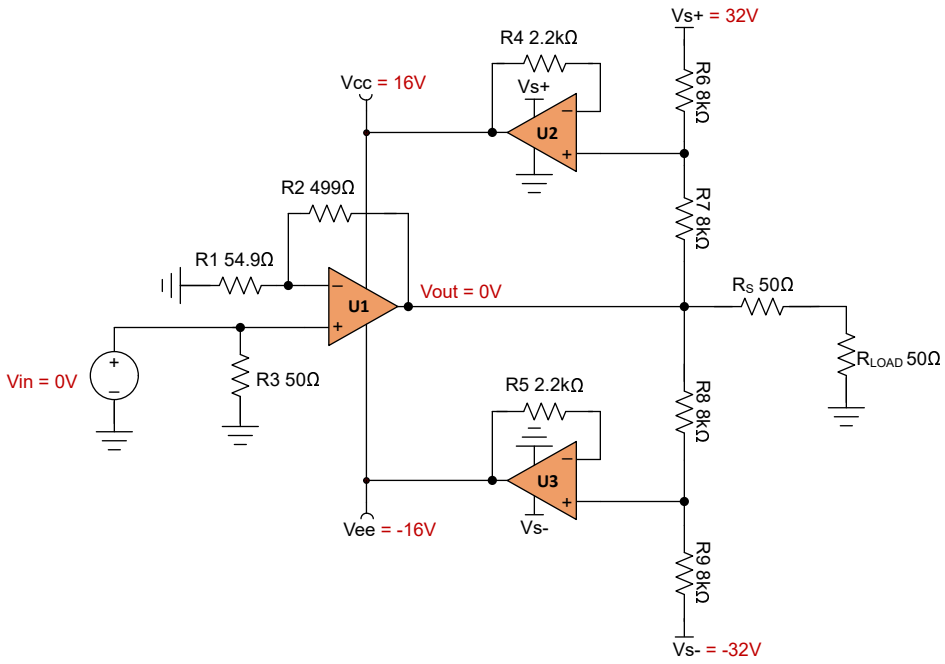


図 2-2. Bootstrapped Power Supply Node Voltages, Vout = 0 V

図 2-3 shows the circuit again with a positive input voltage applied to U1. This corresponds to the circuit behavior during the positive half-cycle of a sinusoid or square wave. In this case, 2 V is applied at the input of U1, resulting in 20 V at the output, due to the gain configuration of +10 V/V. This increases the input voltages of U2 and U3 as defined by 式 1 and 式 2, respectively. Inserting the previoulsy-described values, these equations yield an input of 26 V at U2 and –6 V at U3. Extending these results to 式 3 and 式 4, it is apparent that amplifier U1 is operating with unparallel supply voltages of +26 V and –6 V, as both supplies are shifted upward by exactly half of the increase in output voltage. Note that the differential voltage across the U1 supply pins remains the same at 32 V, which is consistent with the recommended operating conditions in the data sheet.

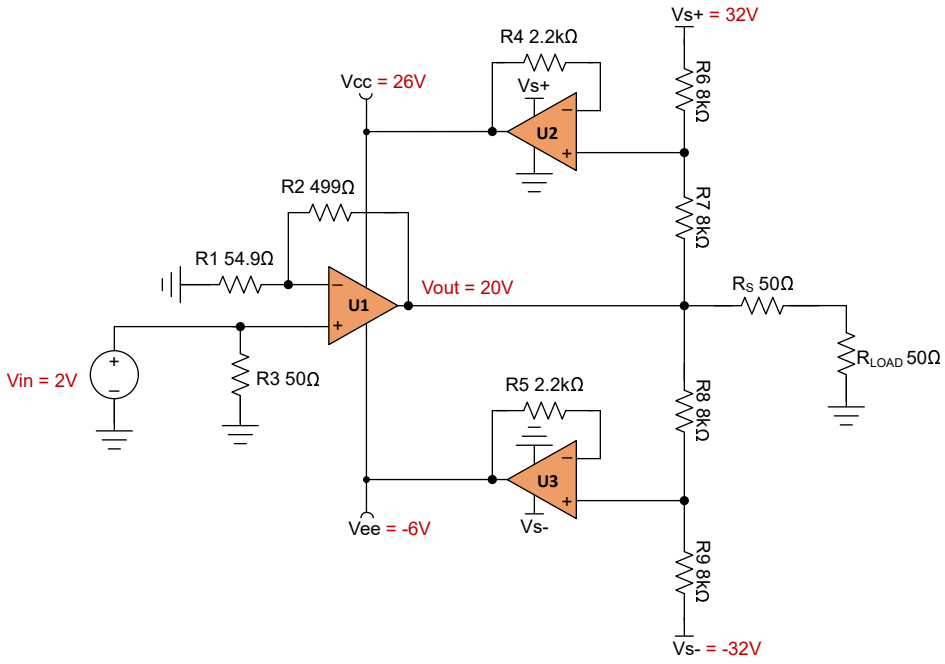


図 2-3. Bootrapped Power Supply Node Voltages, Vout = 20 V

This example is shown again in 図 2-4 with a negative input voltage applied to U1, which corresponds to the negative half-cycle of a sinusoid or square wave. In this case, –2 V is applied at the input of U1, resulting in –20

V at the output. This decreases the input voltages of U2 and U3 as defined by 式 1 and 式 2, resulting in an input of 6 V at U2 and –26 V at U3. Extending these results to 式 3 and 式 4, now amplifier U1 is operating with unparallel supply voltages of +6 V and –26 V, as both supplies are shifted down by exactly half of the decrease in output voltage. As in the previous case, the differential voltage across the U1 supply pins remains a consistent 32 V.

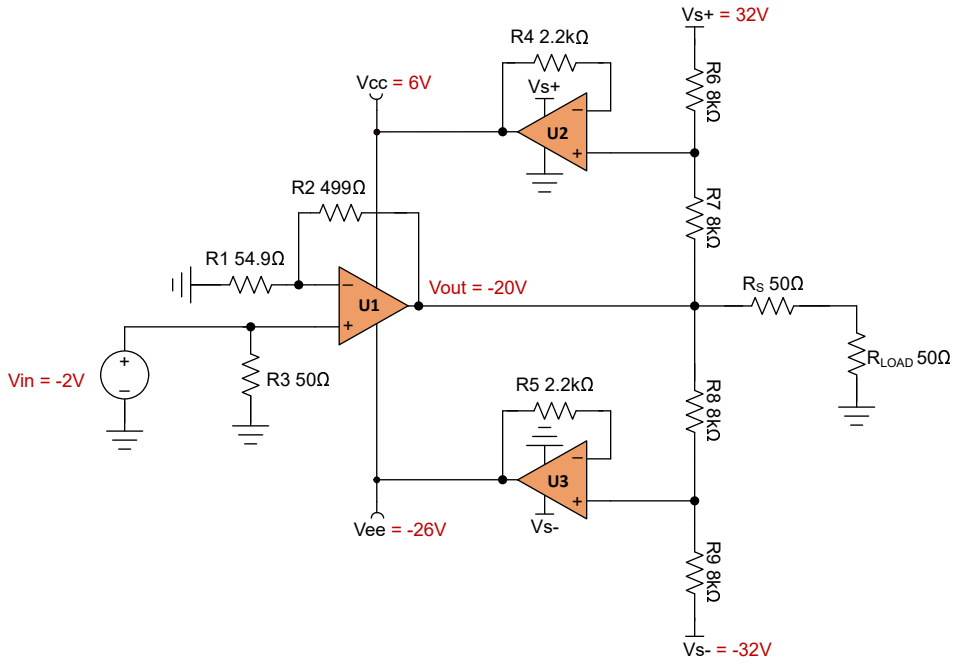


図 2-4. Bootstrapped Power Supply Node Voltages, Vout = –20 V

図 2-5 shows the voltage swing for the output and power supply nodes across the common-mode input range of the circuit. The maximum voltage output swing is defined by the input common mode headroom of the supply modulating amplifiers, and the output voltage headroom of the driver amplifier. In theory, this design could produce a reliable output as high as 52-Vpp over process, however this document will focus on 50-Vpp output as this is the design target (表 1-1).

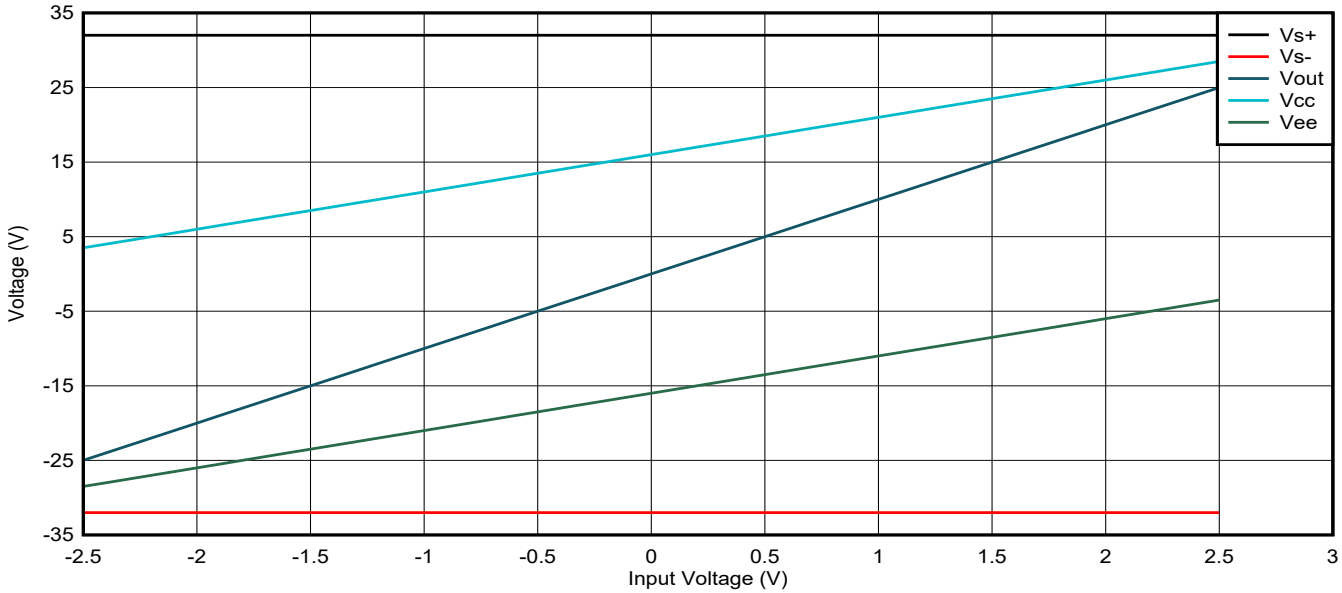


図 2-5. Bootstrapped Power Supply Node Voltages Over Common-Mode Input Range

図 2-6 presents this data again in the time domain with a 1-MHz sinusoidal output. This data was generated with the TINASpice simulation tool and shows how supply rails Vcc and Vee track around the output voltage swing.

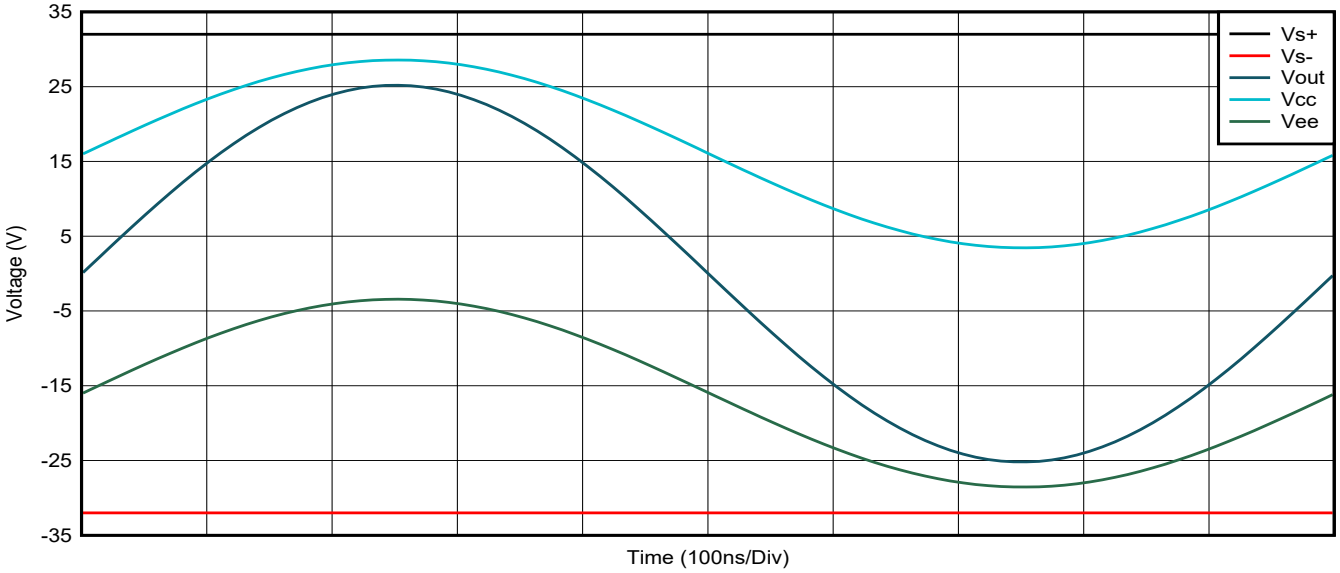


図 2-6. Bootstrapped Power Supply Node Voltages, Sinusoidal Output Swing

2.3.2 Stability Considerations

2.3.2.1 Inclusion of Series Isolation Resistance (R_S)

For an amplifier directly driving a capacitive load, the amplifier is prone to oscillations as a result of the additional phase shift introduced in the loop-gain expression by the amplifier open-loop output impedance and the capacitive load. For a current-feedback amplifier such as the THS3491, the open-loop output impedance and the capacitive load introduce a pole in the open-loop transimpedance gain response. If the pole is at a frequency lower than the non-dominant pole of the amplifier, then the transimpedance loop-gain is reduced and the phase margin is reduced. To counteract the effect of this pole, a series isolation resistor (R_S) is used between the device output and the capacitive load that introduces a zero in the response. TI recommends placing R_S close to the device output to avoid the printed circuit board (PCB) trace parasitic affecting the frequency response of the amplifier.

Depending upon the capacitive load, and as shown in 図 2-7, R_S must be adjusted for a flat frequency response. The inclusion of R_S can result in an increased voltage drop across the series resistor at higher output currents and limits the available output voltage swing at the capacitive load. However, when selecting the series isolation resistance, stability must be of greater concern than output voltage drop.

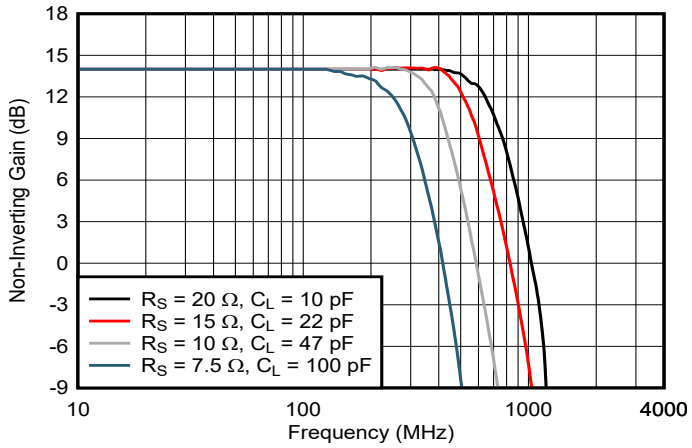


図 2-7. Flat Frequency Response Using Different R_S for a Given C_L (Single THS3491)

2.3.3 Power Dissipation

The THS3491 is designed for high-speed, high-output-power applications that require paying special attention to the thermal considerations when designing the PCB. The amplifier includes automatic thermal shutdown protection circuitry that shuts down the device when the internal junction temperature (T_J) exceeds approximately 160°C, and turns on the device when the device cools down to approximately 145°C. When delivering high output power into capacitive loads, the internal junction temperature (T_J) can exceed the 160°C limit because of internal power dissipation, resulting in thermal shutdown of the device. The occasional $T_{J(MAX)}$ operation of 160°C is allowed. However, for long-term reliability of the device, TI recommends keeping the maximum internal device junction temperature (T_J) below 150°C. Any increase in the device junction temperature is the result of an increased internal power dissipation for a given ambient temperature (T_A). As a result, the internal power dissipation must be limited to prevent the amplifier from continuously running into thermal shutdown.

The following subsections discuss internal amplifier power dissipation (both DC and AC) for a purely resistive output load, as well as the average power dissipation for a simple resistive-capacitive (RC) output load. It is important note that this analysis is not equivalent to the total power drawn from the supplies, but instead is used to determine the linear safe operating area (SOA) of the system.

2.3.3.1 DC Internal Power Dissipation of Driver Amplifier for a Purely Resistive Output Load

The internal power dissipation of an amplifier consists of two parts: the quiescent power that biases internal op-amp circuitry independent of loading, and the power dissipated in the output transistors when the op amp is loaded. For a high output power amplifier such as THS3491, the majority of power dissipation, and therefore temperature rise, occurs in the output transistors of the device.

The quiescent power dissipation (P_Q) shown in 式 5 is the internal amplifier power dissipation when the amplifier output is open, or when there is no current drive in or out of the amplifier.

$$P_Q(W) = (Vcc - Vee) \times I_Q \tag{5}$$

where:

- Vcc = The potential at the positive power supply terminal
- Vee = The potential at the negative power supply terminal
- I_Q = The total quiescent current drawn from the power supply of the device

From 図 2-5, it is apparent that although Vcc and Vee are variable for the driver amplifier (U1), the potential across the supply rails (Vcc – Vee) is constant and equal to the supply potential of amplifiers U2 and U3. Considering that (Vcc – Vee) = Vs+ = –Vs– = Vs , 式 5 is written as 式 6.

$$P_Q(W) = V_S I_Q \tag{6}$$

The THS3491 has a class AB output stage as shown in 図 2-8, in which only one of the output transistors is turned on for high or low output voltage depending upon the source or sink current. For a ground-referenced load, the amplifier sources current for positive output voltages, and sinks current for negative output voltages. 式 7 shows the DC power dissipated in the output transistors ($P_{OUT(DC)}$), for a load (R_L) referenced to ground, when the amplifier is *sourcing* current. This is the voltage drop across the sourcing (NPN) output transistor (V_{cc} – V_{OUT}) multiplied by the output current drive (I_{OUT}).

$$P_{Source(DC)}(W) = (Vcc - V_{OUT}) \times I_{OUT} = (Vcc - V_{OUT})\frac{V_{OUT}}{R_L} \tag{7}$$

where:

- V_{OUT} = Output voltage of the amplifier
- I_{OUT} = Output current drive of the amplifier
- R_L = Total Resistive load at the output of the amplifier. In 図 2-1, R_L is equal to the combination of the series output resistor (R_S) and the load resistor (R_{LOAD}).

式 8 shows the DC power dissipation in the output transistors when the amplifier is *sinking* current for a ground-referenced load. This is similar to 式 7, except that the voltage drop across the *sinking* (PNP) output transistor is considered.

$$P_{Sink(DC)}(W) = (Vee - V_{OUT}) \times I_{OUT} = (Vee - V_{OUT})\frac{V_{OUT}}{R_L} \quad (8)$$

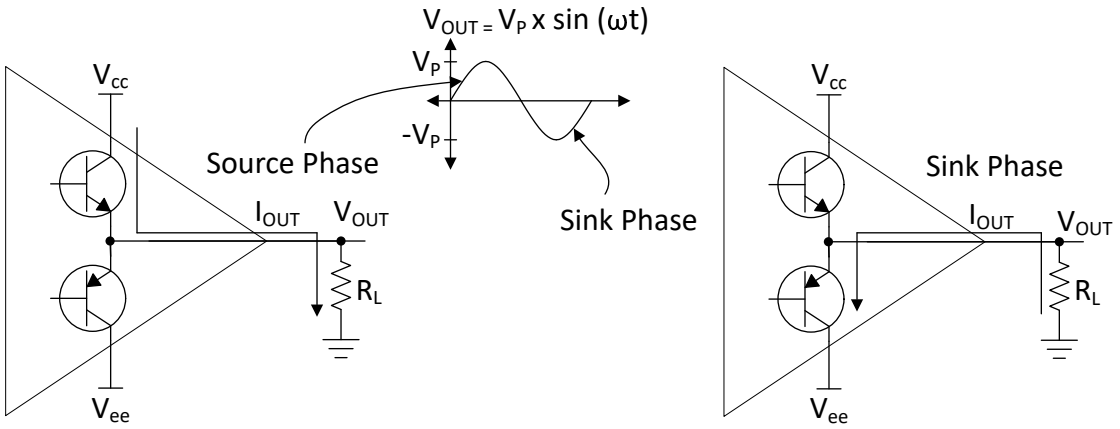


図 2-8. THS3491 Class AB Output Structure

The combination of 式 6 with 式 7 and 式 8 produces 式 9 and 式 10, the total internal DC power dissipation of a single amplifier when sourcing and sinking current, respectively.

$$P_{AmpSource(DC)}(W) = V_S I_Q + (Vcc - V_{OUT})\frac{V_{OUT}}{R_L} \quad (9)$$

$$P_{AmpSink(DC)}(W) = V_S I_Q + (Vee - V_{OUT})\frac{V_{OUT}}{R_L} \quad (10)$$

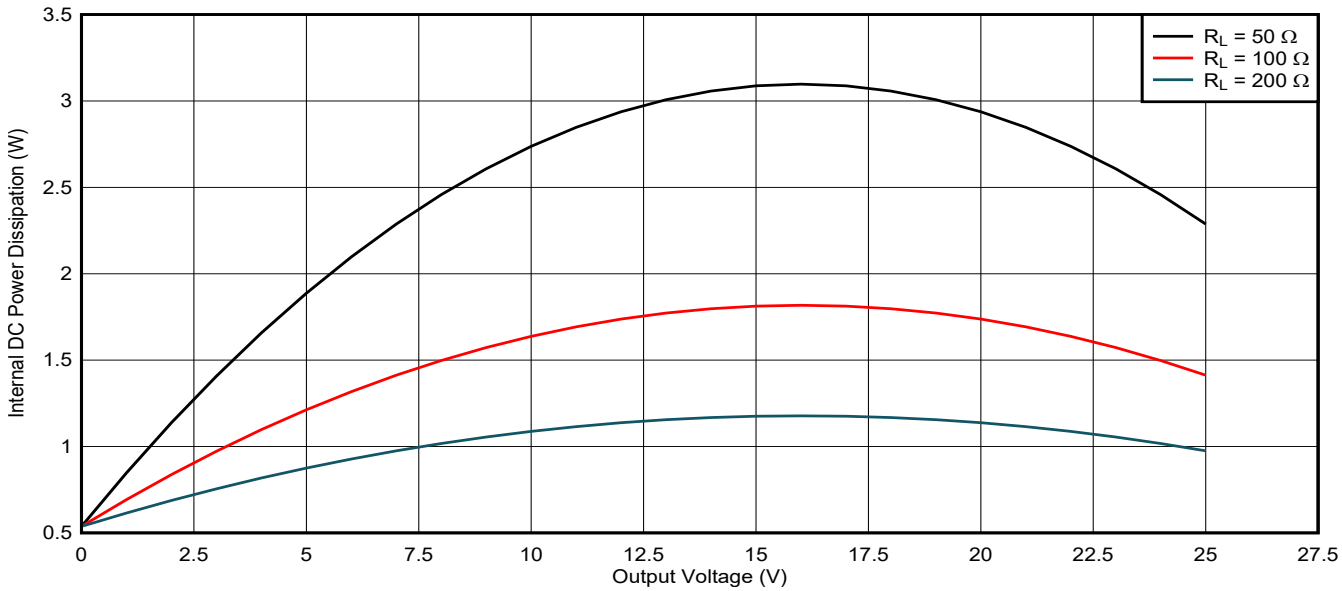


図 2-9. Internal DC Power Dissipation of Driver Amplifier

2.3.3.2 AC Average Internal Power Dissipation of Driver Amplifier for a Purely Resistive Output Load

For a continuous sinusoidal output driving a purely resistive load referenced to ground, the internal average power dissipated ($P_{OUT(AVG)}$) in the output transistors of an amplifier can be calculated by integrating the sinusoid for half a cycle and taking the average. 式 11 uses the positive half-cycle to describe the internal

average power dissipation of the driver amplifier when driving a continuous sinusoidal output into a purely resistive ground-referenced load.

$$P_{OUT(AVG)}(W) = \frac{1}{\pi}\int_0^{\pi}(Vcc - V_{OUT})\frac{V_{OUT}}{R_L}\,dwt \quad (11)$$

As V_{OUT} is sinusoidal in this case, it can be defined by 式 12.

$$V_{OUT} = V_P \times Sin(wt) \quad (12)$$

where

- Vp = Peak output voltage swing

In a typical power calculation, the output voltage is the only variable term in the integration, and the remainder of the terms are constant. For the driver amplifier in this design, Vcc is also variable, but because the power supplies are bootstrapped to the output voltage, Vcc can be written simply in terms of the output voltage as in 式 3. Combining 式 11, 式 12, and 式 3, integrating across the positive half-cycle (0 to π), and dividing by π for averaging, results in 式 13.

$$P_{OUT(AVG)}(W) = \frac{V_P V_S}{\pi R_L} - \frac{{V_P}^2}{4R_L} \quad (13)$$

Including the quiescent power consumption defined in 式 6 with 式 13 produces the total average power dissipation for a single amplifier driving a sinusoid into a purely resistive load, 式 14.

$$V_S I_Q + \frac{V_P V_S}{\pi R_L} - \frac{{V_P}^2}{4R_L} \quad (14)$$

図 2-10 shows the internal average power dissipation as a function of the peak output voltage (Vp) for various load resistances (R_L). The maximum internal average power dissipation occurs when Vp = 2 Vs/π resulting in 式 15.

$$P_{Amp(AVG)}(W)(max) = V_S I_Q + \frac{V_S^2}{\pi^2 R_L} \quad (15)$$

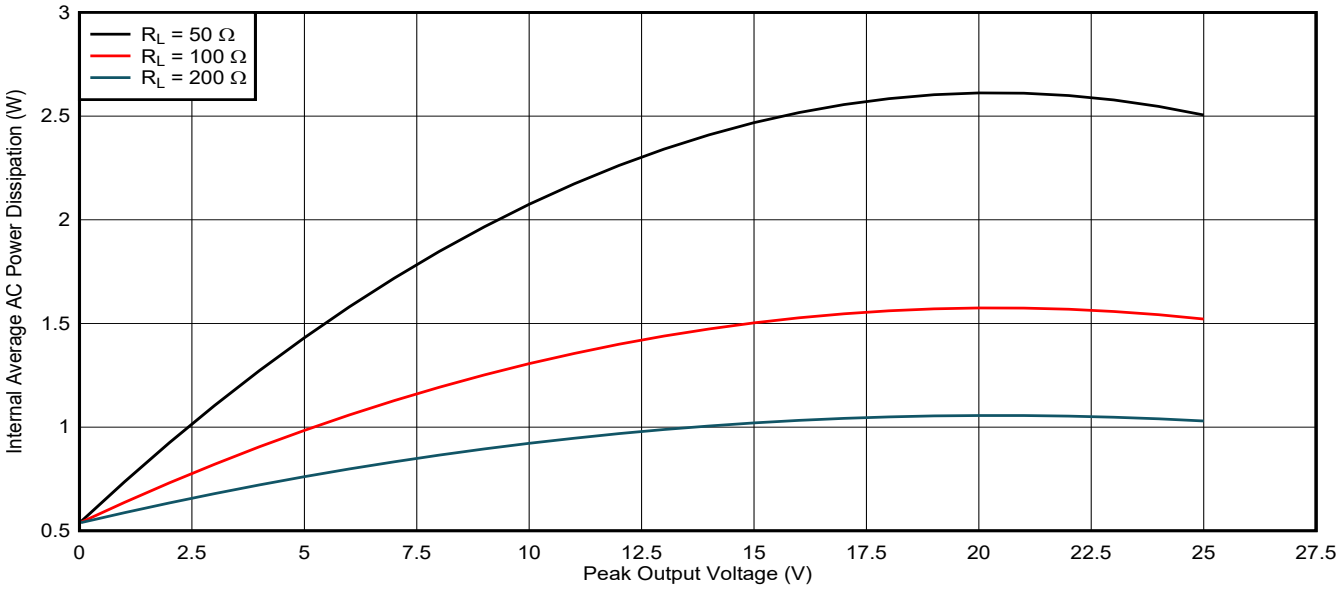


図 2-10. Average Internal AC Power Dissipation of Driver Amplifier

2.3.3.3 Internal Average Power Dissipation of Driver Amplifier for RC Output Load

For a continuous sinusoidal output driving an RC load, the internal average power dissipation ($P_{OUT(AVG)}$) in the output transistors can be calculated as 式 16 shows by subtracting the average power delivered to the load from the average power provided by the supply.

$$P_{OUT(AVG)}(W) = P_{Supply(AC)} - P_{Load(AC)} \tag{16}$$

where

- $P_{SUPPLY(AVG)}$ = Average input power from the supply while driving the RC load
- $P_{LOAD(AVG)}$ = Average output power delivered to the RC load

図 2-11 shows the output structure for an RC load, and 式 17 gives the total reactive load (Z_L).

$$Z_L = R_S + jX_C \tag{17}$$

where

$$X_C = -j\frac{1}{2\pi f C_L} \tag{18}$$

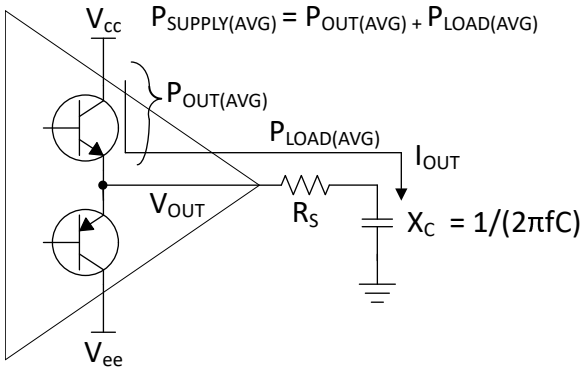


図 2-11. Output Structure for an RC Load (Source Phase)

式 19 shows the average power that the driver amplifier will draw from the power supplies when driving a continuous sinusoidal signal into an RC load referenced to ground. Similar to 式 11, the power is integrated across the positive half-cycle and averaged.

$$P_{Supply(AVG)}(W) = \frac{1}{\pi}\int_0^{\pi}\frac{1}{|Z_L|}Vcc \times V_P \times Sin(wt) \times dwt = \frac{2V_P V_S}{\pi|Z_L|} \tag{19}$$

where

$$|Z_L| = \sqrt{|R_S|^2 + |X_C|^2} \tag{20}$$

式 21 shows the average output power delivered to the RC load. Cos(φ) is the power factor and gives the phase difference between the output voltage and output load current. The power factor corrects for the phase relationship between the voltage and current for the average output power calculation in an RC load. For a purely resistive load, the power factor equals 1 indicating no phase difference between the voltage and currents.

$$P_{Load(AC)}(W) = \frac{1}{2|Z_L|}{V_P}^2 \times Cos(\phi) = \frac{R_S}{2|Z_L|^2}{V_P}^2 \tag{21}$$

where

$Cos(\phi) = \frac{R_S}{|Z_L|}$ and represents the power factor of the circuit. (22)

As a result, 式 23 shows the internal average power dissipation in the output transistors for a single amplifier driving an RC load with a sinusoidal output.

$$P_{OUT(AVG)}(W) = \frac{2V_P V_S}{\pi |Z_L|} - \frac{R_S}{2|Z_L|^2} {V_P}^2 \quad (23)$$

By accounting for the quiescent power dissipation, 式 24 shows the total internal average power dissipation for a single amplifier driving an RC load.

$$P_{AMP(AVG)}(W) = V_S I_Q + \frac{2V_P V_S}{\pi |Z_L|} - \frac{R_S}{2|Z_L|^2} {V_P}^2 \quad (24)$$

2.3.4 Thermal Performance

The device package and the PCB material are responsible for thermal performance and conduction of heat out of the device die. The internal power dissipation of the device increases the internal die junction temperature, and the topic is extensively discussed in セクション 2.3.3.

For an RGT package with an exposed thermal pad, the heat sink at the PCB bottom plane allows the least resistive path for heat transfer, and the majority of thermal energy is dissipated through the thermal pad to the heat sink. Because of the higher thermal handling capability, the inclusion of a heat sink at the bottom of the device allows for higher internal device power dissipation and subsequently allows for driving higher output current from the device.

For a heat sink design, 図 2-12 shows the various sources of thermal resistances. Because power dissipation causes a rise in junction temperature that is similar to the voltage drop across a resistor resulting from current flow, a simplified thermal model (see 図 2-13) can be developed that is analogous to an electrical circuit. The temperature, power dissipation, and thermal resistance are represented as voltage, current, and resistors, respectively. These parameters, as described in 式 25, allow the maximum internal power dissipation to be solved for by using a simple KCL equation.

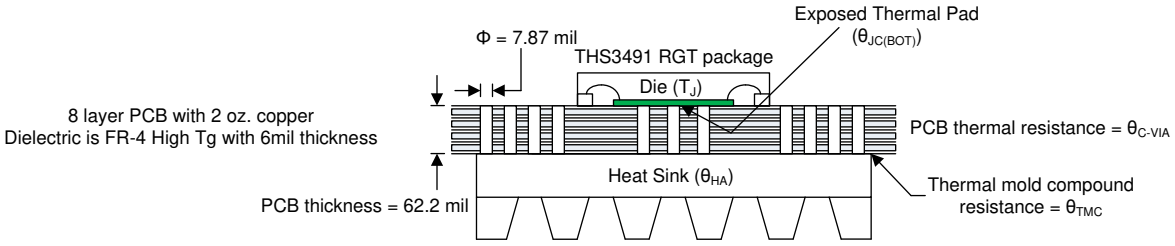


図 2-12. TIDA-060033 PCB Cross Section of Different Thermal Resistances

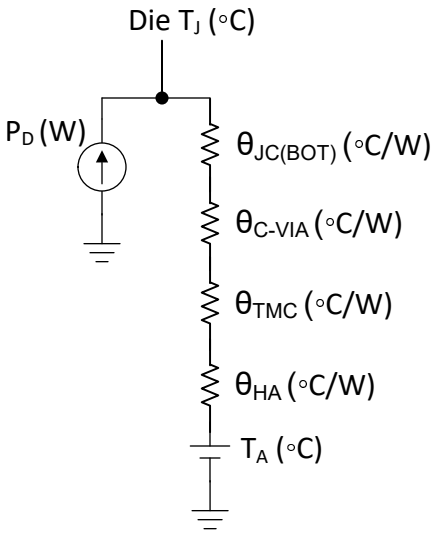


図 2-13. Simplified Thermal Model for Heat Sink Design

$$P_{AMP}(W)(max) = \frac{\left(T_{J(max)} - T_A\right)}{\left(\theta_{JC(BOT)} + \theta_{C-VIA} + \theta_{TMC} + \theta_{HA}\right)} \quad (25)$$

where:

- $P_{D(MAX)}$ (W) = Maximum internal power dissipation of the amplifier
- $T_{J(MAX)}$ (°C) = Absolute maximum junction temperature
- T_A (°C) = Free-air operating ambient temperature
- $\theta_{JC(BOT)}$ (°C/W) = Bottom junction-to-case thermal resistance of the device package from the data sheet
- θ_{C-VIA} (°C/W) = Case to via thermal resistance
- θ_{TMC} (°C/W) = Thermal mold compound resistance between the PCB and heat sink
- θ_{HA} (°C/W) = Heat sink to ambient thermal resistance

To calculate the maximum power dissipation allowed for a heat-sink design, each of the individual thermal resistance parameters in 式 25 must be known. For the TIDA-060033 EVM, an estimate can be made of the thermal resistances that should hold true for most practical applications:

1. The bottom junction-to-case thermal resistance ($\theta_{JC(BOT)}$) is usually provided in the device data sheet. For the THS3491RGT package, this value is 7.8°C/W.
2. The PCB thermal resistance is the thermal resistance of the flooded vias (θ_{C-VIA}), and is estimated from the via pad diameter, the via height, and PCB material of the via. The EVM has two ounces of copper on each layer with a via diameter of 7.87 mil and a PCB thickness of 62.2 mil that results in a single via thermal resistance of 180°C/W. This thermal resistance estimation is based on the Saturn PCB toolkit for an FR-4 dielectric. The PCB is flooded with 80 vias in and around the bottom of the device, which results in an effective θ_{C-VIA} of approximately 3°C/W to 3.5°C/W. For a more accurate PCB thermal resistance estimation, finite element software tools can be used from vendors such as ANSYS or Keysight for thermal modeling of the PCB.
3. The thermal resistance of the heat-sink adhesive or the thermal-mold compound (θ_{TMC}) is approximately 0.3°C/W to 0.5°C/W for a maximum heat transfer from the PCB to the heat sink.
4. BDN14-3CB/A01 is the heat sink selected for this design. The BDN14-3CB/A01 has a natural convection free-air standing thermal resistance of θ_{HA} at approximately 16.2°C/W.

Plugging in these individual estimated thermal resistances into 式 25 results in a combined thermal resistance of 27.5°C/W. For a maximum T_J of 150°C and a free-air operating ambient temperature (T_A) of 25°C, the resulting maximum internal power dissipation allowed is 4.54 W with the BDN14-3CB/A01 heat sink applied.

Considering 式 24, driving a 1-MHz, 50-Vpp sinusoidal output into a 1-nF capacitive load with 50 Ω of isolation resistance, will result in 3.1 W of average internal power dissipation in the driver amplifier. Comparing this to the

previous result proves that the heat sink chosen is thermally sufficient for these output conditions at room temperature. Further analysis of the safe operating area is discussed in セクション 2.3.4.1.

2.3.4.1 Linear Safe Operating Area (SOA)

To be within a linear safe operating area, an amplifier is required to either limit the maximum linear output current drive or the maximum internal power dissipation ($P_{D(MAX)}$) to prevent the device from exceeding the maximum junction temperature ($T_{J(MAX)}$) of 150°C. This limit is usually represented by a linear safe operating area (SOA) graph that defines the operational boundary by plotting the linear output current drive (I_{OUT}) on the y-axis and the voltage developed across the output transistor ($V_{cc} – V_{OUT}$) on the x-axis.

As 図 2-14 shows, the upper bound of the safe operating area is defined by the maximum linear output current drive of the amplifier (420 mA) starting from the left of the x-axis. When the voltage developed across the output transistor ($V_{cc} – V_{OUT}$) increases towards the right of the x-axis, the linear output current reduces to maintain a fixed internal power dissipation across the output transistors. The fixed internal power dissipation depends on the heat sink used, and is derived by 式 25 to keep the $T_{J(MAX)}$ below 150°C for a given ambient temperature (T_A). The linear output current is derived from 式 26 by sweeping ($V_{cc} – V_{OUT}$) from right to left on the x-axis until the I_{OUT} equals the maximum linear output current drive of 420 mA. The ($V_{cc} – V_{OUT}$) on the x-axis is equally applicable for ($V_{ee} – V_{OUT}$), depending upon the output source or sink current cycle for a sinusoidal signal (see 図 2-8).

$$I_{OUT(MAX)} = \frac{P_{D(MAX)} - V_S I_Q}{Vcc - V_{OUT}} \quad (26)$$

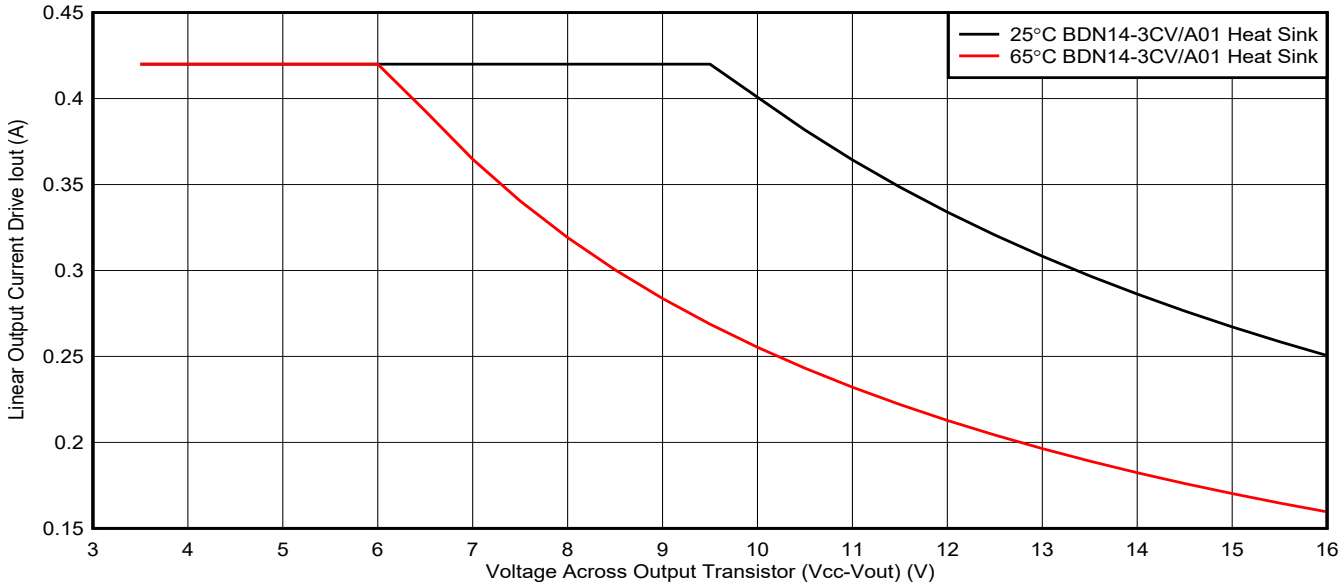


図 2-14. TIDA-060033 Linear Safe Operating Area

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

This reference design uses the design PCB for the measurements in セクション 3.3 to describe the required hardware set up for the frequency response, harmonic distortion, and pulse response measurements, respectively. For frequency response and harmonic distortion tests, a THS3491EVM configured in a gain of 5 V/V was used as a preamplifier stage.

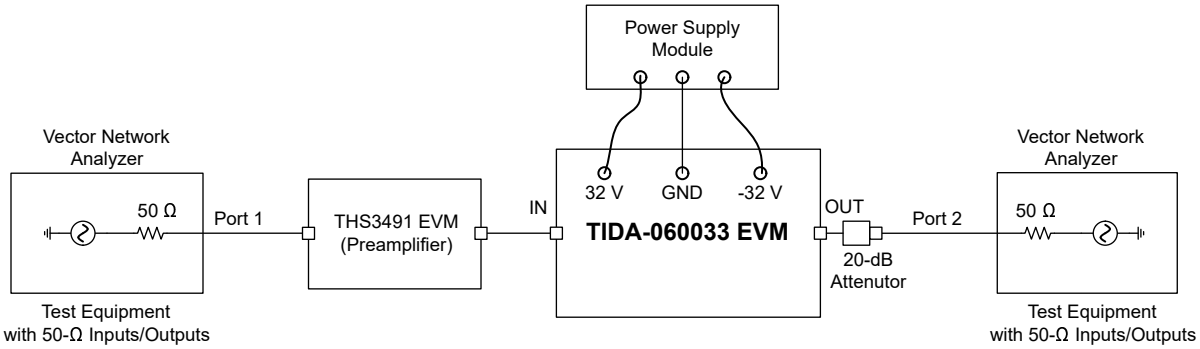


図 3-1. Frequency Response Setup

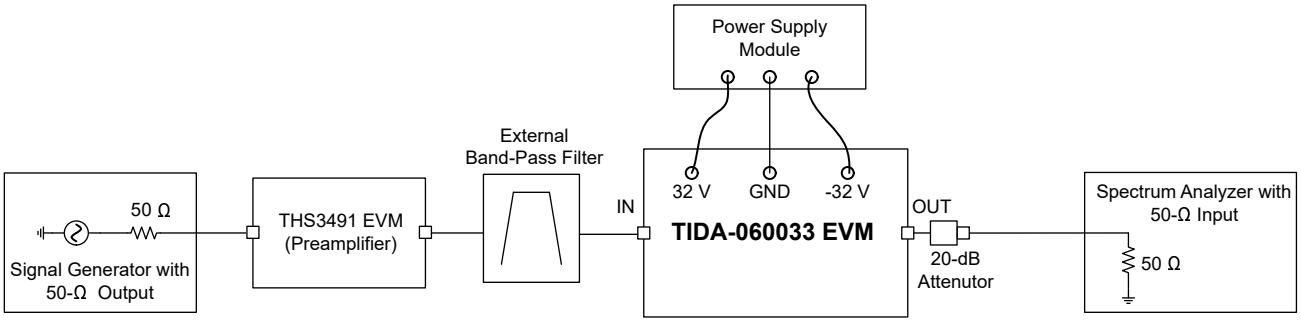


図 3-2. Harmonic Distortion Setup

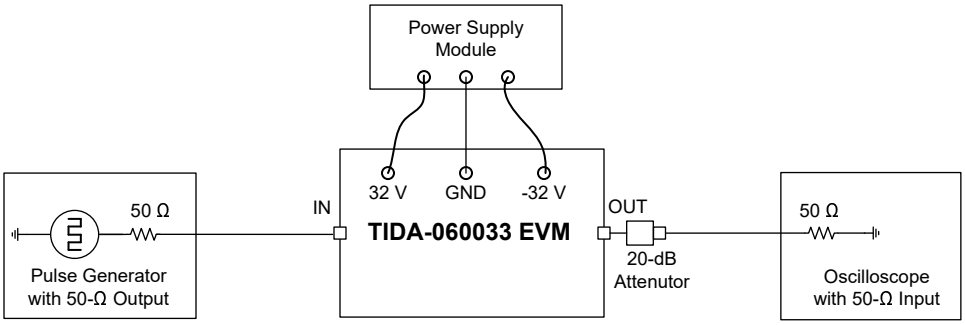


図 3-3. Pulse Response Setup

3.2 Test Setup

図 3-4 illustrates the test set up for the TIDA-060033EVM driving a resistive load. The setup is configured for simple interfacing with 50-Ω test equipment, with a high-power 20-dB, 50-Ω matched attenuator at the output.

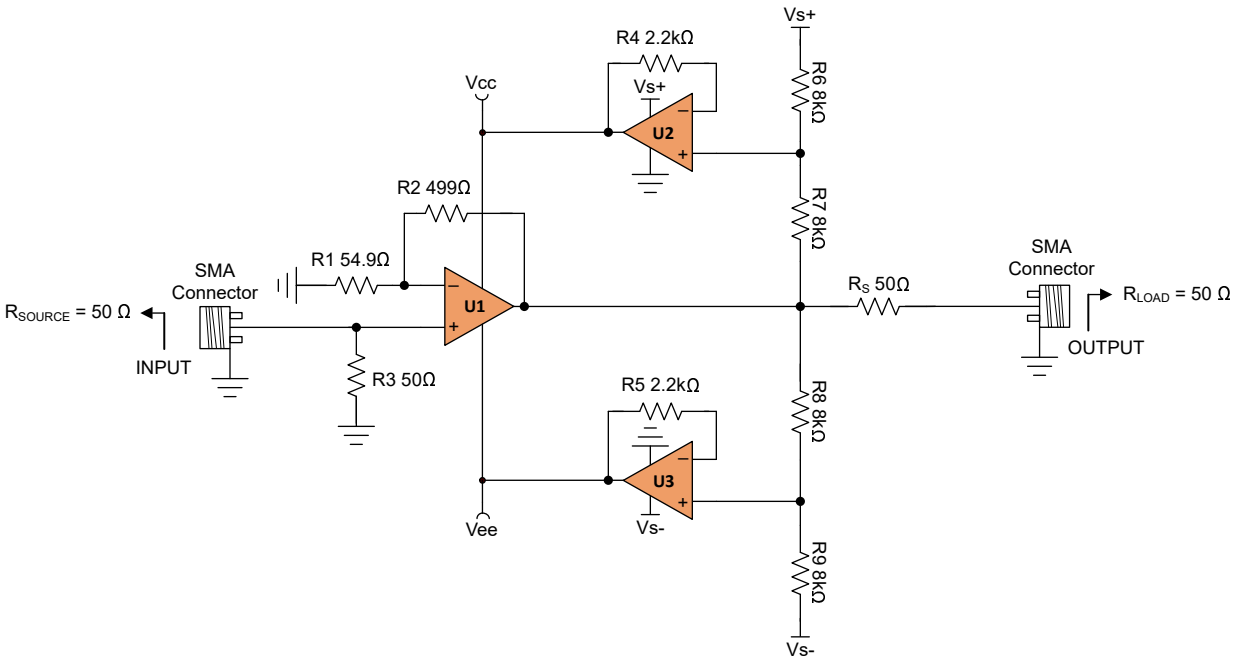


図 3-4. TIDA-060033 Resistive Load Schematic (Simplified)

図 3-5 illustrates the test setup for the TIDA-060033 EVM driving a capacitive load. For stability considerations, a 50-Ω series resistor (R_S) is positioned between the output of the driver amplifier and the 1-nF capacitive load (C_L), as discussed in セクション 2.3.2.1.

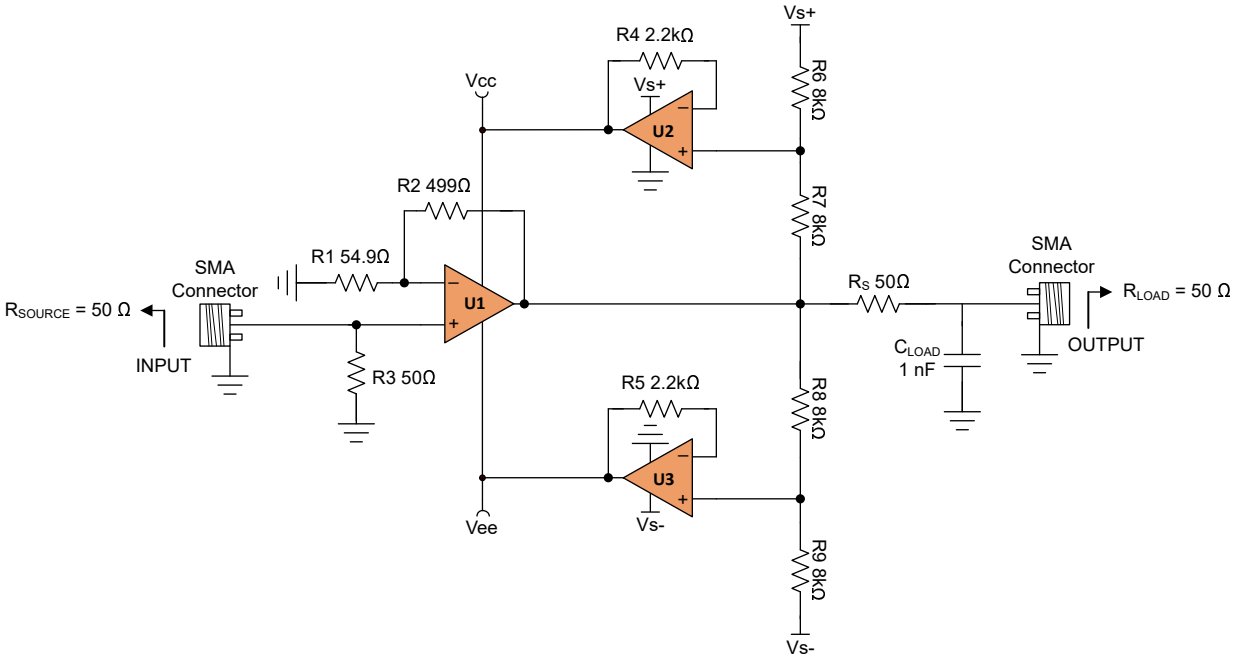


図 3-5. TIDA-060033 RC Load Schematic (Simplified)

3.3 Test Results

The images in 図 3-6 through 図 3-11 were generated using the following parameters.

- **Test Conditions:** Vs+ = 32 V, Vs– = –32 V, T_A = 25°C, R_L = 100 Ω.

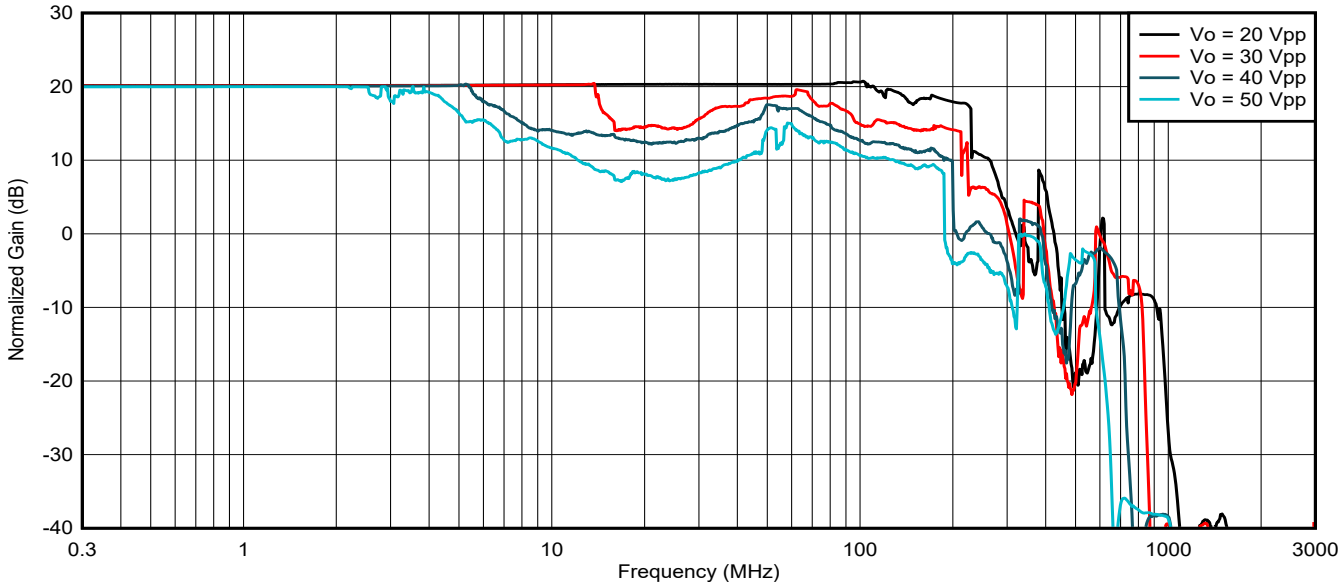


図 3-6. Frequency Response

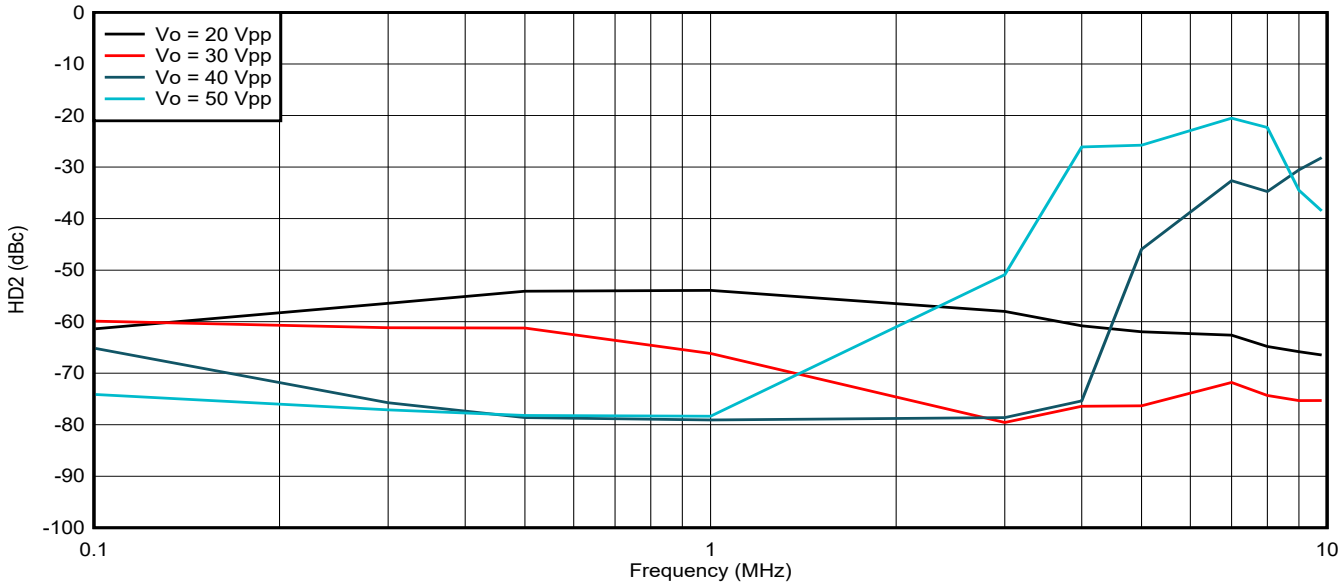


図 3-7. HD2 vs Frequency

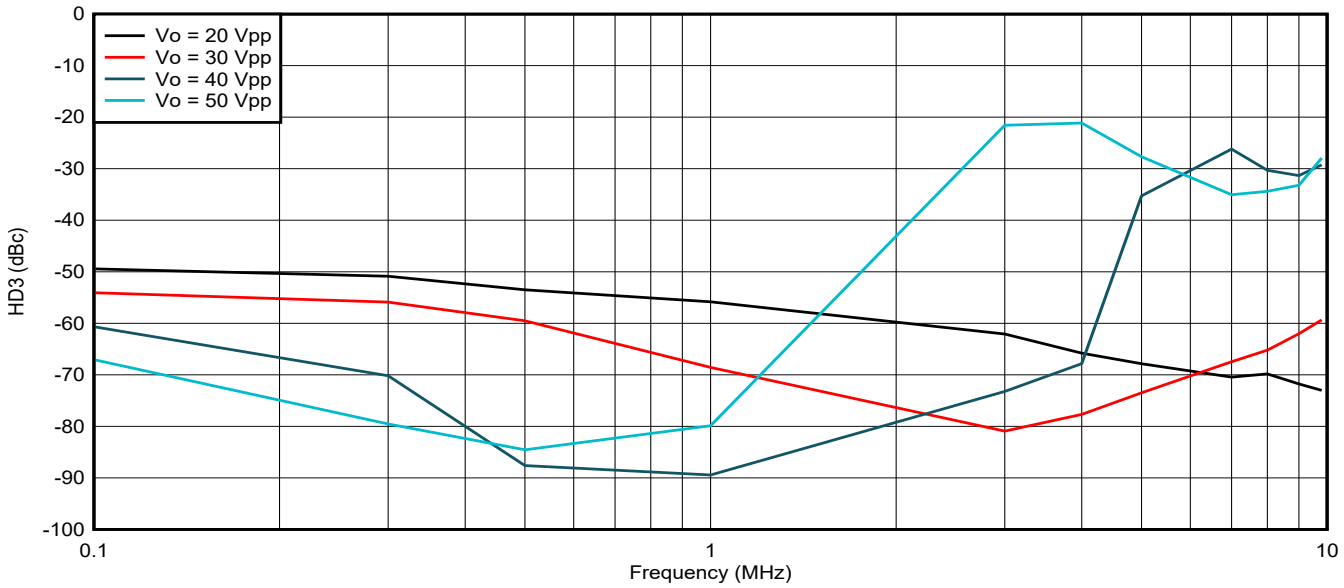


図 3-8. HD3 vs Frequency

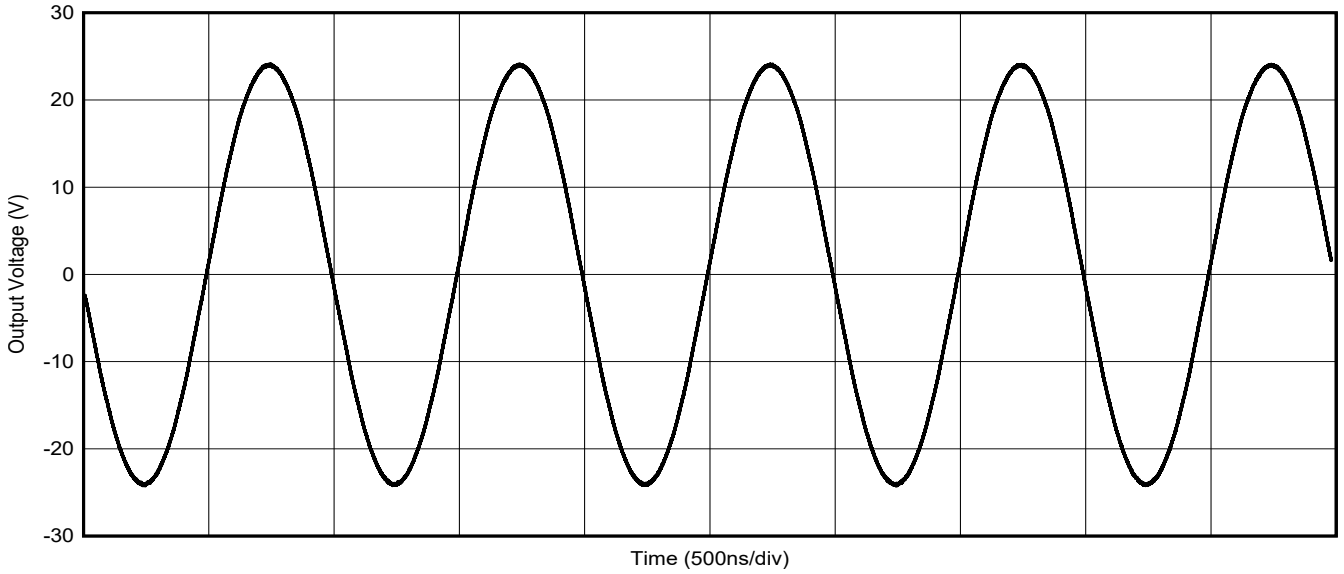


図 3-9. 50-Vpp Sinusoidal Output Swing at 1 MHz

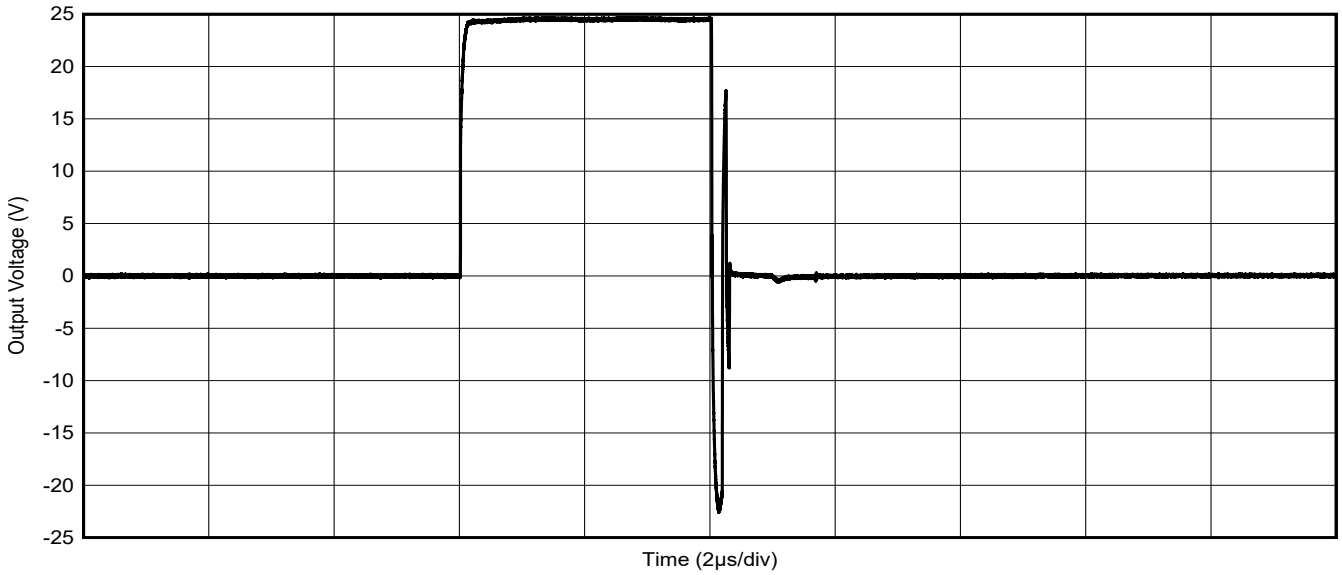


図 3-10. Pulse Response

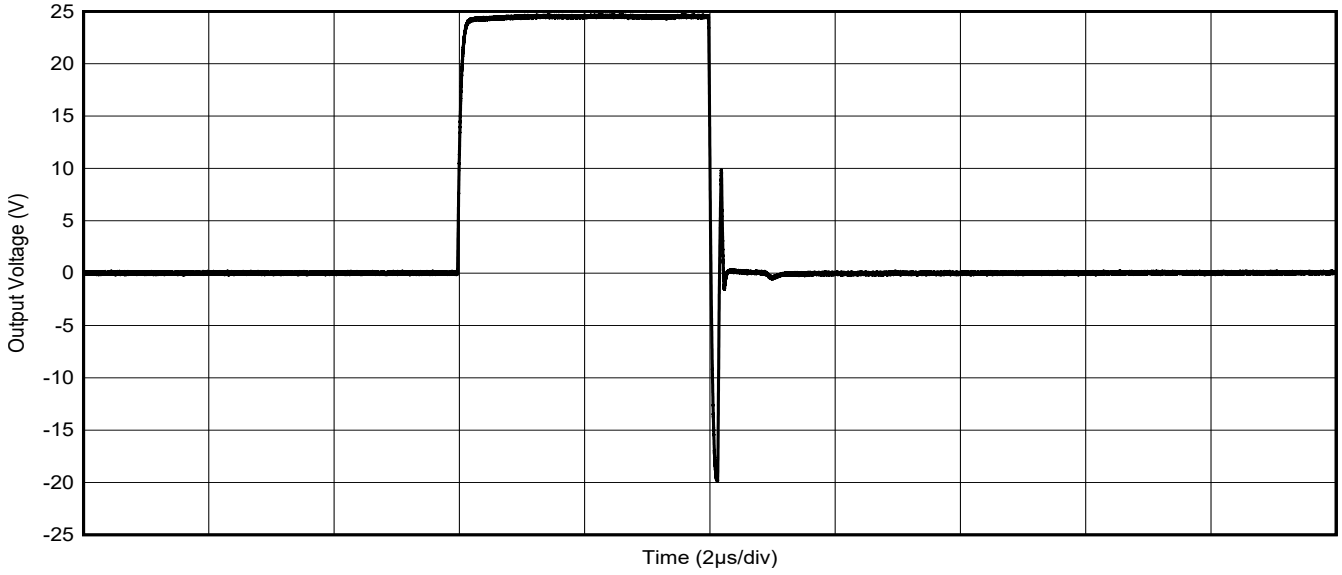


図 3-11. Pulse Response Capacitive Load (C_{LOAD} = 1 nF, R_S = 50 Ω)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-060033.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060033.

4.3 PCB Layout Recommendations

The PCB layout recommendations are similar to the layout guidelines provided in the THS3491 data sheet. The thermal performance for the design is provided in セクション 2.3.4.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-060002.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-060033.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-060033.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060033.

5 Related Documentation

1. Texas Instruments, *THS3491 900-MHz, 500-mA High-Power Output Current Feedback Amplifier* data sheet
2. Texas Instruments, *100-MHz, 1 A Output current driver reference design for high capacitive load applications*
3. Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

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