参考資料

デザイン・ガイド: TIDA-050030
120W デュアルステージ、マトリクス互換、車載ヘッドライト ECU のリファレンス・デザイン

概要

このリファレンス・デザインでは、電圧レギュレーション・モードのインターリーブ昇圧を使用して 4 つの同期整流降圧チャネルに給電する、ヘッドライト ECU について詳しく説明します。このリファレンス・デザインは、マトリクス・ヘッドライトを制御することもでき、車載用ヘッドライトの ECU をエミュレートするためにヒートシンクに取り付けられケースに納められています。

TPS92682-Q1 は、130W の電力を出力できる電圧レギュレーション・モードに設定された 2 相インターリーブ昇圧コントローラとして構成されています。この昇圧出力は、2 つの TPS92520-Q1 2 チャネル同期整流降圧ドライバを駆動し、4 つの降圧チャネルで合わせて 120W を出力します。このリファレンス・デザインは、車載用ヘッドライトの ECU をエミュレートするためにヒートシンクに取り付けられケースに納められています。MSP432 プロセッサにより、TPS92682-Q1 デバイスと 2 つの TPS92520-Q1 デバイスを SPI インターフェイスで制御します。MSP432 は CAN 経由でマスタと通信するほか、CAN トランシーバ経由で UART 通信を使用して照明マトリクス・モジュールとも通信します。

設計に活用するため、複数のベンチ・テスト結果 (例：効率データ、熱測定、ピクセル制御の負荷データ、CISPR 25 Class 5 伝導仕様に基づく EMC 測定) を掲載しています。

リソース

TIDA-050030	デザイン・フォルダ
TSP92682-Q1	プロダクト・フォルダ
TPS92520-Q1	プロダクト・フォルダ

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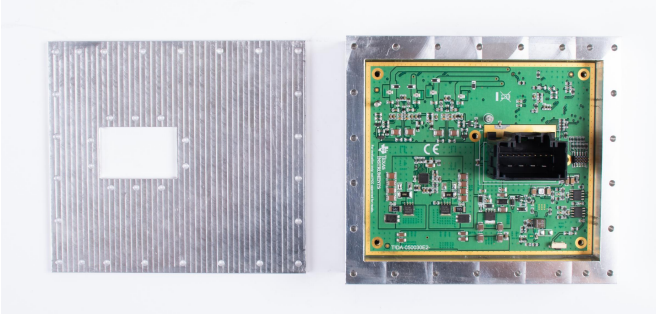
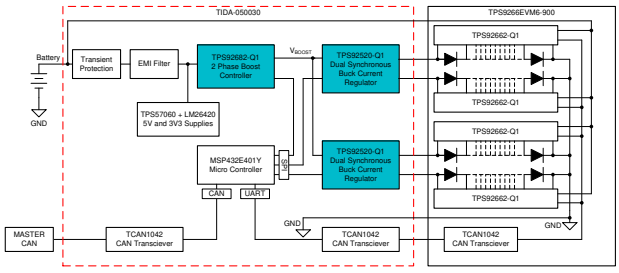
特長

- 1 つの TPS92682 を使用した、電圧出力のインターリーブ昇圧
- 2 つの TPS92520 を使用した、ピクセル制御の負荷に対応する 4 つの同期降圧チャネル
- 動的負荷、マトリクス・コントローラをサポートし、LED ピクセル制御に対応
- 最大 1.5A 、55W (合計 120W 以下) を供給できる降圧チャネル
- 9V～24V の最大出力動作範囲 (出力電力を下げることで最小 6V の入力電圧でも動作可能)
- ケースに納められたヘッドライト ECU の CISPR 25 Class 5 伝導テスト・データ例 (0.15～108MHz)
- バッテリ逆極性保護回路付きのリファレンス・デザイン

アプリケーション

- 車載照明:
  - 動的および静的ヘッドライト
  - リア・ライト





1 System Description

This reference design demonstrates a self-contained headlight ECU with four output channels that can be pixel controlled for a complete headlight solution including low beam, high beam, turn, and DRL (daytime running lights). The design is a two stage boost into multiple buck configuration. The boost, using one TPS92682 in voltage regulation mode, is an interleaved 130W output with adjustable voltage output. The four-buck outputs are delivered by two dual-channel TPS92520 synchronous buck converters. The system can operate during cold crank and load dump conditions when the battery voltage varies. A two-stage ECU is needed due to the dynamic nature of a matrix load where the LED current regulation is done by a low output capacitor topology such as a buck at the second stage, and the wide input voltage variability of an automotive battery system requires a boost first stage to ensure a consistent input voltage for the buck second stage. The buck converter outputs are capable of pixel control using TPS9266x lighting matrix manager devices.

The reference design also includes reverse battery protection, bias supplies, a heat sinking enclosure, and a MSP432 micro controller with self-contained software enabling a headlight ECU with CAN interface.

This reference design considers the following as part of the design requirements:

- Each channel capable of 55W max, total for all channels is 120W
- Each channel capable of 1.5-A LED current maximum
- Operation during cold cranking, warm crank, power is derated
- Tested via SPI communications, self-contained ECU via CAN communications
- Enclosure and heatsink to provide EMC and thermal test data
- Reverse battery connection protection

1.1 Key System Specifications

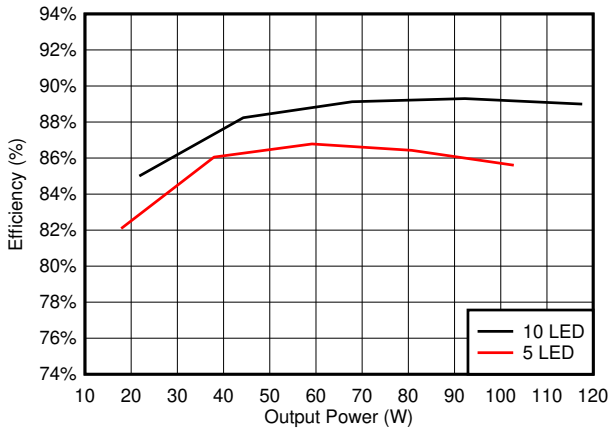
表 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage range of operating DC (continuous)	Full output power	9	13	24	V
Input voltage range of operating DC (power derated)	Power de-rated which covers cold and warm crank conditions	6	-	44	V
OUTPUT CHARACTERISTICS					
Interleaved Boost output	Output power at Vout = 50V			130	W
Maximum string length per channel	LEDs at forward voltage of 3V			14	
VLED output voltage		4		42	V
ILED output current				1.5	A
Bucks Output power				120	W
SYSTEM CHARACTERISTICS					
fSW switching frequency - Boost			400		kHz
fSW switching frequency - Buck			400		kHz

表 1. Key System Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total System Efficiency	@ 5 LEDs		86		%
	@10 LEDs		89		%
EMI (conducted)					
BASE BOARD CHARACTERISTICS					
PCB Form Factor	3.610" (W) x 4.280" (L) x 0.062" (T)	-		-	in.
ECU Fort Factor	4.5" (W) x 5.0" (L) x 1.425" (T)				in.
Number of layers and Stackup	Layer 1:1 oz. cu., Layer 2:2 oz. cu., Layer 3:2 oz. cu., Layer 4:2 oz. cu., Layer 5:2 oz. cu., Layer 5:and 1 oz. cu.	-	6	-	Layers

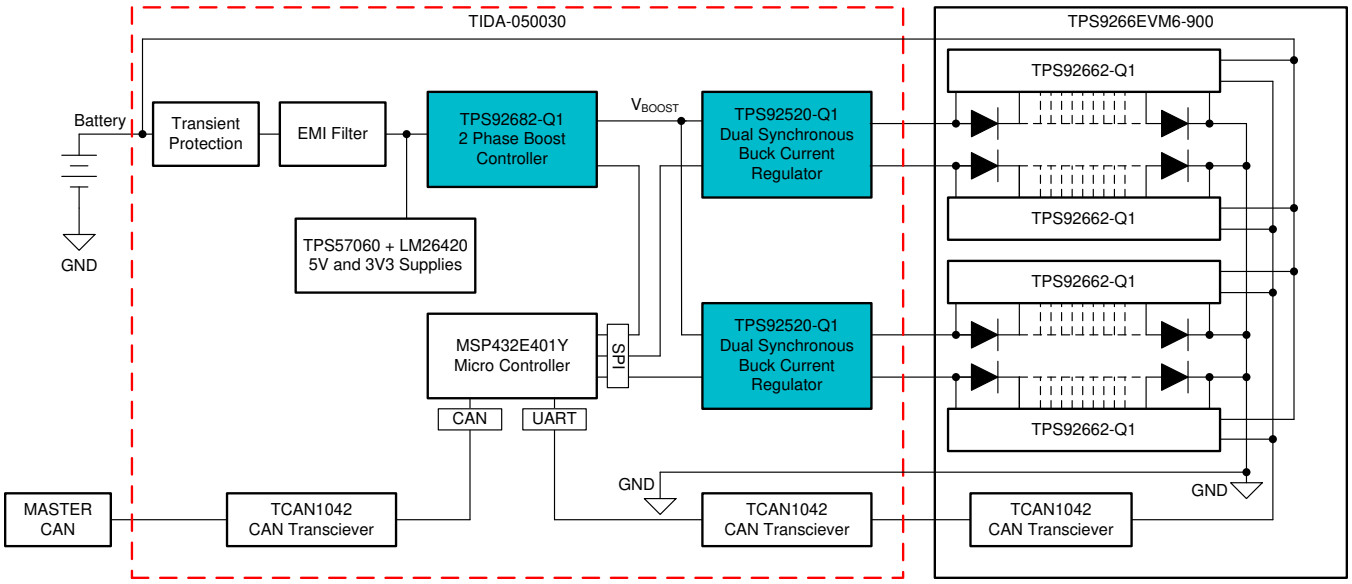
図 1. Output Power vs. Efficiency at VIN = 13 V



2 System Overview

2.1 Block Diagram

図 2. Block Diagram of TIDA-01520



2.2 Design Considerations

This reference design implements a high density, high efficiency, two stage boost into multiple buck LED drivers that supports four channels into a LED matrix manager with a total of 120 watts of output power. The design was implemented considering the following automotive requirements and design goals:

- Small form factor that is approximately a 100 cm^2 with high power density
- Enclosure to provide EMC shielding and heat sinking for thermal dissipation
- Reverse battery connection protection
- Operation during cold cranking, warm crank, power is derated
- Each channel capable of 55W max, total for all channels is 120W
- Each channel capable of 1.5-A LED current maximum
- CISPER25 Class 5 compliant

2.3 Highlighted Products

2.3.1 TPS92682-Q1

The TPS92682-Q1 is a dual-channel, peak current-mode controller with SPI communication interface. The device is programmable to operate in constant-voltage (CV) or constant-current (CC) modes. In CV mode, TPS92682-Q1 can be programmed to operate as two independent or dual-phase Boost voltage regulators. The output voltage can be programmed using an external resistor voltage divider, and a SPI-programmable 8-bit DAC.

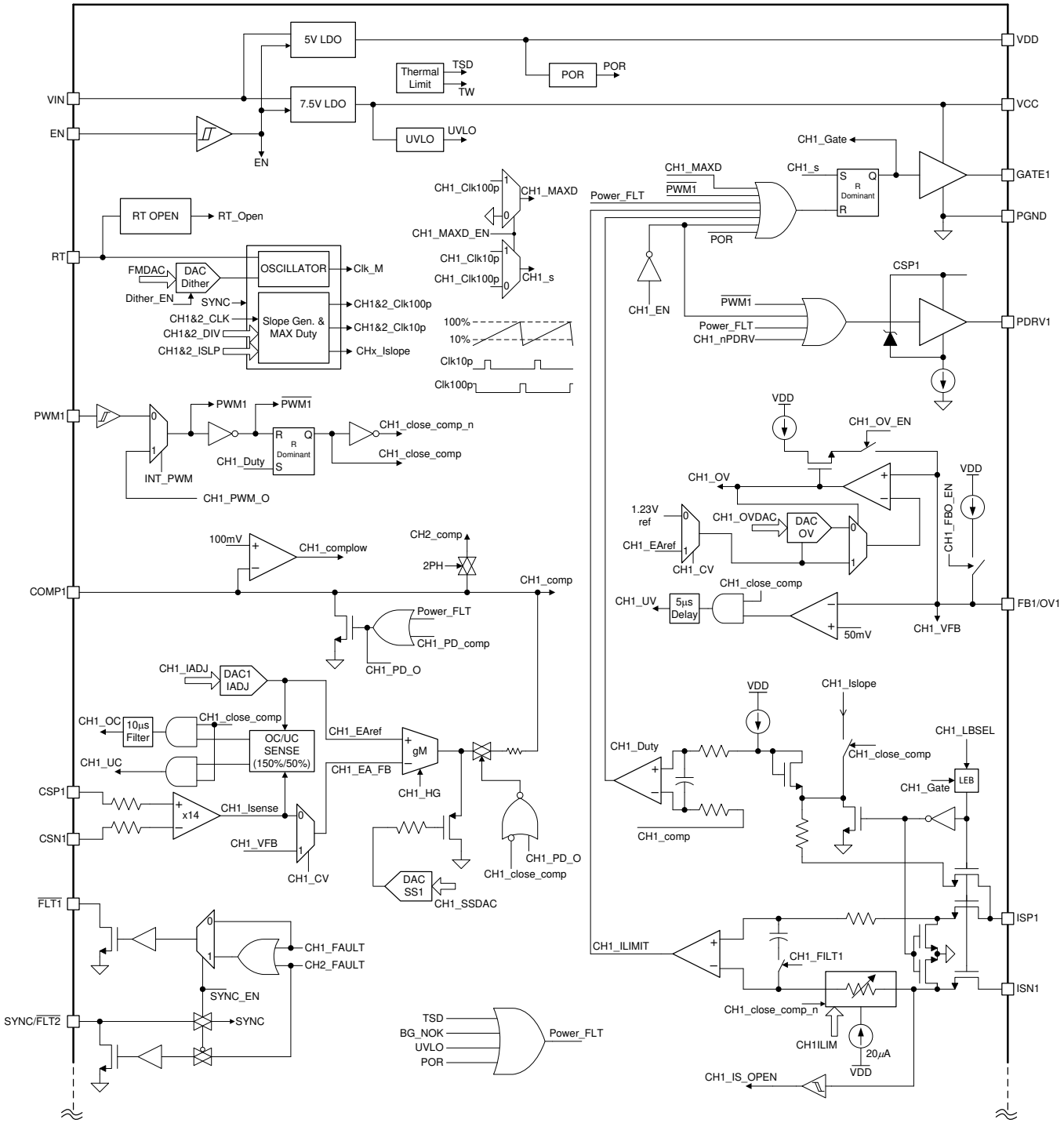
In CC mode, the device is designed to support dual channel step-up or step-down LED driver topologies. LED current can be independently modulated using analog or PWM dimming techniques. Analog dimming with over 28:1 range is obtained using a programmable 8-bit DAC. PWM dimming of LED current is achieved either by directly modulating the PWM input pins with the desired duty cycle, or using a SPI-programmable 10-bit PWM counter. The optional PDRV gate driver output can be used to drive an external P-Channel series MOSFET.

The TPS92682-Q1 incorporates an advanced SPI-programmable diagnostic and fault protection mechanism including: cycle-by-cycle current limit, output overvoltage and undervoltage protection, LED overcurrent protection, and thermal warning. The device also includes an open-drain fault indicator output per channel.

The TPS92682-Q1 includes an LH pin, when pulled high, initiates the limp home (LH) condition. In LH mode, the device uses a separate set of SPI-programmed registers.

図 3 shows the functional block diagram of the TPS92682-Q1 boost controller. The TPS92682-Q1 is used in constant-voltage (CV) mode for the design of this headlight ECU reference design.

図 3. Functional Block Diagram of TPS92682-Q1 Boost Controller



2.3.2 TPS92520-Q1

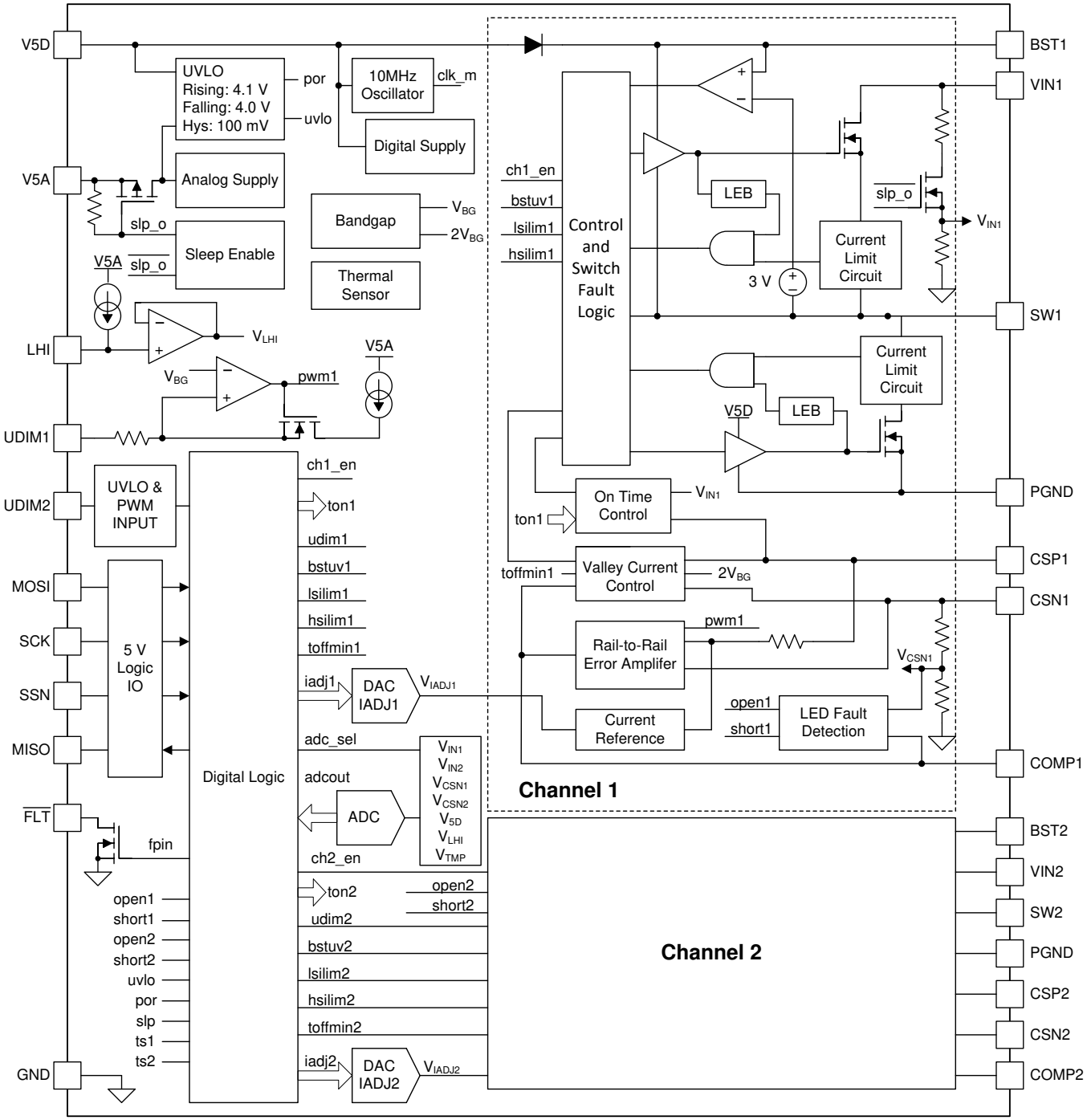
The high-performance LED driver can independently modulate LED current using both analog or PWM dimming techniques. The TPS92520-Q1 is a dual synchronous monolithic device that incorporates four MOSFETs into a high density package that provides superior thermal performance. Linear analog dimming response with over 20:1 range is obtained by programming the 10-bit IADJ value via SPI. PWM dimming of LED current is achieved by directly modulating the corresponding UDIM input pin with the desired duty cycle or by enabling the internal PWM generator circuit. The PWM generator translates the 10-bit PWM register value to a corresponding duty cycle by comparing it to an internal digital counter.

The TPS92520-Q1 incorporates an advanced SPI programmable diagnostic and fault protection featuring: cycle-by-cycle switch current limit, BOOT undervoltage, LED open, LED short, thermal warning and thermal shutdown. An on-board 10-bit ADC samples critical input parameters required for system health monitoring and diagnostics.

The TPS92520-Q1 is available in 6.2 mm x 11 mm thermally enhanced 32-pin HTSSOP package with a 3.86mm x 3.9 mm top exposed pad.

図 4 shows a block diagram of the TPS92520-Q1 buck LED driver.

図 4. Functional Block Diagram of TPS92520-Q1 Buck LED Driver

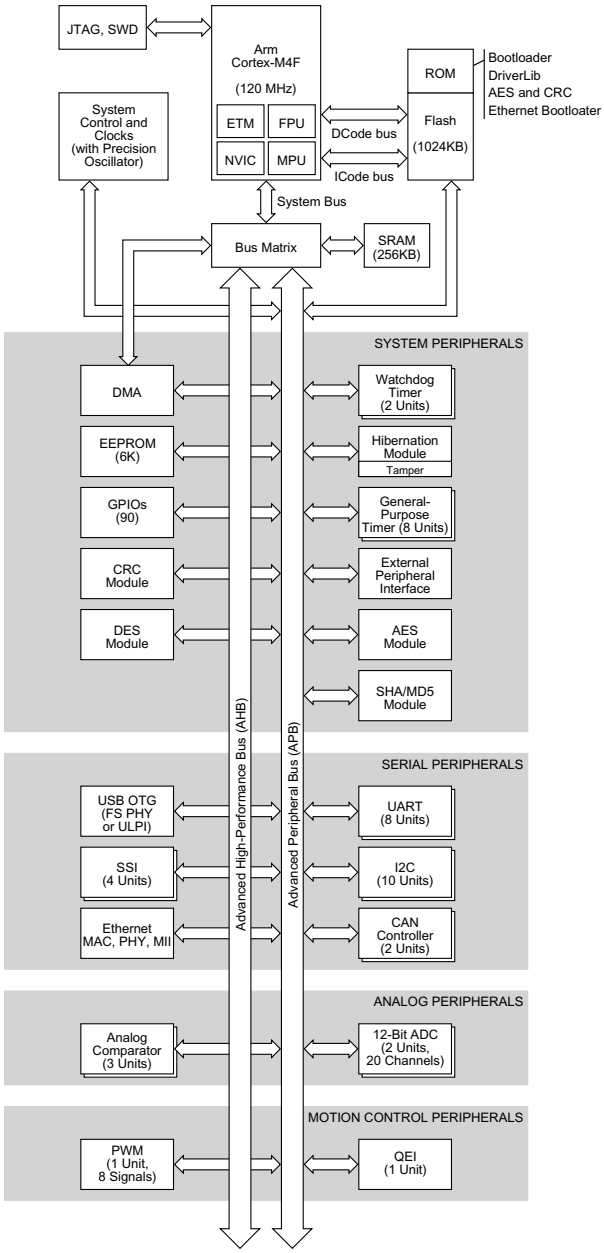


2.3.3 MSP432E401Y

The SimpleLink MSP432E401Y Arm® Cortex® -M4F microcontrollers provide top performance and advanced integration. The product family is positioned for cost-effective applications requiring significant control processing and connectivity capabilities. The MSP432E401Y microcontrollers integrate a large variety of rich communication features to enable a new class of highly connected designs with the ability to allow critical real-time control between performance and power. The microcontrollers feature integrated communication peripherals along with other high-performance analog and digital functions to offer a strong foundation for many different target uses, spanning from human-machine interface (HMI) to networked system management controllers

図 5 shows a block diagram of the MSP432E401Y microcontroller.

図 5. Functional Block Diagram of MSP432E401Y Microcontroller



2.4 System Design Theory

2.4.1 PCB and Form Factor

This reference design uses a six-layer printed circuit board (PCB) where components are placed on both sides and a machined enclosure interfaces to the bottom of the board to provide heat sinking. Thermal vias are used to conduct heat from the top side of the PCB to the bottom for thermal management. The enclosure is machined to allow for direct thermal connection to the TPS92520s on the bottom of the board along with other components that need heasinking directly to the enclosure. Placing components on both sides of the board ensures a high density design. The PCB has a dimension of 109 mm × 92 mm. The primary objective of the design with regards to the PCB is to make a solution that is compact while still adequate heat sinking. The enclosure was also designed to provide shielding for EMI/EMC compliance required by each automotive company. In a final-production version of this reference design, the size of the solution can be further reduced. 図 6 shows a 3D rendering of the PCB.

図 6. 3D Render of TIDA-050030 PCB–Top Side

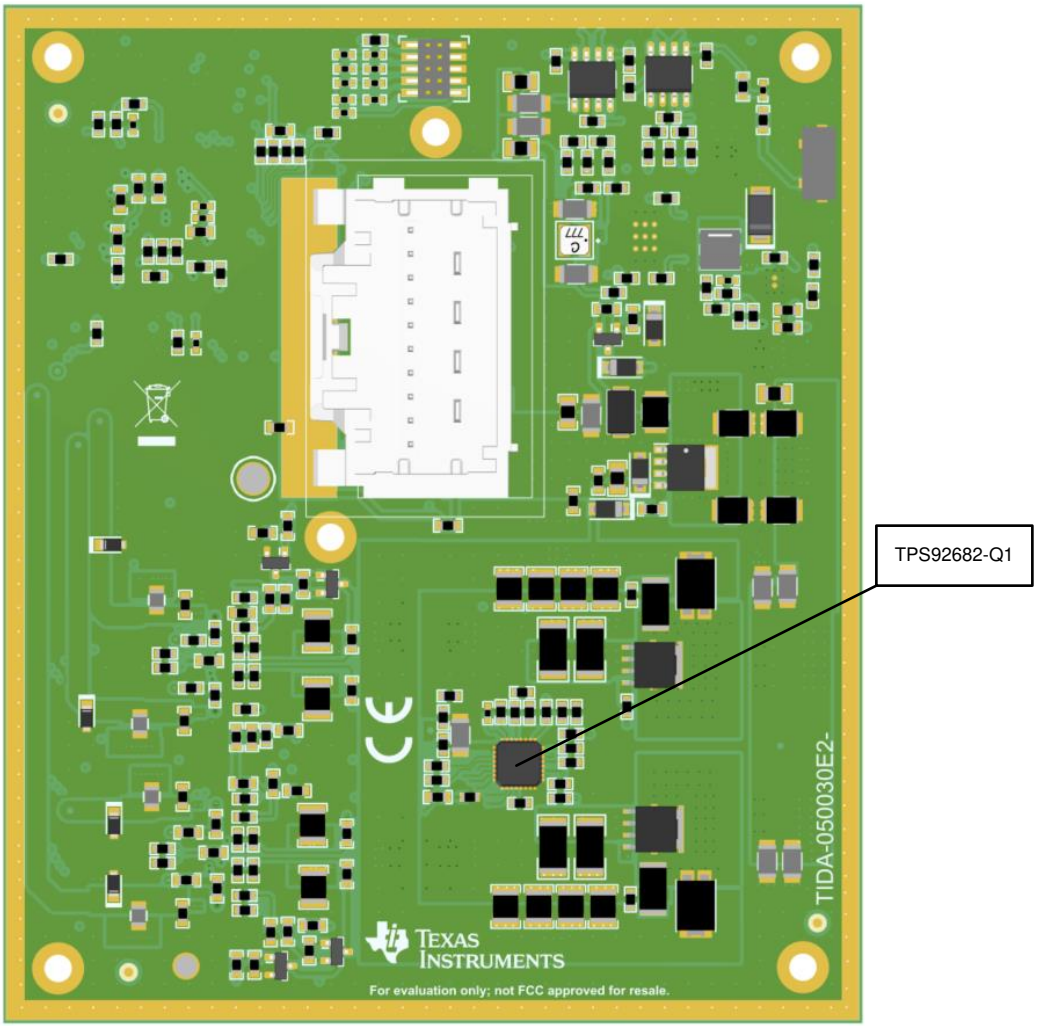
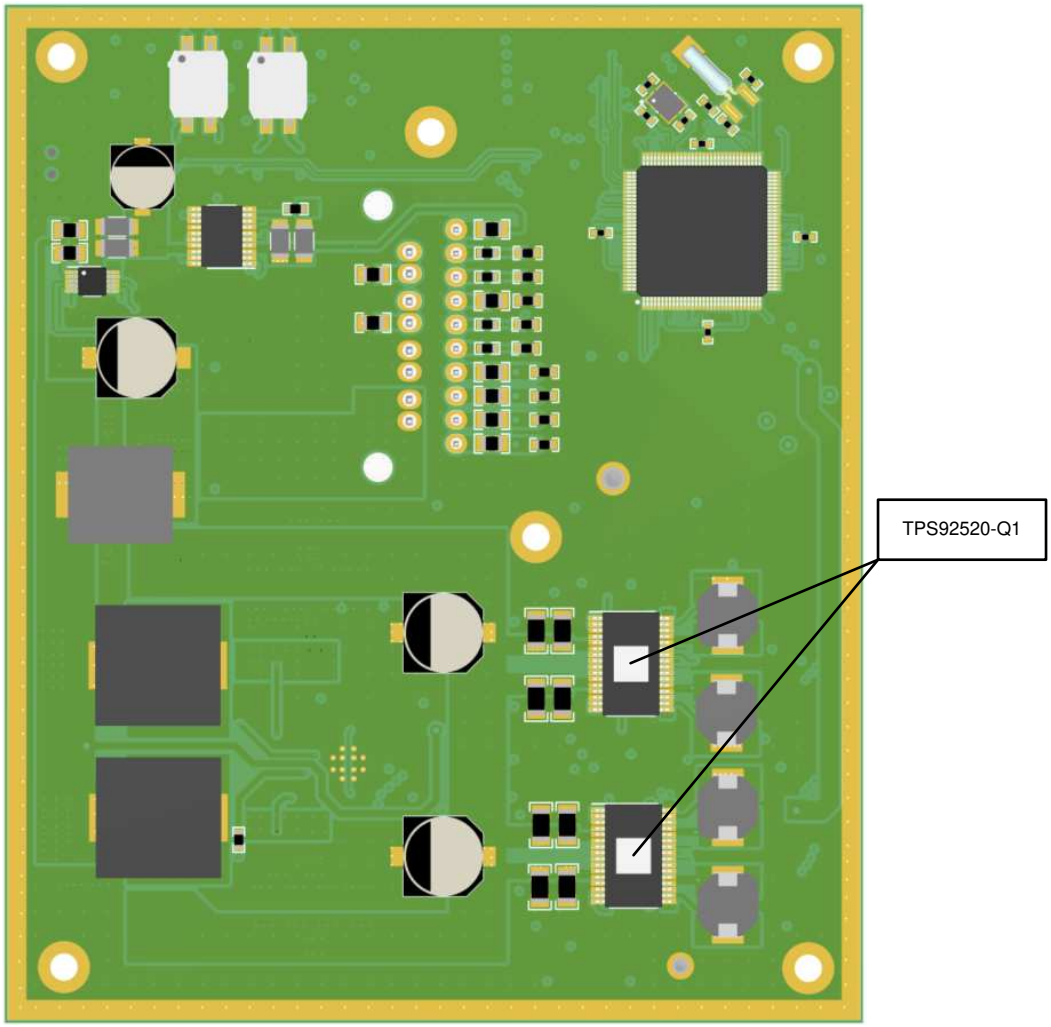


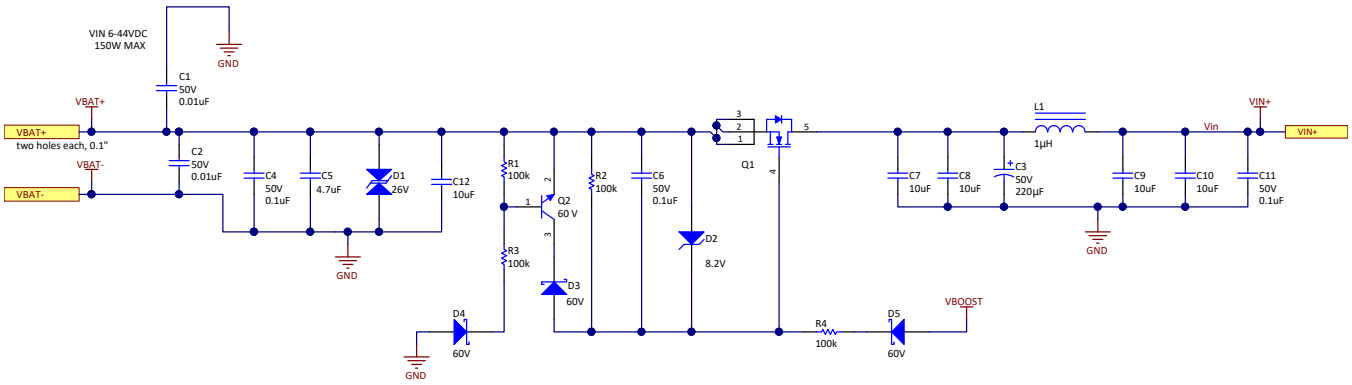
図 7. 3D Render of TIDA-050030 PCB–Bottom Side



2.4.2 Input Protection

In this reference design, reverse polarity protection is implemented by using the body diode of an N-channel MOSFET, Q1, in conjunction with the VBOOST to turn on the MOSFET when the system is active and thus reducing the power dissipation that would otherwise be dissipated using a schottky. Q2, D3, and D4 work together to ensure fast turn off of the Q1 FET during fault conditions, D2 is a zener that protect the gate of the Q1 by clamping it to less than 10 V, and D5 ensures that Q1 doesn't turn on until the system is fully up and running and VBOOST has been raised to greater than +VBAT, see 図 8. D1 is a transient voltage suppressor (TVS) that protections against over voltage conditions during faults and provides reverse battery protection.

図 8. Schematic of Input Protection + EMI Filter



2.4.3 EMI Filter

A LC low-pass filter is placed on the input of the boost controller to attenuate conducted differential mode noise generated by the system. The filter consists of C3, C7, C8, C9, C10, C11, and L1 as shown in 図 8. Additional localized filtering, which includes C1, C2, C4, C5 and C12, is added close to the connector J2 to further help reduce conducted EMI. For more details, see *Simple Success With Conducted EMI From DC-DC Converters*.

2.4.4 TPS92682-Q1 Boost Controller

表 2 shows the default design parameters for the boost controller.

表 2. Design Parameters of Default Boost Controller

DESIGN PARAMETERS	VALUE
Output voltage range	18 V to 55 V
Output power	130 W
Minimum input voltage (DC)	6 V
Typical input voltage (DC)	13.5 V
Maximum input voltage (DC)	24 V
Switching frequency	260 kHz

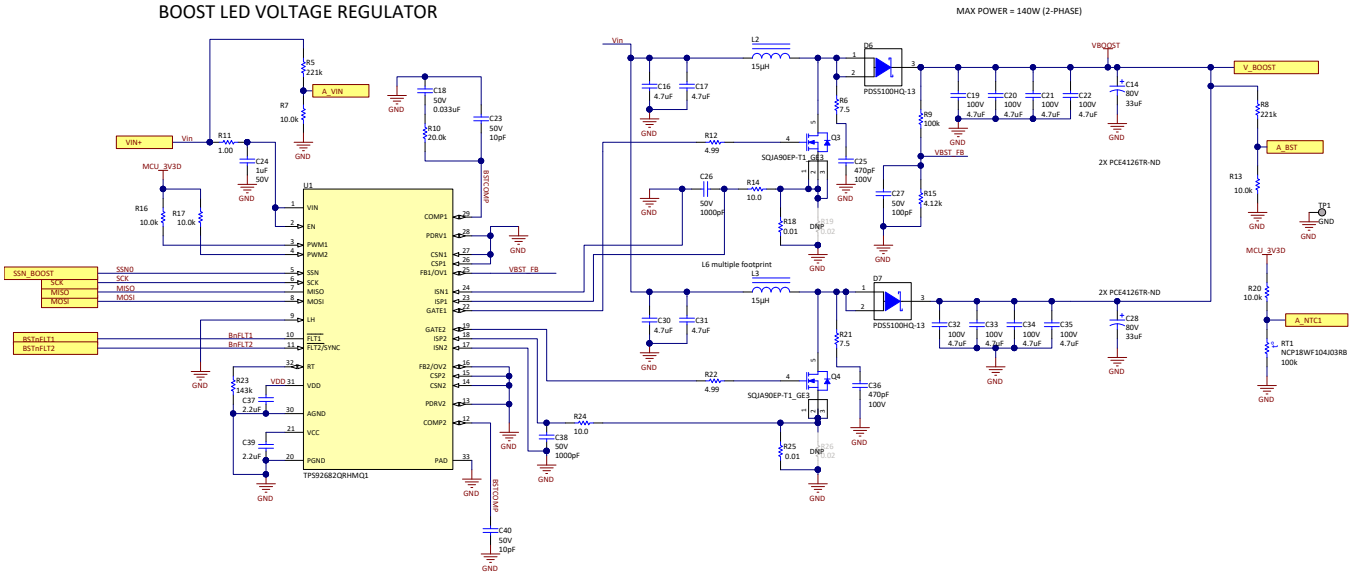
For the maximum boost ratio (6 V to 45 V), the switching frequency of the TPS92682-Q1 is limited by a forced off-time. Based on 式 1, the internal clock frequency, F_{CLKM}, is set by R23. In conjunction with the SWDIV register (address 0x03h) setting (in this case set to divide by four (0x01h), the switching frequency, F_{SW}, is set following to $CHx_{CLK} = f_{CLKM}/4$, where CHx_{CLK} is the channel clocks (switching frequency).

注: The TPS92682 is setup as a two phase constant voltage controller and the effective F_{SW} is twice the channel frequency.

$$f_{CLKM} = \frac{10^{12}}{12.5 \times R_T} \quad (1)$$

図 9 shows the default TPS92682-Q1 boost controller schematic of this reference design.

図 9. Schematic of TPS92682-Q1 Boost Controller



The main components of the boost stage are selected by following the Detailed Design Procedure section in the data sheet *TPS92682-Q1 Dual -Channel Constatnt-Voltage and Constant-Current Controller with SPI Interface*.

R23, same as R_T, sets the switching frequency. The inductor L2 and L3 has a value of 15 µH with a saturation current rating above the maximum expected inductor current of 10.6 A at a minimum input voltage of 9 V. Based on this input current capability, a value of 10 mΩ is selected for the current sense resistor R18 and R25. R14, R26, C26, and C38 form a filter for the current sensing for each phase.

The output capacitors smooth the output voltage ripple and provide a source of charge during transient loading conditions. Also the output capacitors reduce the output voltage overshoot when the load is disconnected suddenly. Ripple current rating of output capacitor must be carefully selected. In a boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high, which makes ceramic capacitors a perfect fit. The output voltage ripple is dominated by ESR of the output capacitors. Paralleling the output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors. This example uses four 4.7-µF ceramic capacitors and one 0.1-µF ceramic capacitor with a voltage rating of 100 V per phase. Additional bulk capacitance was added via two 33-µF electrolytic capacitors for added ripple reduction and greater energy storage. A higher output voltage ripple in this reference design is not a concern for the buck LED drivers, which are connected to the boost output voltage. Input capacitors C16, C17, C30, and C31 smooth the input voltage ripple. This reference design uses small-sized 4.7-µF ceramic capacitors with a voltage rating of 50 V.

The low-side power switches Q3 and Q4 are 80-V rated N-channel MOSFETs in a PowerPAK® package. 100-V Schottky diodes D6 and D7 are used as the catch diode to improve efficiency. R12 and R22 are gate resistors that can limit the rise and fall times of the switch node voltage. A resistor-capacitor snubber network (R6, R21, C25, and C36) across the N-channel MOSFETs, Q3 and Q4, reduces ringing and spikes at the switching node. For how to calculate these values, see *Power Tips: Calculate an R-C snubber in seven steps*.

R10, C18, C23 and C40 configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For more details, see *How to Measure the Loop Transfer Function of Power Supplies*.

See 4.3 for layout guidelines for the boost controller in this reference design.

2.4.5 TPS92520-Q1 Buck LED Driver

表 3 shows the default design parameters for the buck LED drivers.

表 3. Design Parameters of Default Buck LED Driver

DESIGN PARAMETER	RANGE	DEFAULT VALUE
Input voltage	18 V to 55 V	50 V
LED forward voltage		3 V
Number of LEDs in series	1 to 14	8
Output current range	0.2 A to 1.5 A	1 A
Output voltage	3 V to 42 V	24 V
Output power per channel	30 W max	24 W
Switching frequency		440 kHz

図 10 and 図 11 shows the default TPS92520-Q1 LED driver schematic of this reference design.

図 10. Schematic of TPS92520-Q1 Buck LED Driver–Channels 1 and 2

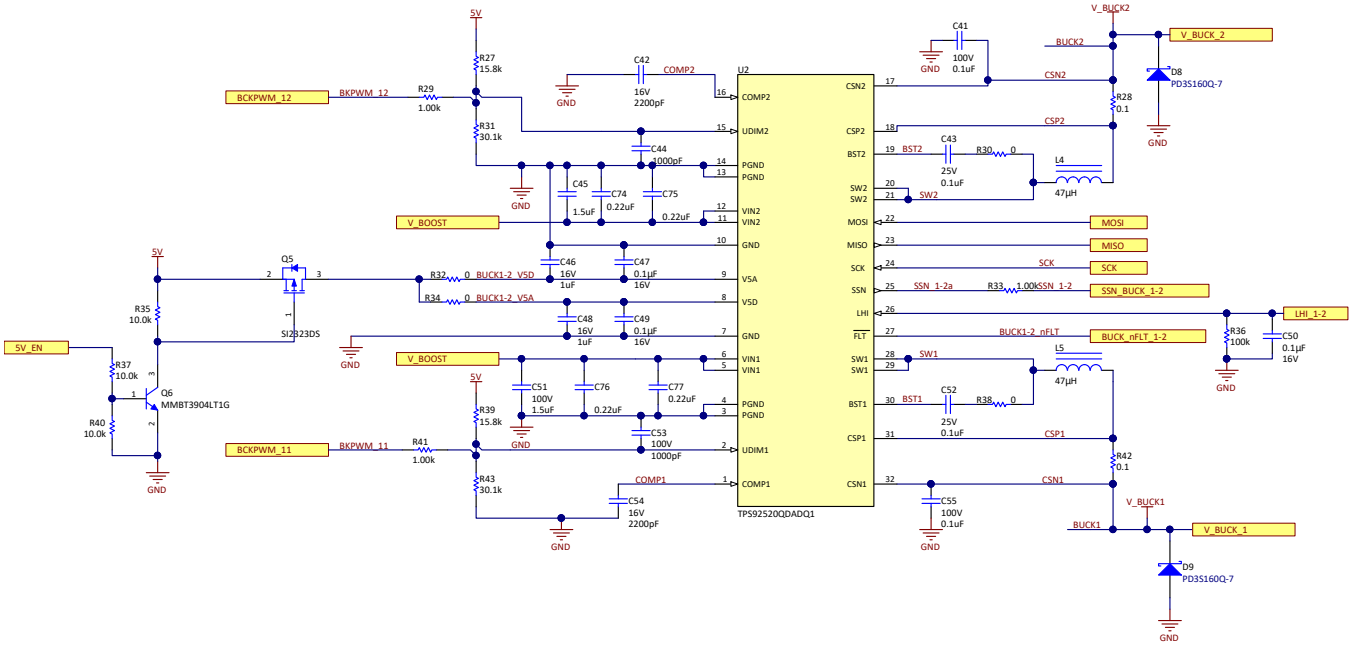
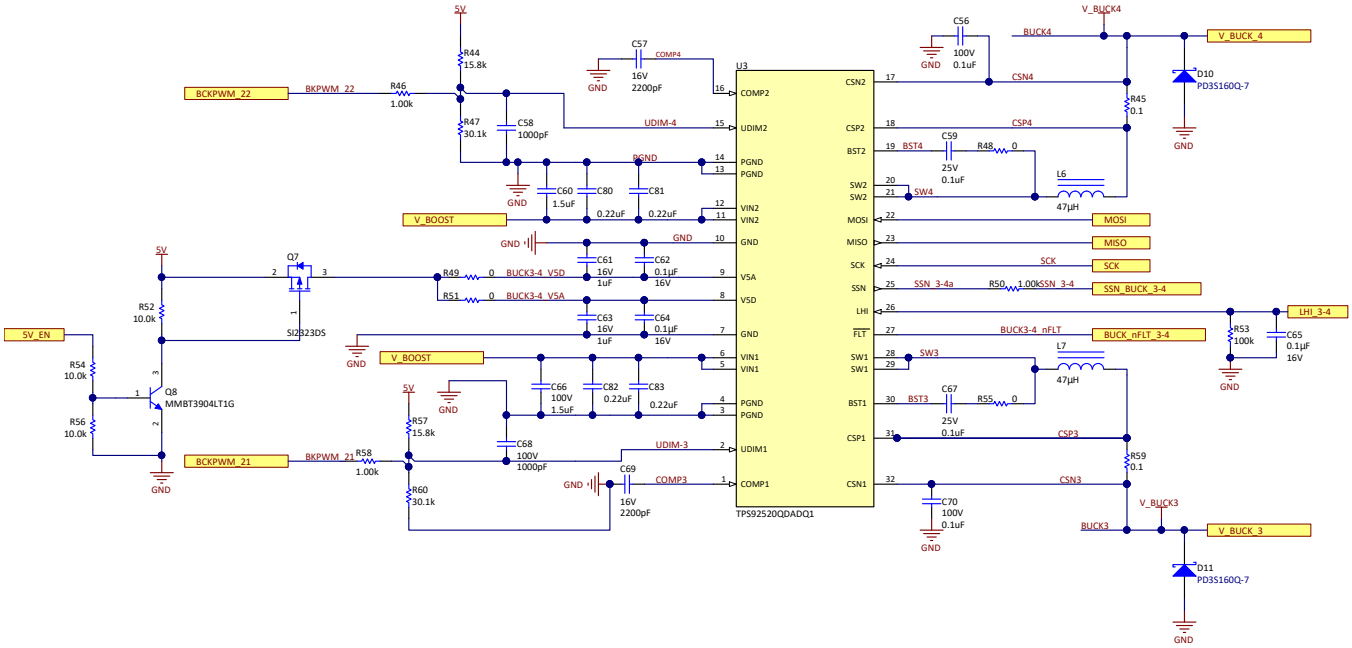


図 11. Schematic of TPS92520-Q1 Buck LED Driver–Channels 3 and 4.



The main components of the buck LED drivers are selected by following the Detailed Design Procedure section in *TPS92520-Q1 4.5V to 65V Input Dual 1.6-A Synchronous Buck LED Driver with SPI Control*.

Components R22, R35, C26, and C39 are used to program the off-time of the hysteretic LED drivers to 0.2 µs. With the default configuration, the LED current is set to 1 A with a inductor ripple current of 0.1 A. When selecting an inductor, ensure the ratings for both peak and average current are adequate. For the inductors L3 and L4, a value of 47 µH is selected. Based on the output current capability, a value of 220 mΩ is selected for the current sense resistors R21 and R34. R23, R24, R36, and R37 program the startup and UVLO level. C28 and C40 at the UVLO pin are placed for noise immunity. Capacitors C20 and C33 tied to the switch node (SW pin) and the diodes D6 and D10 connected to the VCC supply power the BOOT pin to ensure proper operation of the internal MOSFET. The 10-µF VCC capacitors C19 and C31 supply current for the device operation as well as additional power for external circuitry. The low-side rectifier diodes D7 and D12 are 3-A rated, low-leakage, Schottky diodes in a PowerDI5 package. Diodes D8 and D13 provide reverse polarity protection to the PWM pin because the signal is coming from the input voltage. With a voltage higher than 1 V on the PWM, the device starts operation.

The input capacitors C21, C22, C23, C34, C35, and C36 provide a low impedance source for the discontinuous input current of the buck LED drivers. The output capacitors C24, C25, C37, and C38 in parallel with the LED load reduce the ripple current on the LEDs. The TPS9250-Q1 has a rail to rail, fast output current sense that allows true average current regulation all the way down to fully shunted output to allow for current regulation accuracy as well as dynamic load operation.

2.4.6 Duty Cycle Consideration

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is derived using 式 2:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

There is no limitation for small duty cycles, since at low duty cycles, the switching frequency is reduced as needed to always ensure current regulation. The maximum duty cycle attainable is limited by the minimum off-time duration and is a function of switching frequency.

2.4.7 Switching Frequency Selection

Nominal switching frequency ($t_{ON} > t_{ON(MIN)}$) is set by programming the CHxTON register. The switching varies slightly over operating range and temperature based on converter efficiency. 表 4 shows common switching frequencies and corresponding CHxTON register values.

表 4. Frequency Setting

FREQUENCY	CHxTON REGISTER VALUE (DECIMAL)	CHxTON REGISTER VALUE (BINARY)
200 kHz	3	000011
400 kHz	7	000111
1 MHz	19	010011
1.6 MHz	31	011111
2.2 MHz	43	101011

2.4.8 LED Current Set Point

The LED current is set by the external resistor, R_{CS}, and the CHxIADJ register value. The current sense resistor, R_{CS}, is selected to meet the maximum LED current specification and 90% of the full-scale range of CHxIADJ-DAC.

$$R_{CS} = \frac{0.9 \times V_{DAC(FS)}}{14 \times I_{LED(MAX)}} \tag{3}$$

The LED current can be varied between minimum and maximum specified limits by writing to the CHxIADJ register.

2.4.9 Inductor Selection

The inductor is sized to meet the ripple specification at 50% duty cycle. TI recommends a minimum of 30% peak-to-peak inductor ripple to ensure periodic switching operation. Use 式 4 to calculate the inductor value.

$$L = \frac{V_{IN(TYP)}}{4 \times \Delta i_L \times f_{SW}} \tag{4}$$

Use 式 5 and 式 6 to calculate the RMS and peak currents through the inductor. It is important that the inductor is rated to handle these currents.

$$i_{L(RMS)} = \sqrt{\left(I^2_{LED(MAX)} + \frac{\Delta i^2_{L(MAX)}}{12} \right)} \tag{5}$$

$$i_{L(PK)} = I_{LED(MAX)} + \frac{\Delta i_{L(MAX)}}{2} \tag{6}$$

2.4.10 Output Capacitor Selection

The output capacitor value depends on the total series resistance of the LED string, r_D, and the switching frequency, f_{SW}. The capacitance required for the target LED ripple current is calculated using the .

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED}} \quad (7)$$

For applications where the converter supports pixel beam or matrix LED loads, additional design considerations influence the selection of output capacitor. The size of the output capacitor depends on the slew-rate setting of the LED bypass switches and must be selected after consulting the lighting matrix manager.

When choosing the output capacitors, it is important to consider the ESR and the ESL characteristics since they directly impact the LED current ripple. Ceramic capacitors are the best choice due to the following:

- Low ESR
- High ripple current rating
- Long lifetime
- Good temperature performance

With ceramic capacitor technoloy, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions. TI recommends an X7R dielectric with a voltage rating greater than maximum LED stack voltage.

2.4.11 Input Capacitor Selection

The input capacitor buffers the input voltage for transient events and decouples the converter from the supply. TI recommends a 2.2 µF input capacitor across the VIN pin and PGND placed close to the device, and connected using wide traces. X7R-rated ceramic capacitors are the best choice due to the low ESR, high ripple current rating, and good temperature performance. Additional capacitance can be required to further limit the input voltage deviation during PWM dimming operation.

2.4.12 Bootstrap Capacitor Selection

The bootstrap capacitor biases the high-side gate driver during the high-side FET on-time. The required capacitance depends on the PWM dimming frequency, PWM_{FREQ}, and is sized to avoid boot undervoltage and fault during PWM dimming operation. The bootstrap capacitance, C_{BST}, is calculated using .

$$C_{BST} = \frac{I_{Q(BST)}}{\left(V_{5D} + V_{BST(HYS)} - V_{BST(UV)}\right) \times PWM_{FREQ}} \quad (8)$$

表 5 summarizes the TI recommended bootstrap capacitor value for different PWM dimming frequencies.

表 5. Bootstrap Capacitor Value

PWM DIMMING FREQUENCY (Hz)	BOOTSTRAP CAPACITOR (µF)
1395	0.1
1221	0.1
977	0.15
814	0.15
610	0.22
407	0.33
199	0.56
100	1

2.4.13 Compensation Capacitor Selection

A simple integral compensator is recommended to achieve stable operation across the wide operating range. Use to calculate the compensation capacitor needed to achieve stable response.

$$C_{COMP} = \frac{0.0055 \times \sigma_{BW}}{f_{SW}} \quad (9)$$

The factor, σ_{BW}, determines the bandwidth of the loop and is usually set between 50 and 100 is recommended. A larger σ_{BW} value results in lower loop bandwidth and over-damped response.

2.4.14 Input Undervoltage Protection

図 10 and 図 11 shows that the undervoltage protection threshold is programmed using a resistor divider, R_{UV1} and R_{UV2}, from the input voltage, V_{IN}, to ground. Use 式 10 and 式 11 to calculate the resistor values.

$$R_{UVx2} = \frac{V_{HYS}}{I_{UDIM(UVLO)}} \quad (10)$$

$$R_{UVx1} = \frac{V_{UDIM(RISE)}}{V_{INx(RISE)} - V_{UDIM(RISE)}} \times R_{UVx2} \quad (11)$$

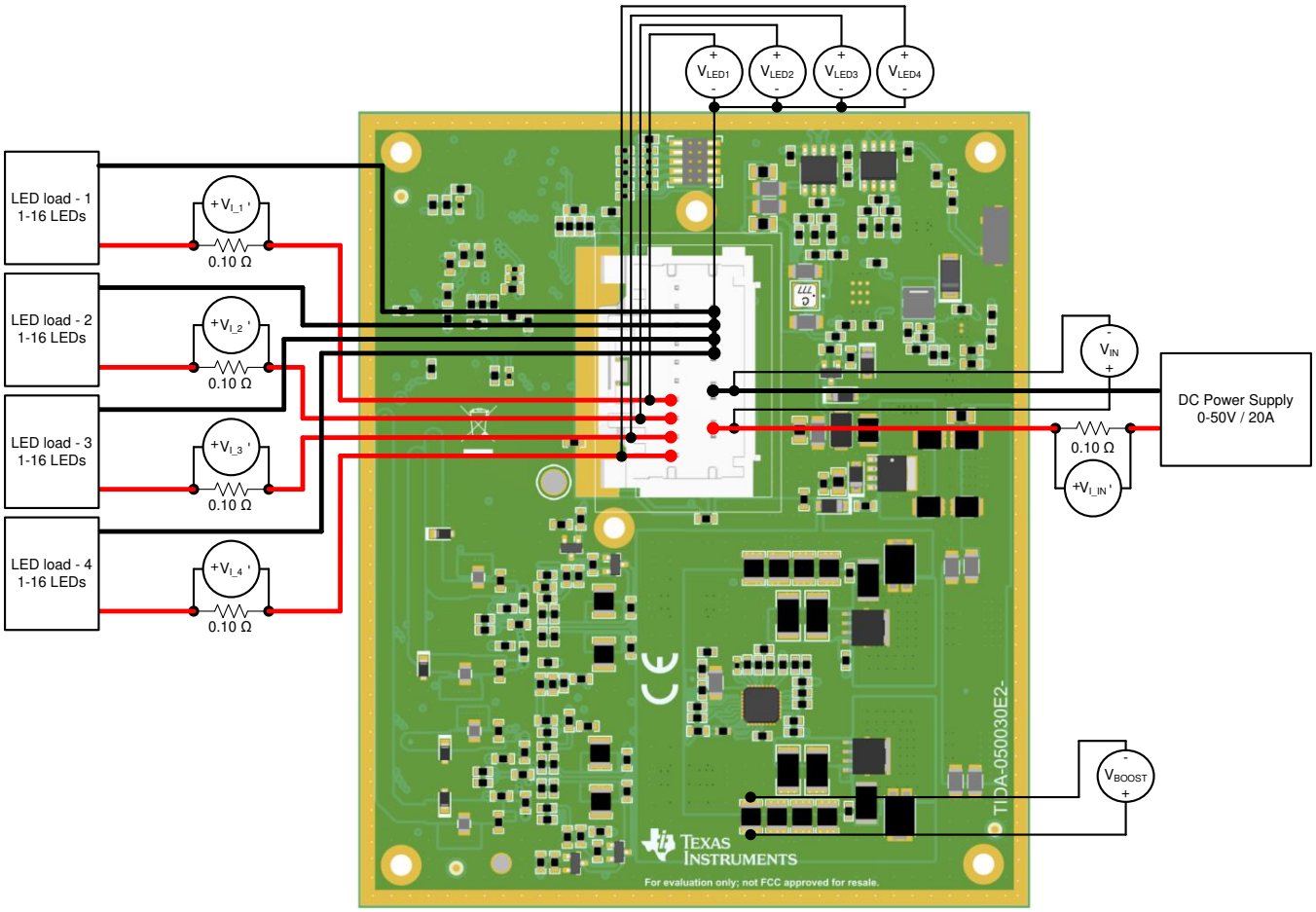
See 4.3 for layout guidelines for the TPS92520-Q1 in this reference design.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

図 12 shows the default test setup for taking efficiency measurements, startup/shutdown, and steady state waveforms of this reference design. Voltage measurements were taken using kelvin connections. The currents were measured using a one percent, 0.1 Ω shunt resistor in conjunction with a precision multi meter for all current measurements. Voltage and current waveforms were taken using voltage and current probes with an oscilloscope. Inductor currents were measured by putting a loop in series with the inductor and using the current probe attached to the oscilloscope.

図 12. Efficiency, Startup/Shutdown, and Steady State Test Setup



Connect a DC power supply to each input terminal (J2, pin 11 (+BAT) and 12 (-BAT)) and the LED strings to the output terminals (J2, pin 1-4, 13, and 1 4).

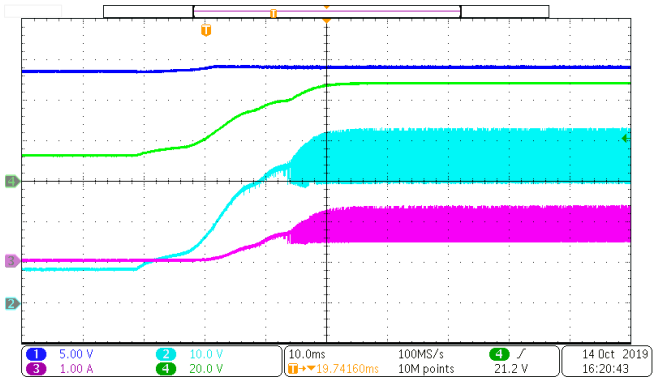
3.2 Testing and Results

All tests in this section are performed in the default configuration where the input voltage is 13.5 V and the LED current is adjusted to generate 30W per channel up to 1.5A. Testing was done with 10 and 5 LEDs.

3.2.1 Startup/Shutdown

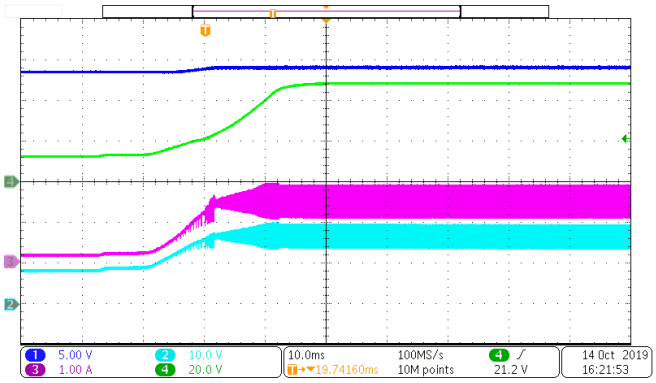
図 13 through 図 16 show the startup and shutdown behavior of the reference design. During startup, the adaptive pre-boost control starts acting and regulates the boost output voltage to the set level.

図 13. Startup, 12 LEDs at 0.75A



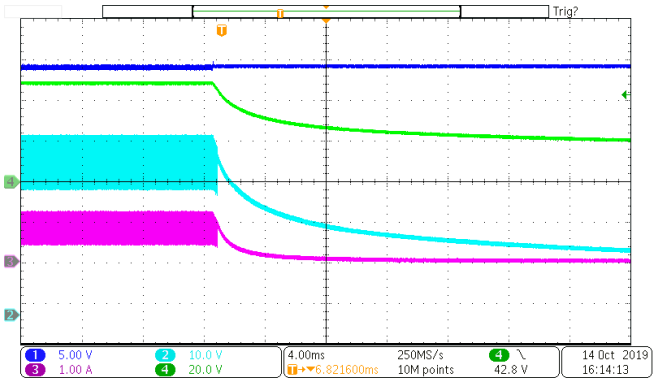
CH1: VIN, CH2: VOUT LED driver, CH3: LED current, CH4: VBOOST

図 14. Startup, 6 LEDs at 1.5A



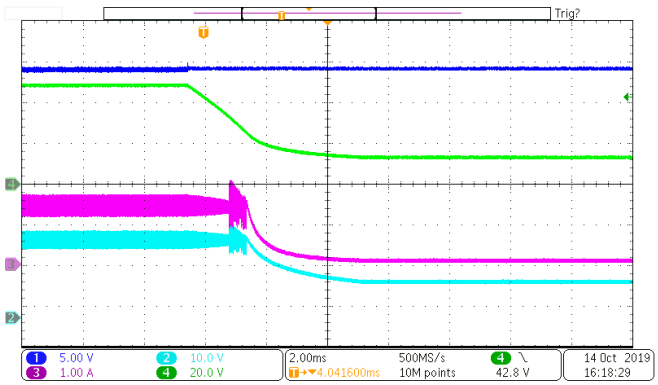
CH1: VIN, CH2: VOUT LED driver, CH3: LED current, CH4: VBOOST

図 15. Shutdown, 12 LEDs at 1.5A



CH1: VIN, CH2: VOUT LED driver, CH3: LED current, CH4: VBOOST

図 16. Shutdown, 12 LEDs at 0.75A

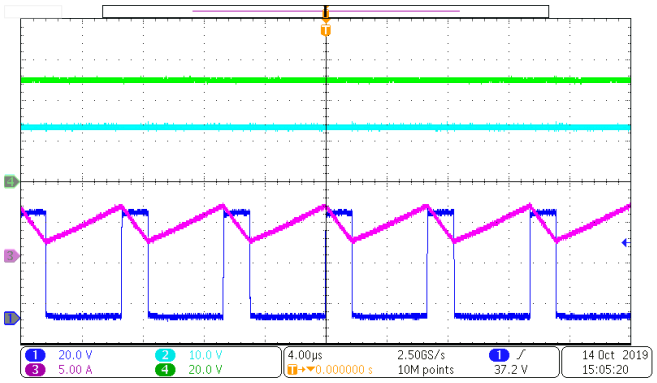


CH1: VIN, CH2: VOUT LED driver, CH3: LED current, CH4: VBOOST

3.2.2 Steady State Operation

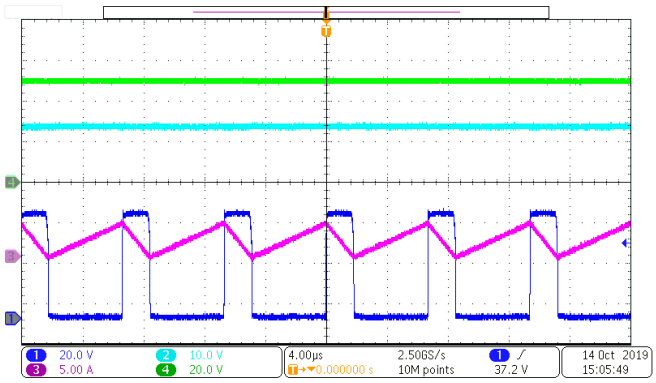
図 17 through 図 20 show the steady state operation of the TPS92682-Q1 boost controller. With 10 LEDs connected, the boost controller operates with nearly a 50 percent duty cycle.

図 17. Boost Operation at 120W output



CH1: SW boost, CH2: VIN, CH3: IL boost, CH4: VBOOST
(NOTE: only one of two phases)

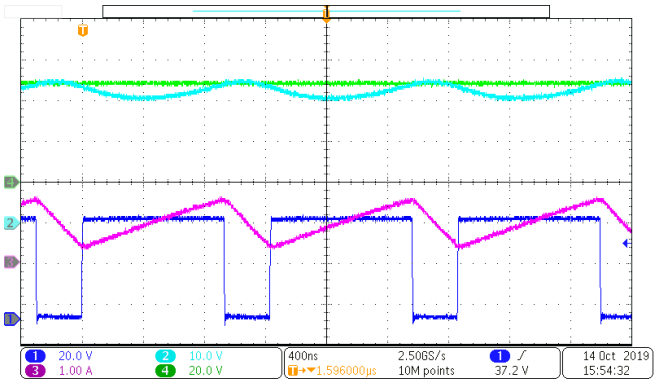
図 18. Boost Operation at 60W output



CH1: SW boost, CH2: VIN, CH3: IL boost, CH4: VBOOST
(NOTE: only one of two phases)

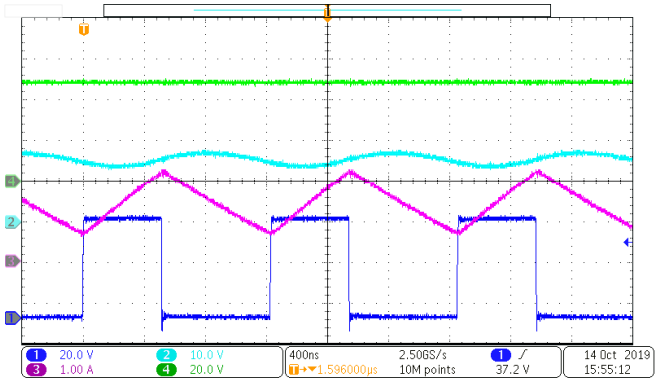
図 19 and 図 20 show the steady state operation of the TPS92520-Q1 buck LED driver.

図 19. LED Driver Operation at 12 LEDs and 1A



CH1: SW LED driver, CH2: VOUT LED driver, CH3: IL LED,
CH4: VBOOST

図 20. LED Driver Operation at 6LEDs at 1A

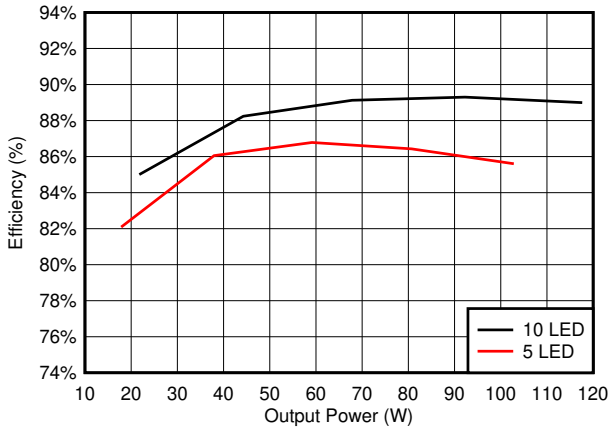


CH1: SW LED driver, CH2: VOUT LED driver, CH3: IL LED,
CH4: VBOOST

3.2.3 Efficiency

図 21 shows the efficiency of the design in different conditions. To achieve a total efficiency of 89 percent, each stage (boost and buck) operates with an efficiency of ≈ 94 percent.

図 21. Output Power vs. Efficiency at VIN = 13 V



3.2.4 Thermal Performance

図 22 through 図 25 show the thermal behavior for different conditions. To improve the thermal performance of the whole board, consider implementing the following items:

- Add more layers on the PCB
- Increase the PCB size
- Increase the copper thickness to 2 oz
- Add a heat sink
- Select larger and more expensive components

The design was run at 120 watts of output power at input voltage of 13.5 V and allowed to thermally stabilize. The TPS92520-Q1 has an internal temp sense to allow for the measurement of the junction temperature of the device via register TEMPL/H (0x1B/1C). The internal junction temperatures of U2 and U3 where read via the SPI bus to confirm the rise in junction temperature (T_J) of the two TPS92520's compared to the ambient air temp of 25°C. The junction temperatures, T_J, are listed in each figure as TPS92520_1-2 and TPS92520_3-4.

図 22. Thermal Image with respect to TIDA-050030 PCB.

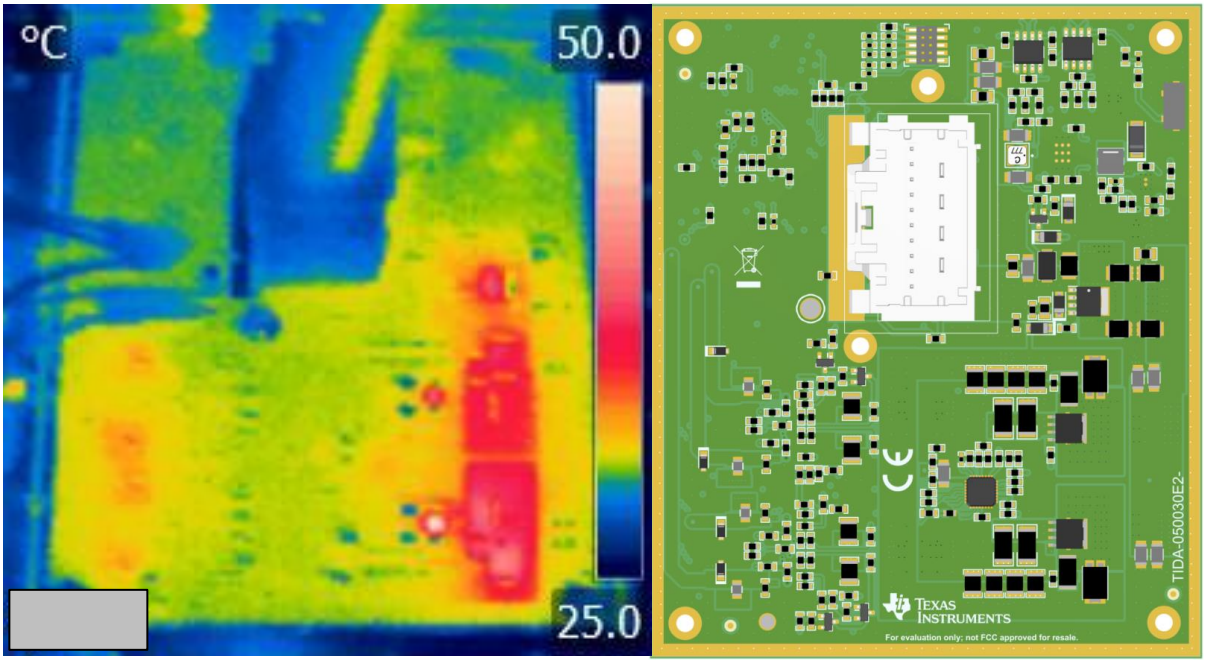


図 23 shows temperatures at various sample points (Sp). Figure A shows that most of the power dissipation is contained within the boost converter section of the design. Sp1 is the case temperature of the TPS92682-Q1. Sp2 and Sp3 are temperatures at the current sense resistors (R25 and R18). Sp5 is the temperature for the current sense resistor of for VBUCK1 (R42). Sp4 and Sp6 are the temperatures next to Q3, D6, Q4, and D7.

図 23. Thermal Image of Top Side PCB at ≈120W Output and at 13.5 V Input. Sample Points 1-6 Shown

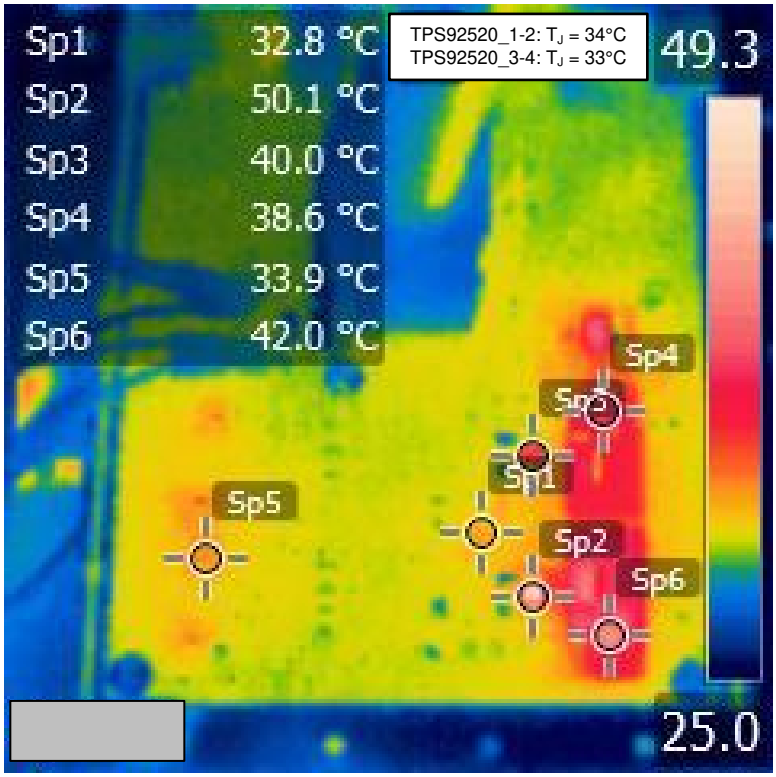


図 24 shows a close up of the boost converters surface temperatures. Sp1 shows the temperature at U1 (TPS92682-Q1). Sp2 and Sp3 show the temperatures of the current sense resistors R18 and R23. Sp4 shows the temp at schottky diode D7 and Sp5 shows the temperature at Q4. We are seeing no more than a 30°C rise worst case at the sense resistors. The other parts that are seeing significant power dissipation are seeing less than 20°C rise.

図 24. Thermal Image: Closeup of Boost Converter Circuitry at ≈ 120 W Output

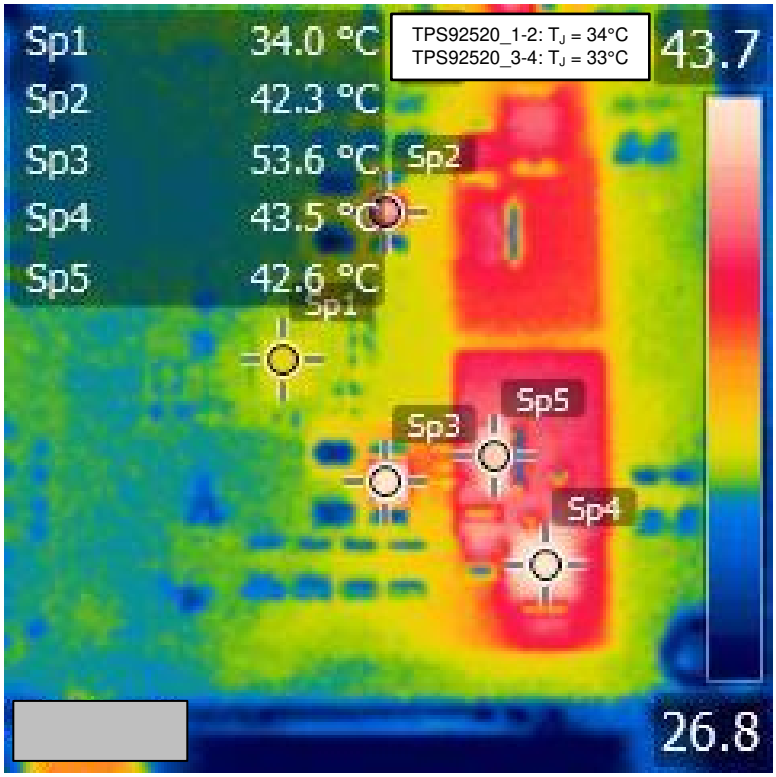
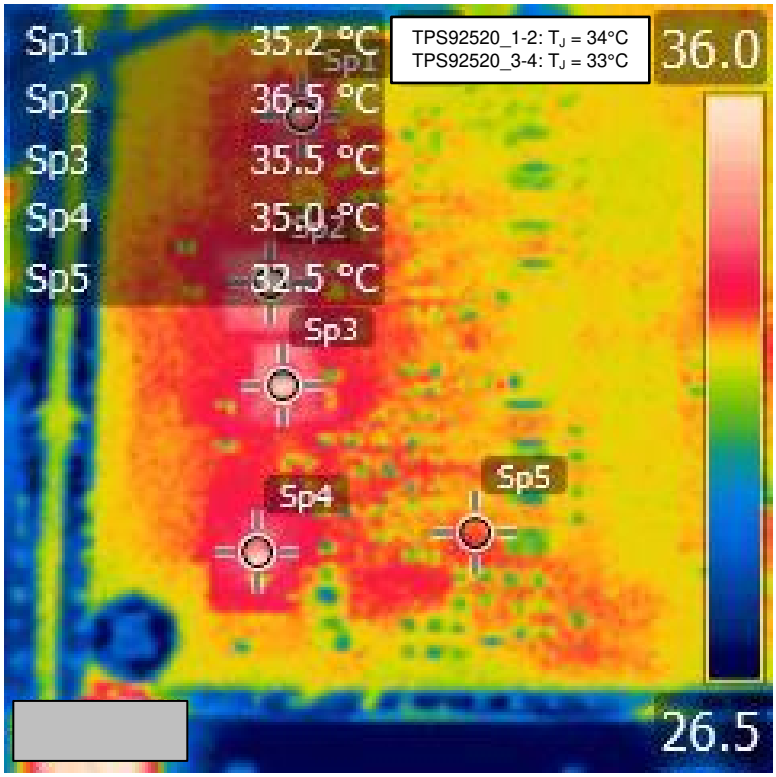


図 25 shows a close up of the two buck LED driver's (TPS92520-Q1) surface temperatures. Sp1, Sp2, Sp3, and Sp4 shows the temperature at all four current sense resistors (R28, R42, R45, and R59) for the four channels (VBUCK1/2/3/4). Sp5 shows the temperatures at the PCB above the TPS92520. We are seeing no more than a 12°C rise worst case at the sense resistors. The TPS92520's are seeing less than 10°C rise given 120W of output power. The enhanced 32-pin HTSSOP package with the 3.86mm x 3.9 mm top exposed pad when mated with heat sink enclosure in conjunction with thermal potting compound performs very well.

図 25. Thermal Image: Closeup of Buck Converter Circuitry at ≈ 120 W Output



3.2.5 LED Matrix Manager

図 26 shows the setup of the design operating with a full light matrix manager solution, specifically the TPS92662/3-Q1 EVM. The matrix evaluation module was controlled via CAN and registers were modified to adjust phase, pulse width, and slew rate, see TPS92662/3-Q1 datasheet for specific register details.

図 26. TIDA 050030 Setup for Lighting Matrix Module Testing

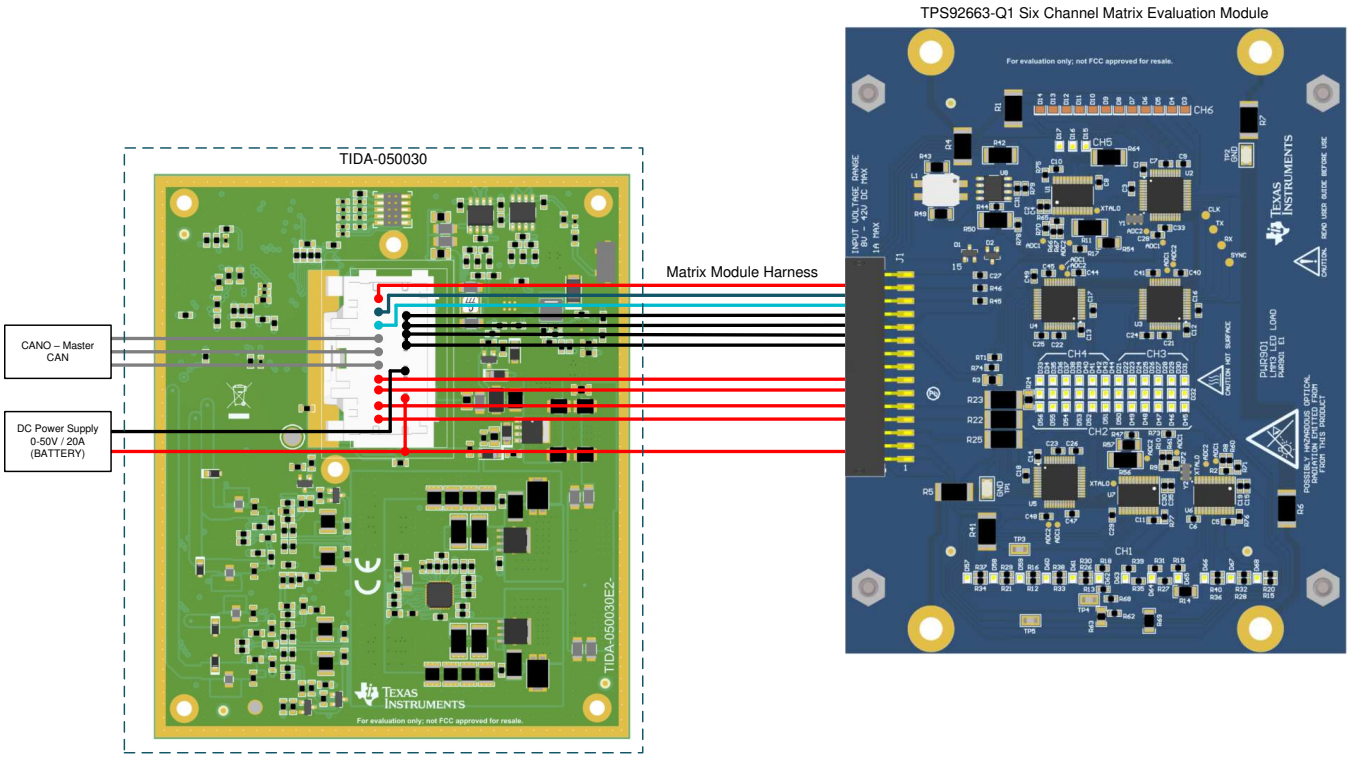
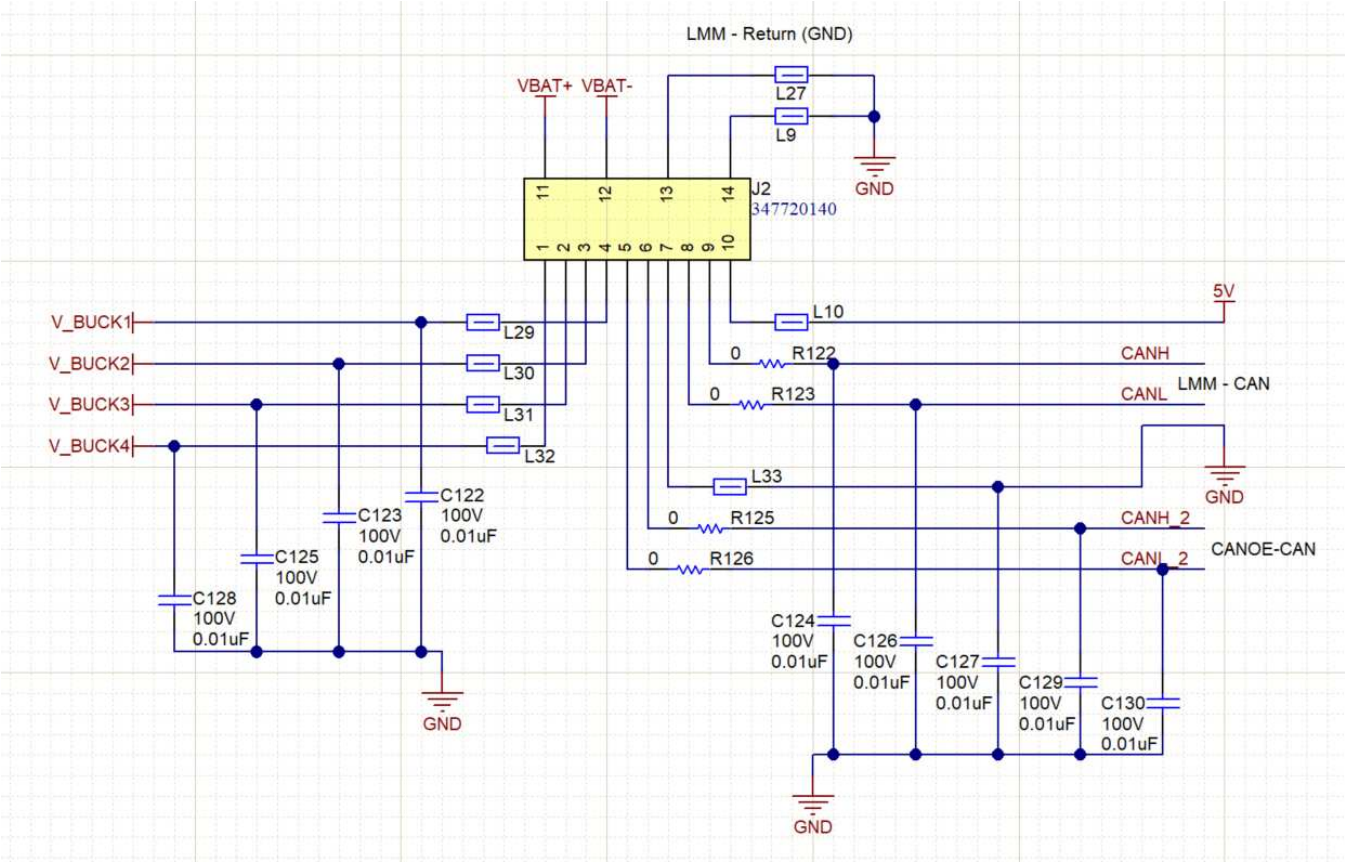


図 27 shows the connection points for the TIDA-050030 connector to the TPS92663-Q1 six channel matrix evaluation module.

図 27. Schematic of TIDA-050030 Connector Connections



Channel 2 of the oscilloscope was setup on V_BUCK2 (teal) to measure the LED voltage of the TIDA-050030 board, while channel 3 of the oscilloscope (magenta) was a current probe measuring the output current of V_BUCK2. The worst case phase and pulse width settings were selected to demonstrate performance. 図 27 shows the connection points for the TIDA-050030 connector to the TPS92663-Q1 six channel matrix evaluation module. TheTPS92662-Q1's registers were setup for phase, pulse width, and slew rate. It is important to note that 図 28, 図 29, and 図 30 show how the TPS92520-Q1's maintains current regulation with minimal over/undershoot with fast settling to the regulation set point. See the TPS92662-Q1 data sheet for details about registers and settings.

図 28. Waveforms of 0 Phase Shift, 20/1024 Pulse Width, SLEWRATE=01, at 350mA Using Lighting Matrix Module EVM

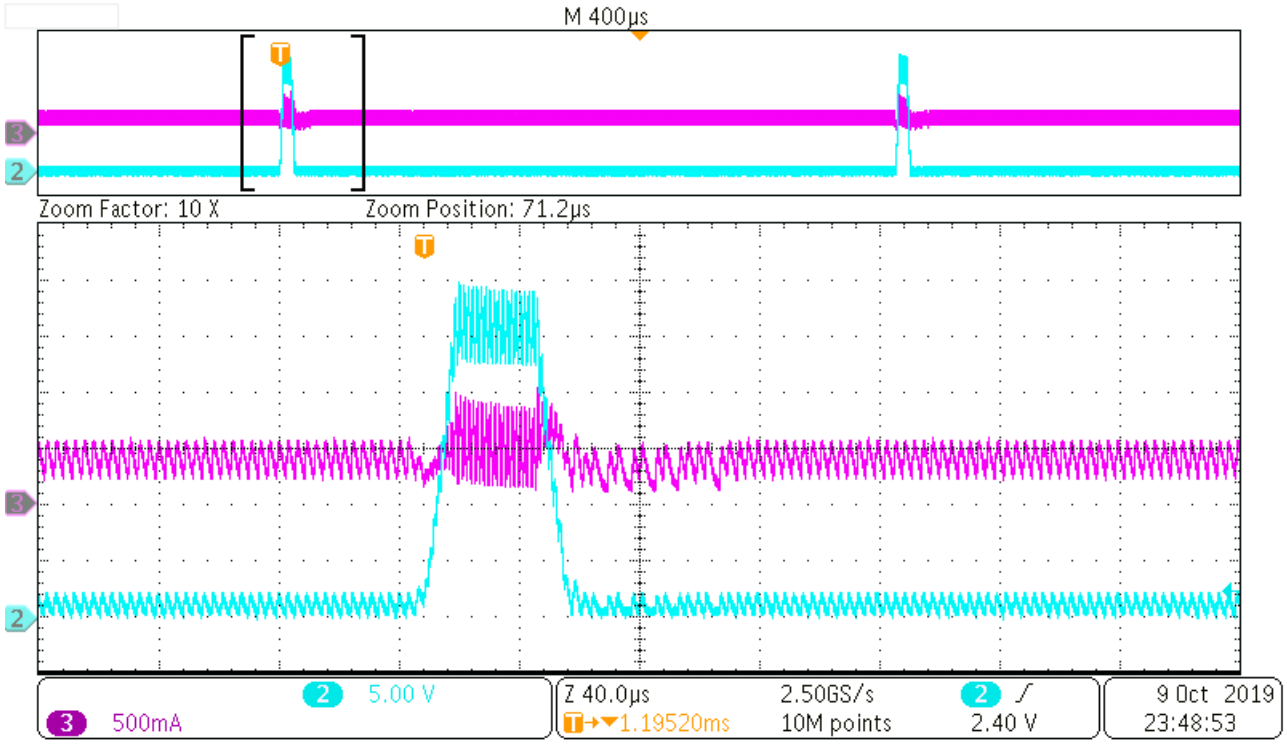


図 29. Waveforms of 0 Phase Shift, 1000/1024 Pulse Width, SLEWRATE=01, at 350mA Using Lighting Matrix Module EVM

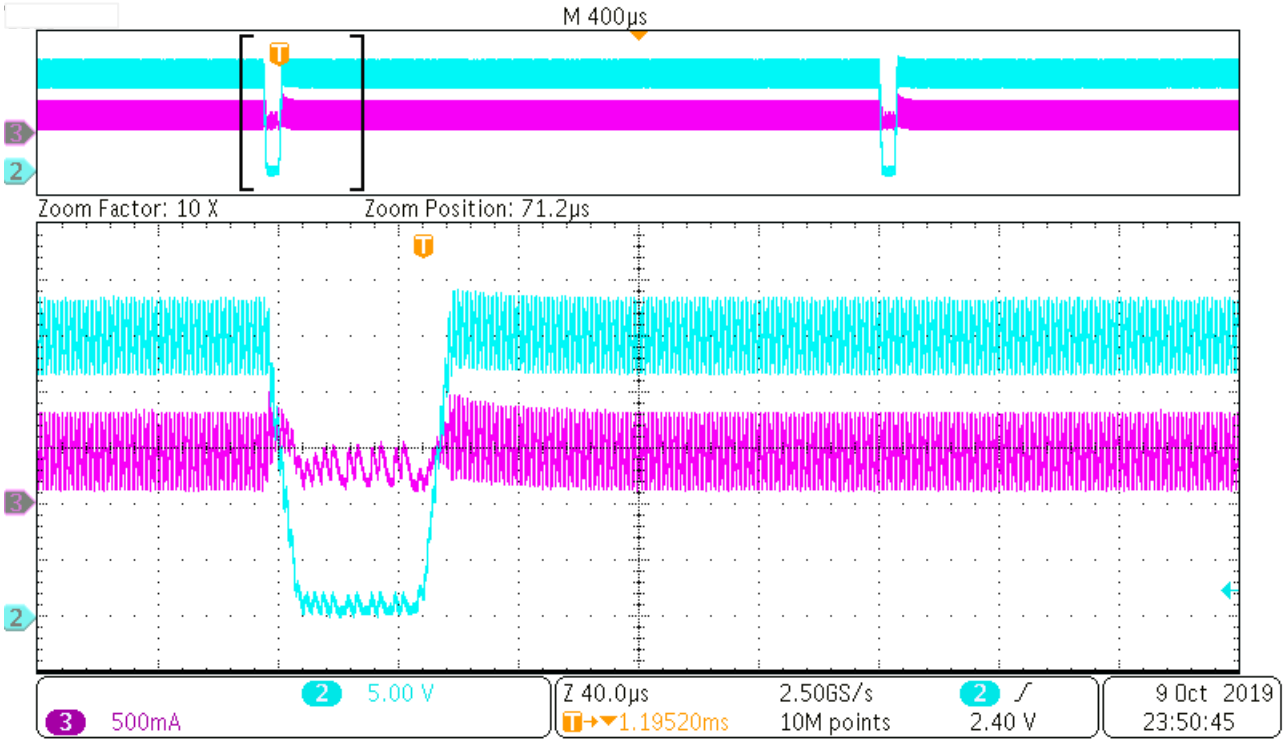
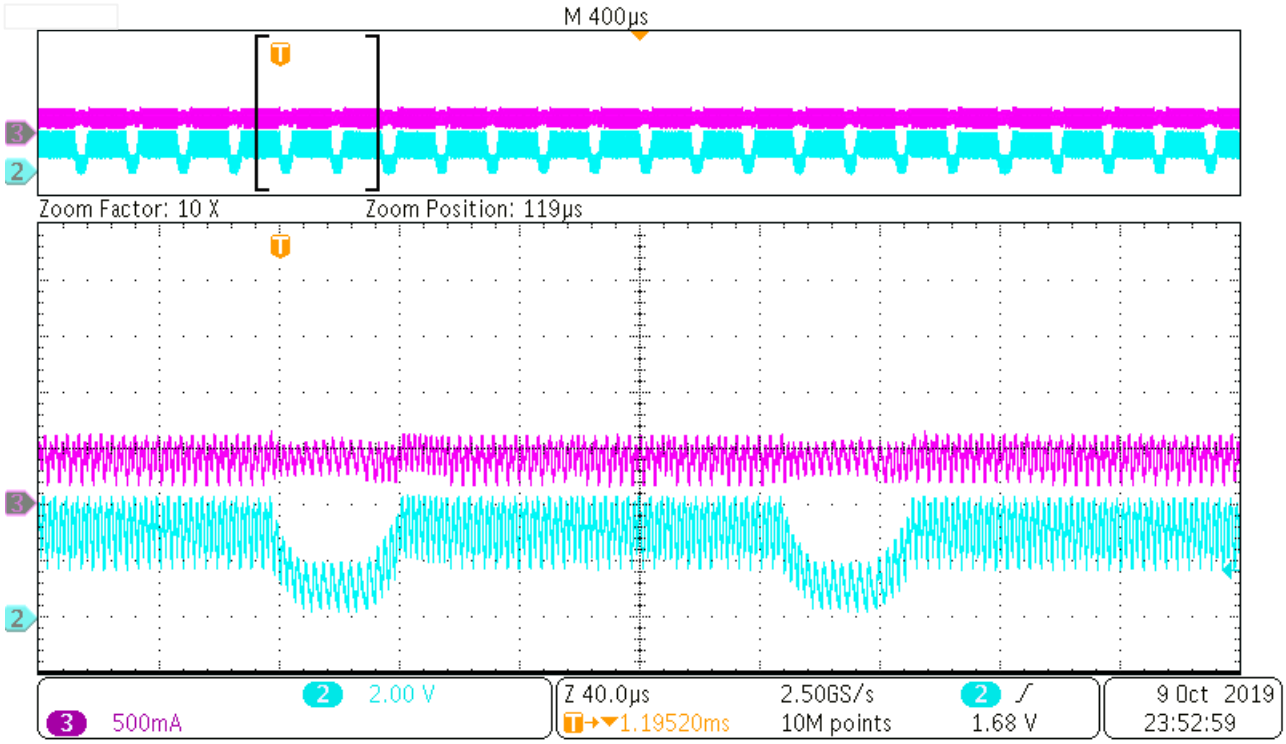


図 30. Waveforms of 85 Phase Shift, 70/1024 Pulse Width, SLEWRATE=01, at 350mA Using Lighting Matrix Module EVM



3.2.6 Electromagnetic Compatibility (EMC)

All tests in this section are performed according to the CISPR 25 standard. 図 31 shows the setup. Note that the test setup for conducted emissions is a worst case scenario where the LED driver PCB is placed 5 cm above the reference ground plane. In a real application housing, the distance from the LED driver PCB to the reference ground plane will be higher; thus, the common-mode noise coupling will be lower.

図 31. CISPR 25 Conducted Emissions Setup

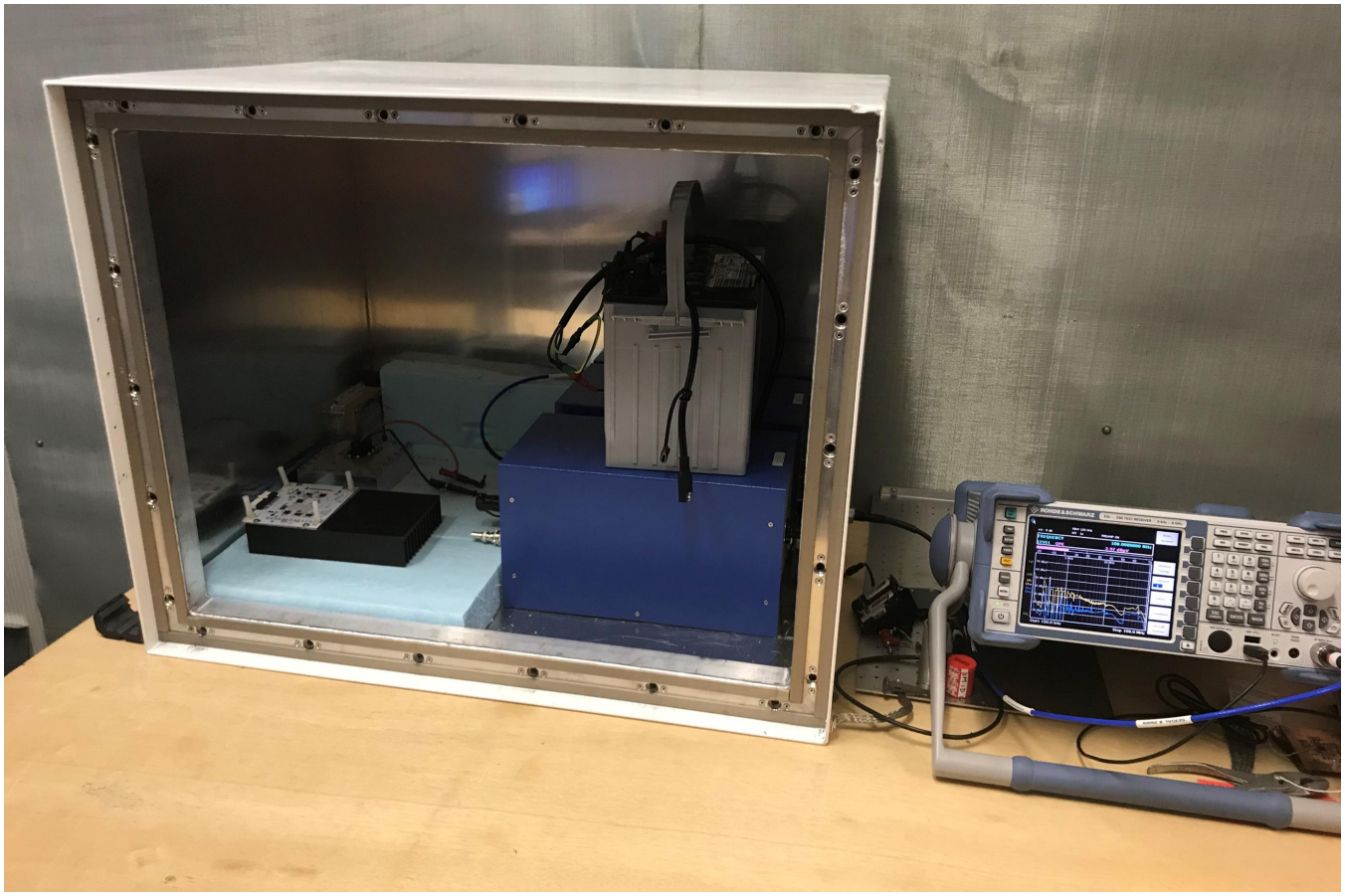
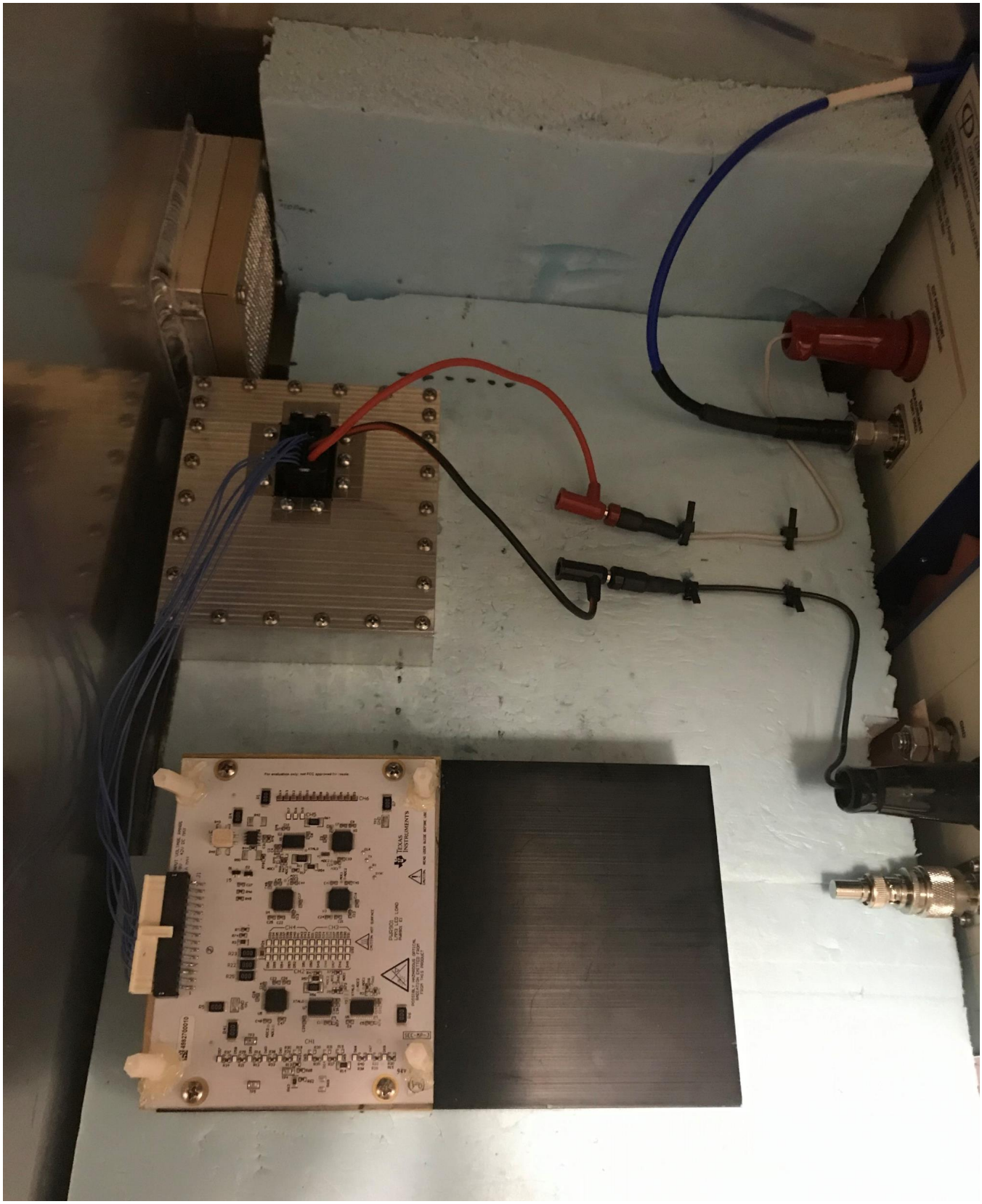


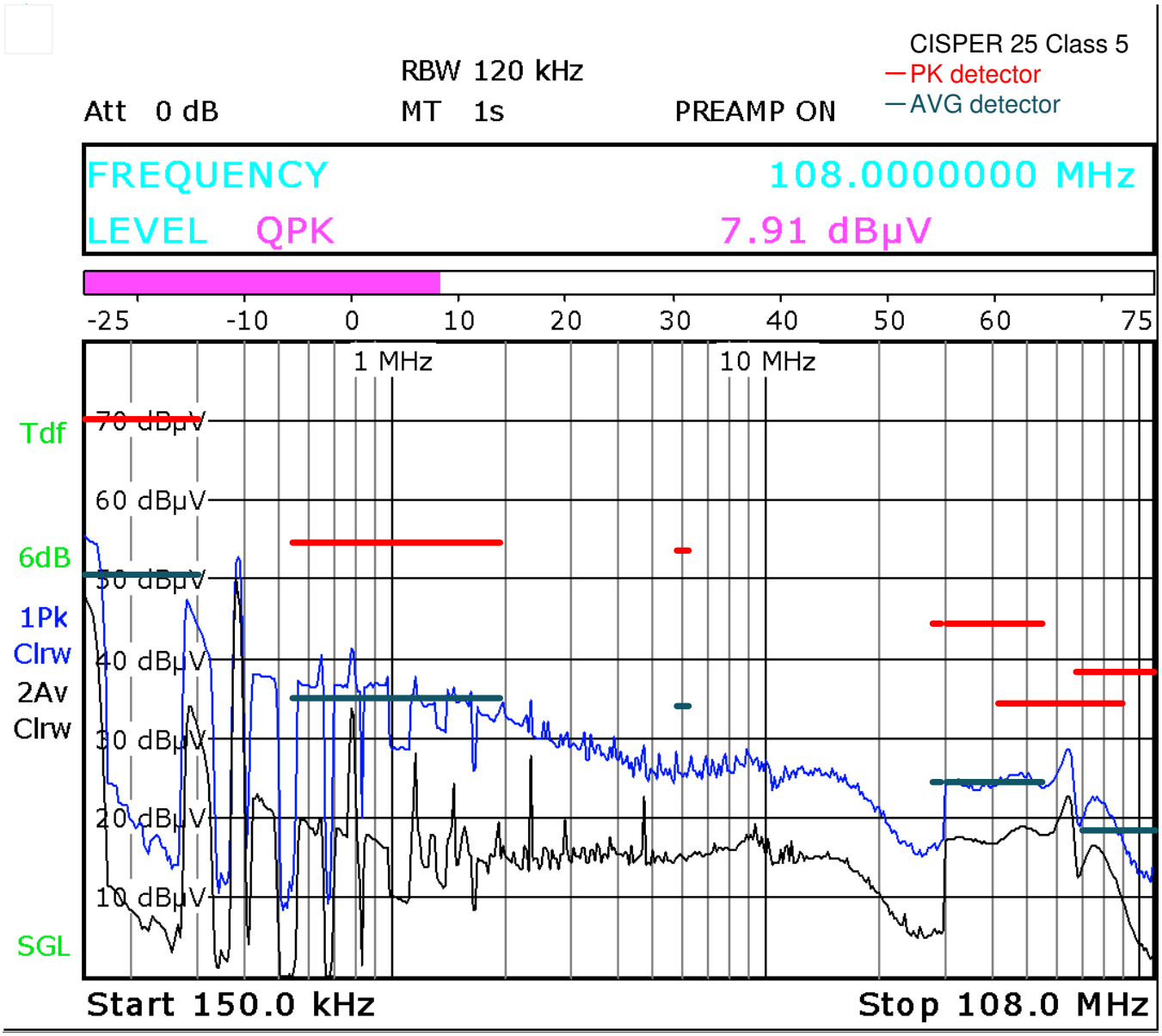
図 32. CISPR 25 Conducted Emissions Connections



3.2.6.1 Conducted Emissions

図 33 shows the conducted emissions at a power level of approximately 68 W with all four channels with 10 LEDs per channel. From 150 kHz to 30 MHz, the design is passing class 5.

図 33. Conducted Emissions: 0.15 MHz to 30 MHz, BUCK1, BUCK2, BUCK3, and BUCK4 on Ten LEDs (≈ 86 W)



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050030.

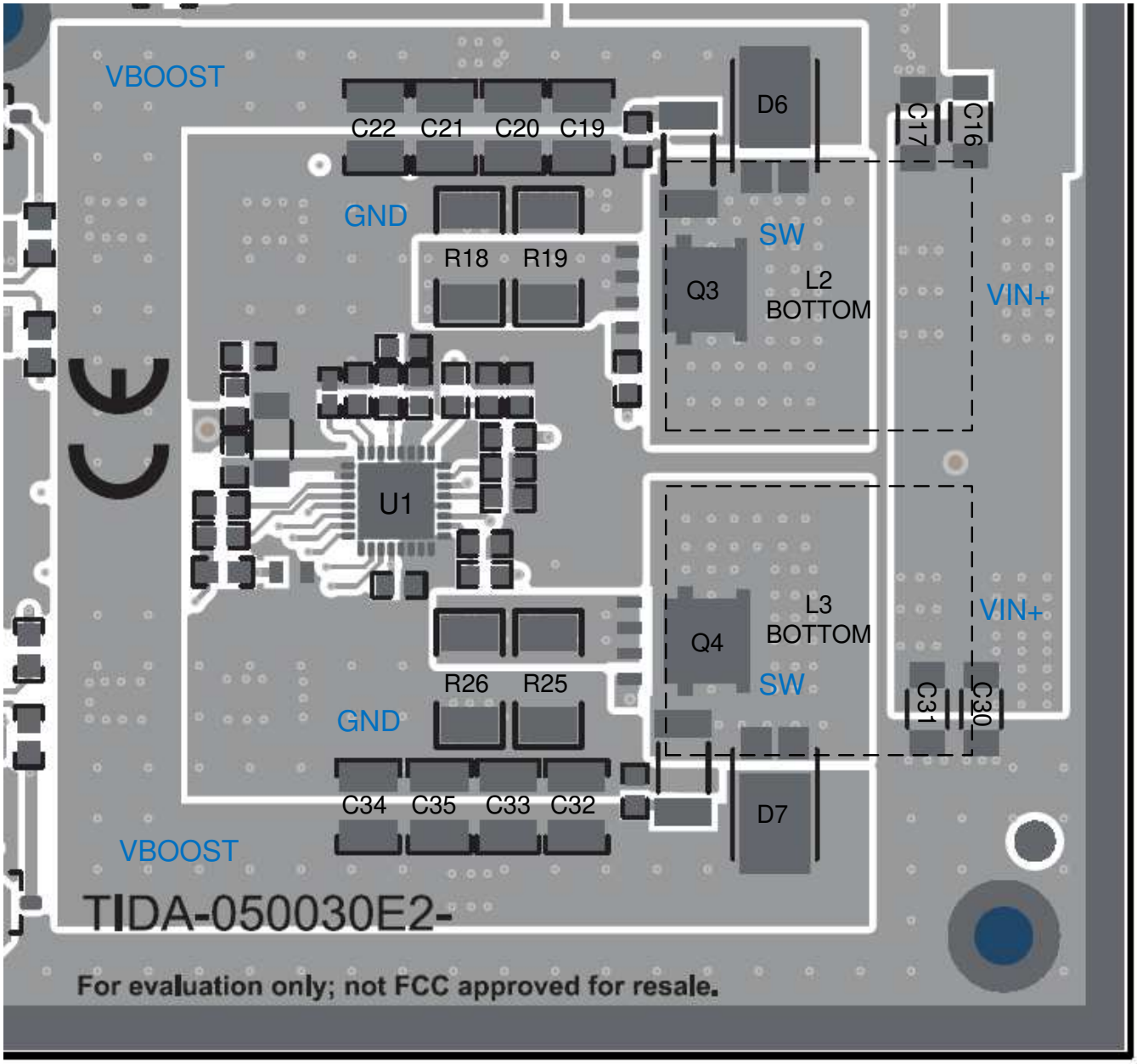
4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050030.

4.3 PCB Layout Recommendations

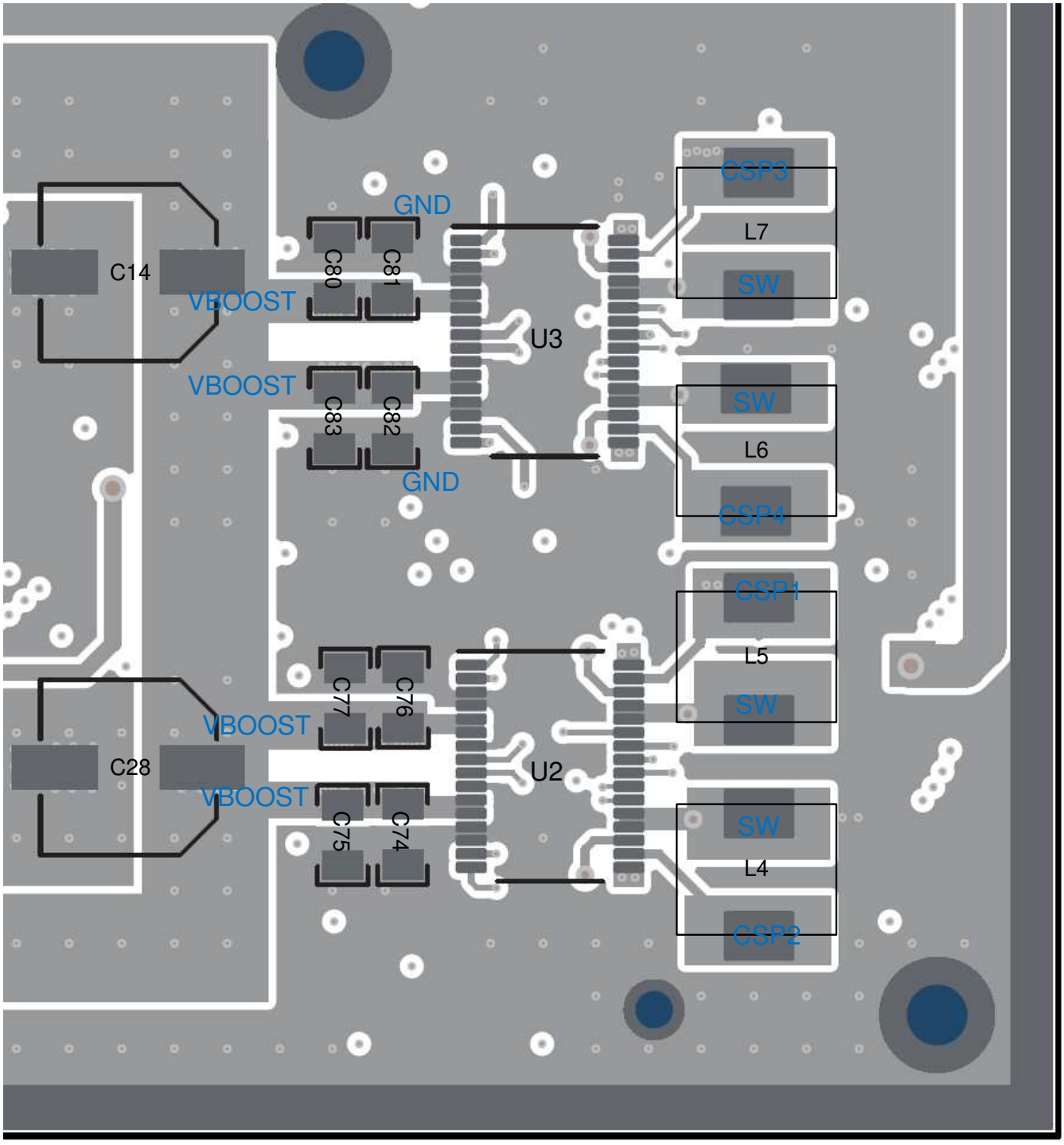
The layout of the boost controller as shown in 図 34 is created by following the layout example and guidelines in the Layout section of *TPS92682-Q1 Dual Channel Constant-Voltage and Constant-Current Controller with SPI Interface*.

図 34. TPS92682-Q1 Boost Controller Layout (Top Layer)



The layout of the buck converters as shown in 図 35 is created by following the layout examples and guidelines in the application note: *TPS92520-Q1 4.5V to 65V Input Dual 1.6-A Synchronous Buck LED Driver with SPI Control* or *AN-1229 SIMPLE SWITCHER PCB Layout Guidelines*.

図 35. TPS92520-Q1 Buck LED Drivers Layout (Bottom Layer)



4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050030.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-050030.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050030.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050030.

5 Related Documentation

1. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters Application Report*
2. Texas Instruments, *LM5122 Wide-Input Synchronous Boost Controller With Multiple Phase Capability Data Sheet*
3. TI E2E Community, *Power Tips: Calculate an R-C snubber in seven steps*
4. Texas Instruments, *AN-1889 How to Measure the Loop Transfer Function of Power Supplies Application Report*
5. Texas Instruments, *TPS92520-Q1 4.5V to 65V Input Dual 1.6-A Synchronous Buck LED Driver with SPI Control*
6. Texas Instruments, *PMP9796 - 5V Low-Power TEC Driver Reference Design*

5.1 商標

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年10月発行のものから更新 **Page**

- figure 28 title "Phase Margin" to "Phase Shift" 変更 29
- figure 29 title "Phase Margin" to "Phase Shift" 変更 29
- figure 30 title "Phase Margin" to "Phase Shift" 変更 30

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