参考資料

デザイン・ガイド：TIDA-010083
マシン・ビジョン・カメラおよびビジョン・センサ向け高密度、絶縁型 PoE / GigE のリファレンス・デザイン

概要

Power over Ethernet (PoE) は、ケーブル 1 本で電力とデータを伝送し、高いデータレートと長距離伝送を実現する簡単で信頼性の高いソリューションです。このため、PoE はマシン・ビジョン・カメラやビジョン・センサといった小型のデバイスに最適です。

このリファレンス・デザインは、1Gb/s 物理層 (PHY) と高効率の絶縁型電源ソリューションを 27 x 27mm の超小型フォーム・ファクタに搭載した完全な PoE 受電デバイス (PD) を実装するものです。

リソース

TIDA-010083	デザイン・フォルダ
TPS23758	プロダクト・フォルダ
DP83867IR	プロダクト・フォルダ
LM74700-Q1	プロダクト・フォルダ
TVS3300	プロダクト・フォルダ
ISO1212	プロダクト・フォルダ
TPS62801	プロダクト・フォルダ
TPS62802	プロダクト・フォルダ
TPD4E05U06	プロダクト・フォルダ
CSD17579Q3A	プロダクト・フォルダ
CSD19538Q2	プロダクト・フォルダ

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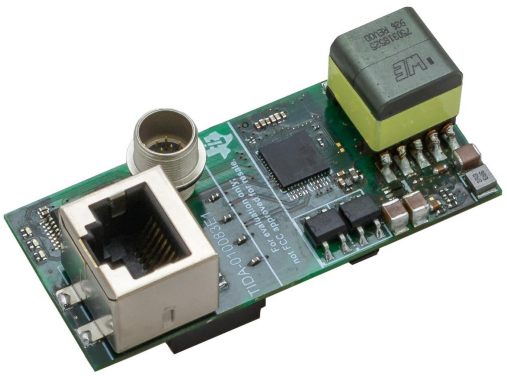
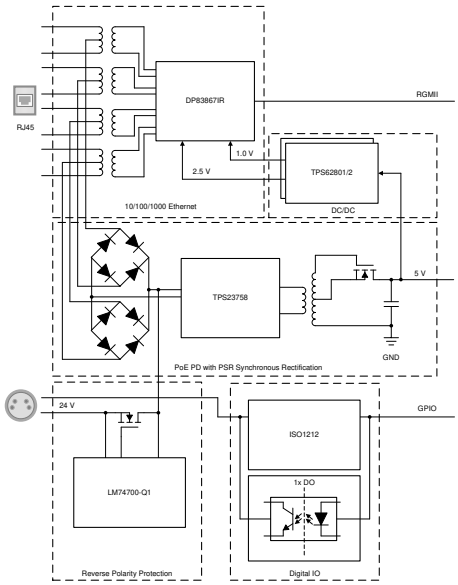


特長

- IEEE802.3 at PoE Type 1 PD Class 0：13W
- 同期整流式フライバック
  - フォトカプラなしの 1 次側帰還
  - 5V 出力、±2% 未満の精度
  - 最大 92% の効率
- 追加の 24V 補助入力
- 10/100/1000Mbit/s イーサネット
- RGMII インターフェイス
- 2x 絶縁型デジタル入力
- 1x 絶縁型デジタル出力
- 27 x 27mm の小型フォーム・ファクタ

アプリケーション

- ビジョン・センサ
- カメラ
- バーコード・リーダー



1 System Description

Machine vision is becoming more popular in factory automation, where cameras can not only read codes but also identify objects, conduct quality tests, and control processes. Because of these quality tests and control of processes, there is demand to have a 100% quality check for the production line.

A vision camera simply delivers a raw image of an object. Most modern vision cameras come in a very small footprint – 29 x 29 x 29 mm^3 – with all electronics, including the interfaces, located in this small housing. Complementary metal oxide semiconductor (CMOS) sensors used in such cameras are sensitive to heat. Their image quality degrades with higher temperatures, therefore it is important to keep the power dissipation low. The small housing leaves no room for a fan or heat sink and doesn't allow the dissipation of a lot of heat. It is still necessary to include a CMOS sensor and a field-programmable gate array (FPGA) or processor, as well as a high-speed interface and the necessary power supply. The electronic system must be able to capture, process, and transmit uncompressed video frames at high frame rates and resolutions. Gigabit Ethernet is widely used for these type of cameras as it is a reliable and very well supported interface.

An increasing amount of these devices make use of PoE. This offers the possibility to add power to the high speed Ethernet connection. This has the advantage to use one cable for power as well as for data connection with up to 100-m cable length at a data rate of up to 1000 Mbit/s. Such a camera requires the installation of only one standard Ethernet cable and can connect the camera without an additional cable for powering the camera. This combination of a widely used data interface together with power makes it very simple and reliable to setup a machine vision camera in the factory floor.

This reference design features a power solution which uses the available 13 W of input power to generate an isolated 5-V rail in a highly efficient way. The reference design also includes the Ethernet data transformer and PHY. Moreover, digital inputs and outputs are part of this design. The design has a small footprint of 27 x 27 mm^2.

This design consists of three major independent parts:

- The first part is the IEEE802.3at compliant Type 1 Class 0 PD with up to 13 W and a 5-V output voltage. The TPS23758 used here combines the PD controller as well as the flyback converter with an integrated switching MOSFET. The flyback converter uses primary side feedback, so an optocoupler or secondary shunt reference is not needed. To maintain a stable voltage over a wide load range and high efficiency, synchronous rectification is used.
- The second part is the Ethernet subsystem, including a data transformer and 10/100/1000 Mbit/s Ethernet PHY DP83867IR. In addition to the PHY, the necessary power and clock supply are also included on the board. Three status LEDs on the board show the link state of the PHY.
- As most systems also need some digital inputs and outputs, this design contains two isolated digital inputs and one digital output.

1.1 Key System Specifications

WARNING

Depending on the load and input voltages connected to this design, some components can reach high temperatures. See 3.4.1 for thermal images showing the hot spots. Overloading the circuit can result in overheating components and damaged parts.

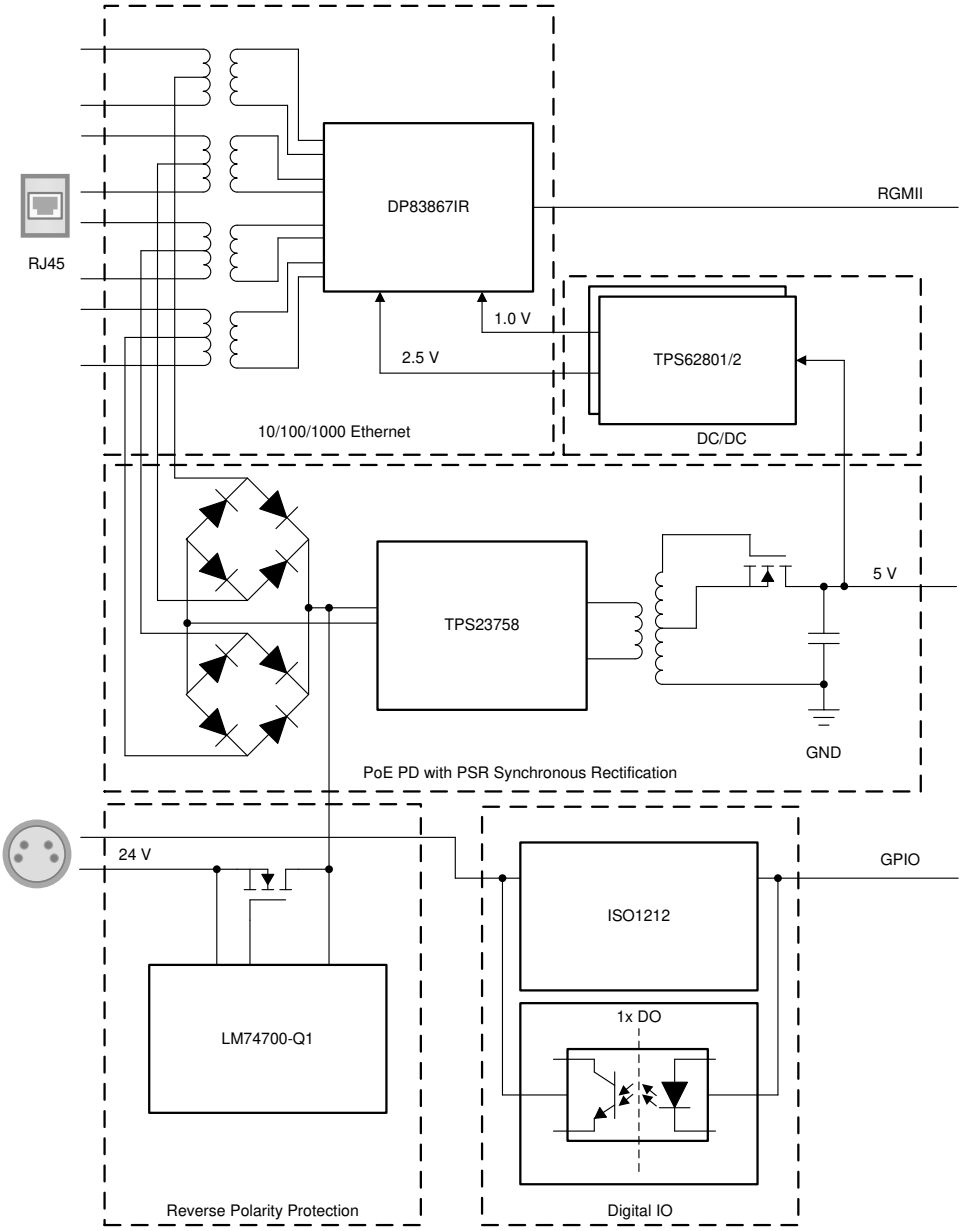
表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
PoE input voltage	36 - 57 V	2.4.1.2
Auxiliary input voltage	18 - 36 V	2.4.1.4
Isolated output voltage	5 V	2.4.1.2
Output current	Up to 2.3 A	2.4.1.2
Output voltage tolerance	< ±2 %	3.2.1
Efficiency	Up to 92%	
Maximum PoE power	13 W	2.4.1.1
PoE class	Type 1 Class 0	2.4.1.1
Isolation	Functional	
Data rate	10/100/1000 Mbit/s	2.4.2
Digital inputs	2x Isolated	2.4.3
Digital outputs	1x Isolated	2.4.3

2 System Overview

2.1 Block Diagram

図 1. TIDA-010083 Block Diagram



2.2 Design Considerations

The target of this design is a complete PoE PD with isolation as well as an Ethernet PHY for space-critical applications such as machine vision cameras, but also applications with the demand for higher peak power are covered.

This reference design is designed for a very small form factor of 27 x 27 mm². Because the area taken by the connectors and the data transformer is already in that range, it is split into two boards of that size. The two boards are connected together by a flex PCB in the middle and can be folded to fit into that small area. However, this reference design is not manufactured in that way as it would complicate testing and development. Instead, it is manufactured as a standard rigid PCB, so it can easily be tested.

One board contains the connectors to the outer world of the system, the RJ45 connector for Ethernet and an 8-pin connector for auxiliary power as well as digital inputs and outputs. Also on this board are the data transformer and a couple of status LEDs signaling the state of the Ethernet PHY.

The second board contains the rest of the subsystem, as well as a connector interfacing a processor or FPGA board. On this board, the complete PoE PD, including the diode bridges, filtering, PD controller, auxiliary input, and flyback, are located. Also, the Ethernet PHY with the necessary components such as DC/DC regulators and clock generation are on this board.

This reference design can be operated as a stand-alone design or together with a processor or FPGA board. For testing the data path in a stand-alone operation, the PHY can be placed in a loop-back mode to send back every received frame.

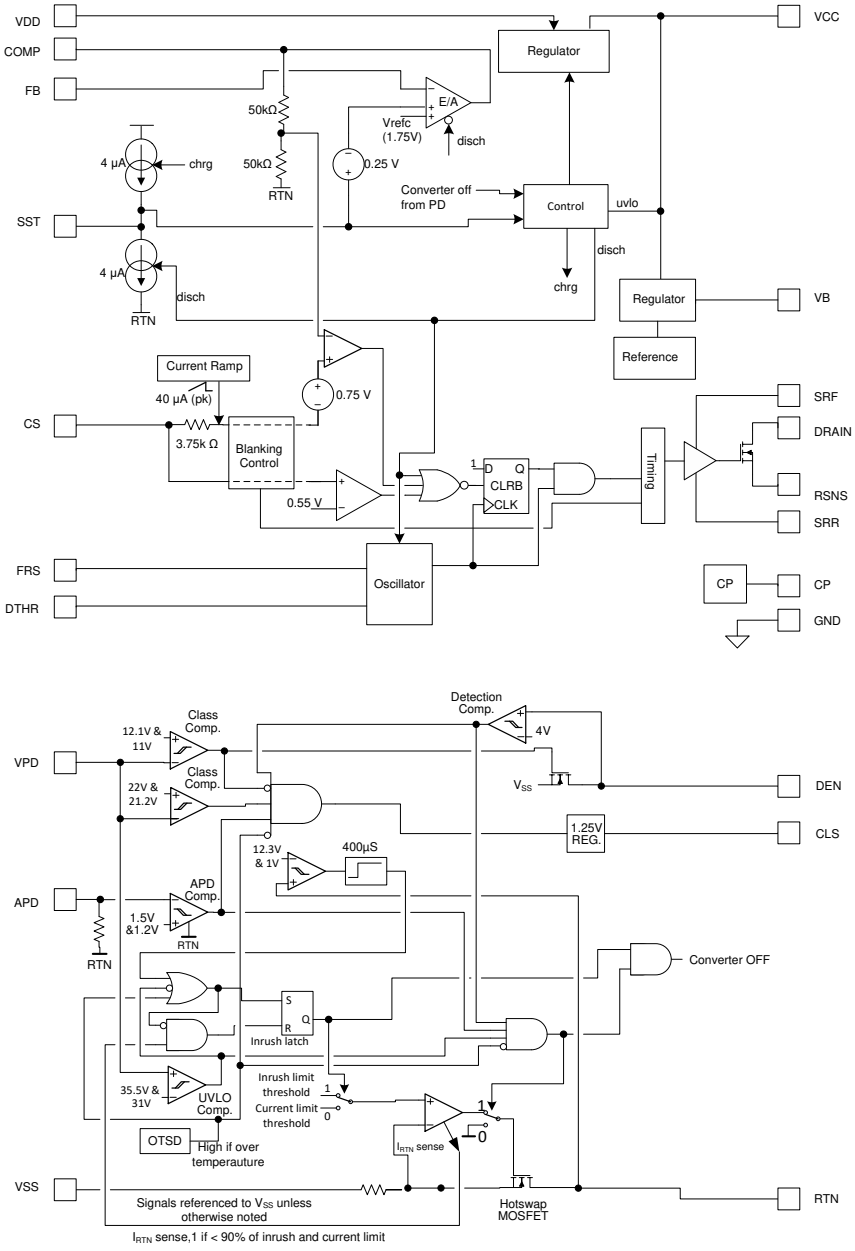
2.3 Highlighted Products

This section contains the most important parts used in the reference design, mentioning the most important technical data that make it suitable for this subsystem.

2.3.1 TPS23758

The TPS23758 device combines a Power over Ethernet (PoE) powered device (PD) interface, a 150-V switching power FET, and a current-mode DC-DC controller optimized for flyback topology. The high level of integration along with primary side regulation (PSR), spread spectrum frequency dithering (SSFD), and advanced startup makes the TPS23758 an ideal solution for size-constrained applications. The PoE implementation supports the IEEE 802.3at standard as a 13-W, Type 1 PD.

図 2. TPS23758 Block Diagram



Key features that make it suitable for this application:

- Complete IEEE 802.3at PD solution for type 1 PoE
- Robust 100-V, 0.36-Ω (typical) hotswap MOSFET
- Integrated PWM controller with 0.77-Ω (typical) 150-V power MOSFET
- Flyback controller with PSR
- Supports CCM operation with secondary side synchronous FET— multi-outputs
- ±1% (typical, 5-V output) load regulation (0-100% load range) — with Sync FET
- Primary adapter priority input

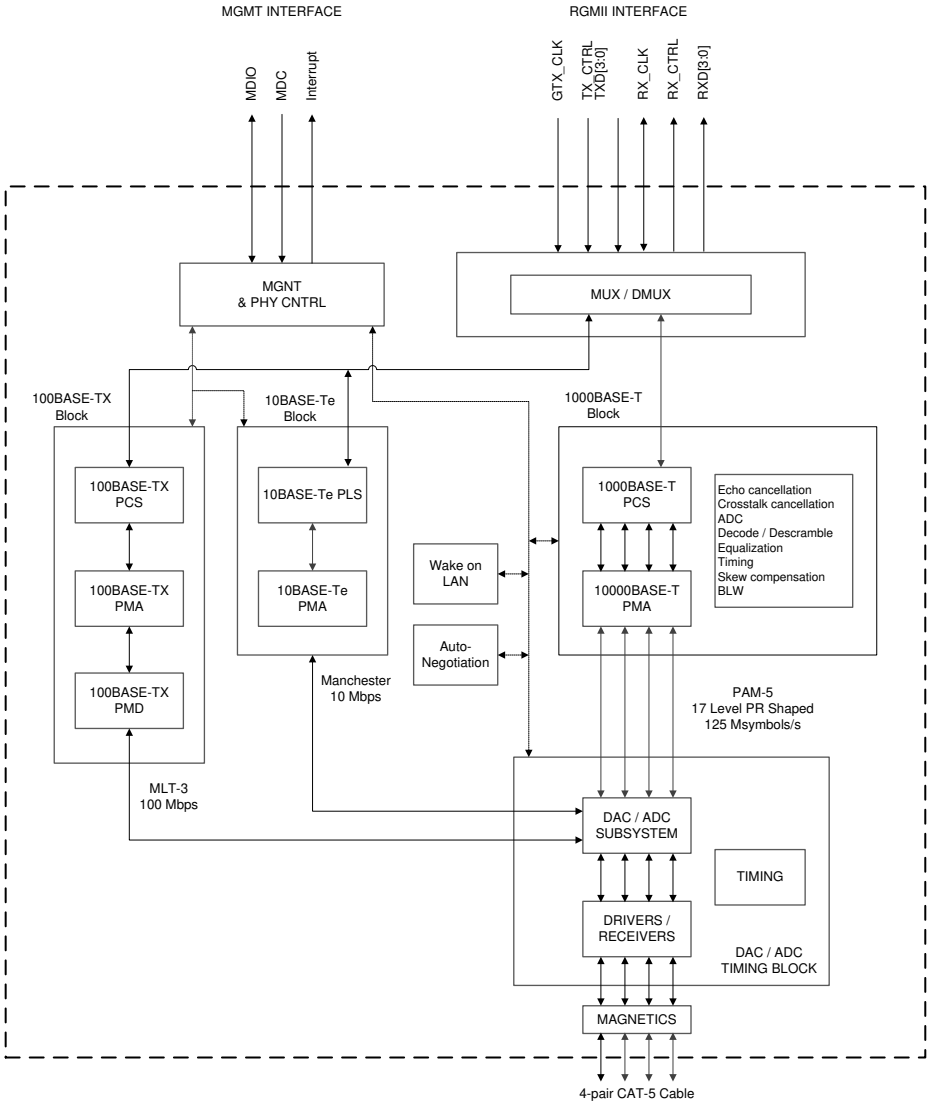
2.3.2 DP83867IR

The DP83867 device is a robust, low power, fully featured physical layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds 8-kV IEC 61000-4-2 (direct contact).

The DP83867 is designed for easy implementation of 10/100/1000 Mbps Ethernet LANs. It interfaces directly to twisted pair media through an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3 Standard Media Independent Interface (MII), the IEEE 802.3 Gigabit Media Independent Interface (GMII) or Reduced GMII (RGMII). The QFP package supports MII/GMII/RGMII whereas the QFN package supports RGMII.

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

図 3. DP83867IR Block Diagram



Key features that make it suitable for this application:

- Low power consumption of 457 mW
- Ultra low RGMII latency TX < 90 ns, RX < 290 ns

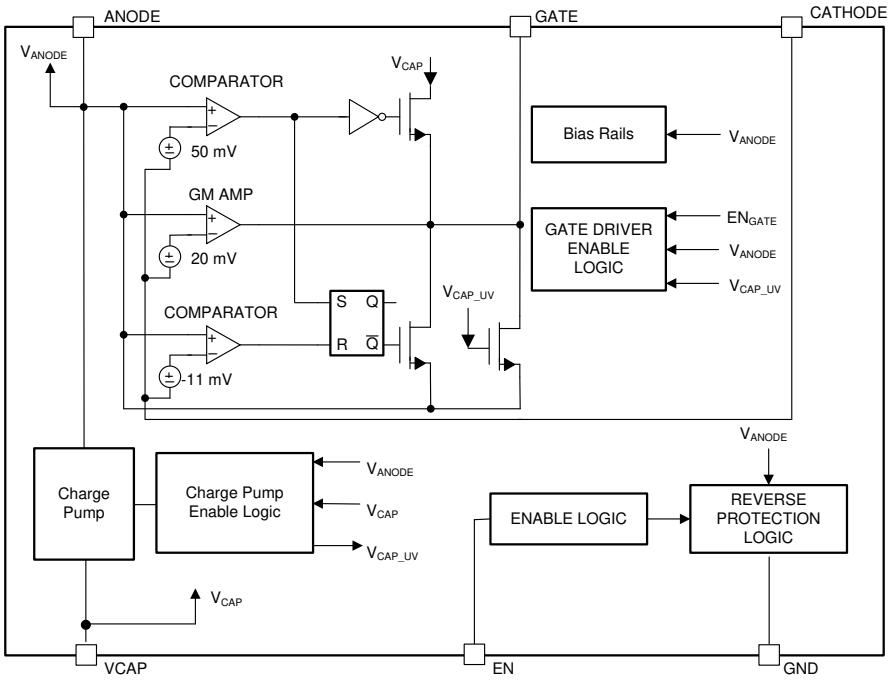
- Exceeds 8000-V IEC 61000-4-2 ESD protection
- Integrated MDI termination resistors
- Programmable MII/GMII/RGMII termination impedance
- IEEE 1588 time stamp support
- Fully compatible to IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T specification
- Configurable I/O voltage (3.3 V, 2.5 V, 1.8 V)

2.3.3 LM74700-Q1

The LM74700-Q1 ideal diode controller operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low-loss, reverse-polarity protection. The wide supply input range of 3 to 65 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from negative supply voltages down to –65 V. With a low $R_{DS(on)}$ external N-channel MOSFET, a very low forward voltage drop can be achieved while minimizing the amount of power dissipated in the MOSFET. For low-load currents, the forward voltage is regulated to 20 mV to enable graceful shutdown of the MOSFET. External MOSFETs with 5 V or lower threshold voltage are recommended. With the enable pin low, the controller is off and draws approximately 3 µA of current.

The LM74700-Q1 controller provides a charge pump gate drive for an external N-channel MOSFET. The high voltage rating of LM74700-Q1 helps to simplify the system designs for automotive ISO7637 protection. Fast response to reverse current blocking makes the device suitable for systems with output voltage holdup requirements during ISO7637 pulse testing, as well as power fail and brownout conditions. The LM74700-Q1 is also suitable for ORing applications or AC rectification.

図 4. LM74700-Q1 Block Diagram



Key features that make it suitable for this application:

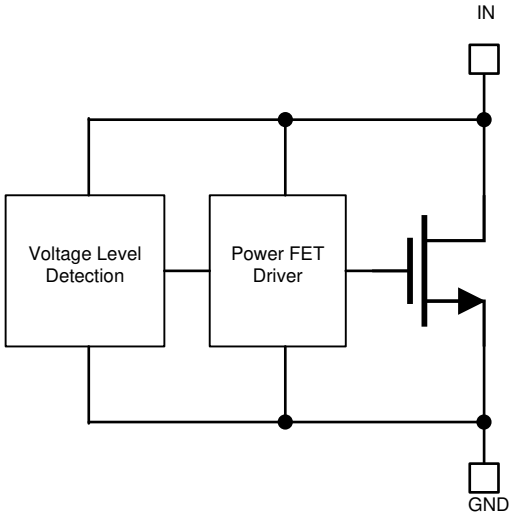
- 3.2-V to 65-V input range (3.9-V start up)
- –65-V reverse voltage rating
- Charge pump for external N-Channel MOSFET
- 20-mV ANODE to CATHODE forward voltage drop regulation
- 80-µA operating quiescent current (EN = High)
- Fast response to reverse current blocking: < 0.75 µs

2.3.4 TVS3300

The TVS3300 device robustly shunts up to 35 A of IEC 61000-4-5 fault current to protect systems from high-power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to 1-kV IEC 61000-4-5 open circuit voltage coupled through a 42-Ω impedance. The TVS3300 device uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 40 V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

In addition, the TVS3300 is available in small 1 mm × 1.1 mm WCSP and 2 mm × 2 mm SON footprints which are ideal for space-constrained applications, offering up to a 90 percent reduction in size compared to industry standard SMA and SMB packages. The extremely low device leakage and capacitance ensure a minimal effect on the protected line. To ensure robust protection over the lifetime of the product, TI tests the TVS3300 against 4000 repetitive surge strikes at high temperature with no shift in device performance.

図 5. TVS3300 Block Diagram



Key features that make it suitable for this application:

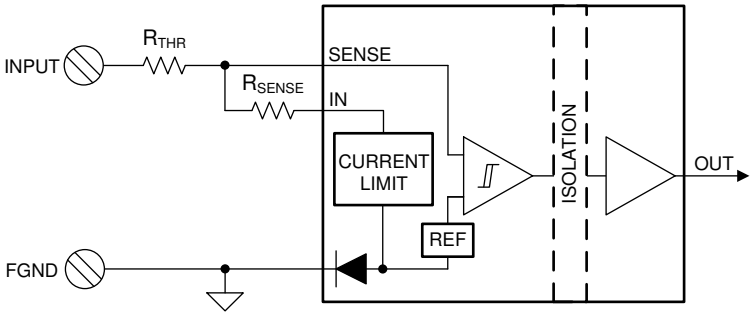
- Protection against 1-kV, 42-Ω IEC 61000-4-5 surge test for industrial signal lines
- Maximum clamping voltage of 40 V at 35 A of 8/20-µs surge current
- Standoff voltage: 33 V
- Low leakage current: 19 nA typical at 27°C
- Low capacitance: 130 pF
- Integrated level 4 IEC 61000-4-2 ESD protection

2.3.5 ISO1212

The ISO1211 and ISO1212 devices are isolated 24-V to 60-V digital input receivers, compliant to IEC 61131-2 Type 1, 2, and 3 characteristics. These devices enable 9-V to 300-V DC and AC digital input modules in programmable logic controllers (PLCs), motor-control, grid infrastructure, and other industrial applications. Unlike traditional optocoupler solutions with discrete, imprecise current limiting circuitry, the ISO121x devices provide a simple, low-power solution with an accurate current limit to enable the design of compact and high-density I/O modules. These devices do not require field-side power supply and are configurable as sourcing or sinking inputs.

The ISO121x devices operate over the supply range of 2.25 V to 5.5 V, supporting 2.5-V, 3.3-V, and 5-V controllers. A ±60-V input tolerance with reverse polarity protection helps ensure the input pins are protected in case of faults with negligible reverse current. These devices support up to 4-Mbps data rates passing a minimum pulse width of 150 ns for high-speed operation. The ISO1211 device is ideal for designs that require channel-to-channel isolation and the ISO1212 device is ideal for multichannel space-constrained designs.

図 6. ISO1212 Block Diagram



Key features that make it suitable for this application:

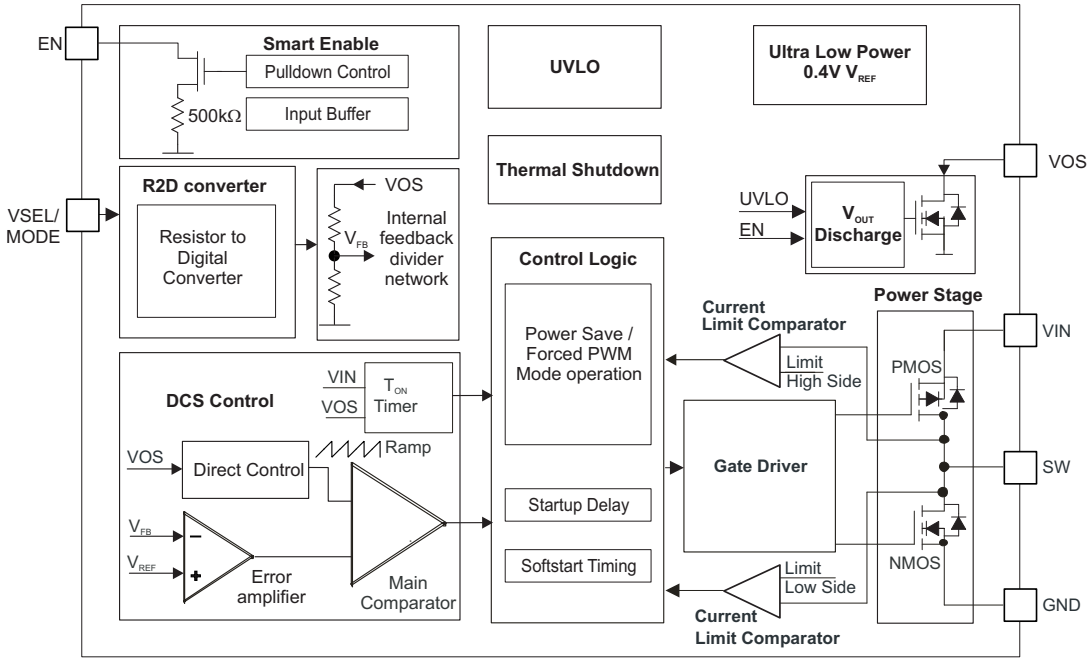
- Compliant to IEC 61131-2; type 1, 2, 3 characteristics for 24-V isolated digital inputs
- Supports 9-V to 300-V DC and AC digital input designs using external resistors
- Accurate current limit for low-power dissipation:
  - 2.2 mA to 2.47 mA for type 3
  - Adjustable up to 6.5 mA
  - High input-voltage range with reverse polarity protection: ±60 V
  - High data rates: up to 4 Mbps
  - Wide supply range (VCC1): 2.25 V to 5.5 V
  - UL 1577 recognition, 2500-VRMS insulation

2.3.6 TPS62801/2

The TPS6280x device family is a step down converter with 2.3-µA typical quiescent current featuring highest efficiency and smallest solution size. TI's DCS-Control™ topology enables the device to operate with tiny inductors and capacitors with a switching frequency up to 4MHz. At light load conditions, it seamlessly enters Power Save Mode to reduce switching cycles and maintain high efficiency.

Connecting the VSEL/MODE pin to GND selects a fixed output voltage. With only one external resistor connected to VSEL/MODE pin, 16 internally set output voltages can be selected. An integrated R2D (resistor to digital) converter reads out the external resistor and sets the output voltage. The same device part number can be used for different applications and voltage rails just by changing a single resistor. Furthermore, the internally set output voltage provides better accuracy compared to a traditional external resistor divider network. Once the device has started up, the DC/DC converter enters Forced PWM Mode by applying a high level at the VSEL/MODE pin. In this operating mode, the device runs at a typical 4-MHz or 1.5-MHz switching frequency, enabling lowest output voltage ripple and highest efficiency. The TPS6280x device series comes in a tiny 6-pin WCSP package with 0.35-mm pitch.

図 7. TPS62801/2 Block Diagram



Key features that make it suitable for this application:

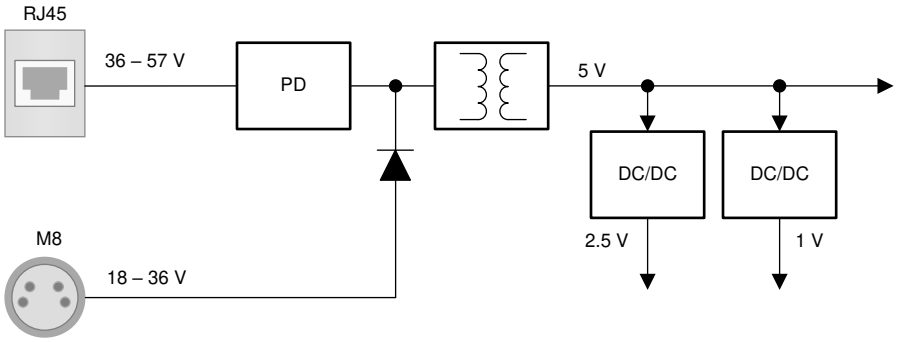
- Input voltage range from 1.8 V to 5.5 V
- 2.3-µA operating quiescent current
- Up to 4-MHz switching frequency
- R2D converter for flexible V_{OUT} setting
- Output discharge
- 100% duty cycle operation

2.4 System Design Theory

This reference design consists of three major parts that will be discussed here: The Power over Ethernet (PoE) powered device (PD), the Ethernet physical layer (PHY), and the digital IO.

2.4.1 Power Tree

図 8. Power Tree of the TIDA-010083



This reference design has two different power supply inputs. One power option is Power over Ethernet (PoE), and the other option is an auxiliary voltage input. These two power inputs are multiplexed to power a flyback converter. If both power sources are present, the auxiliary power is prioritized. The flyback is configured to a regulated output voltage of 5 V that can be used to power a system. Moreover, this 5-V rail is used to generate two additional voltages, necessary to supply the Ethernet physical layer (PHY). 図 9 gives an overview of the power tree.

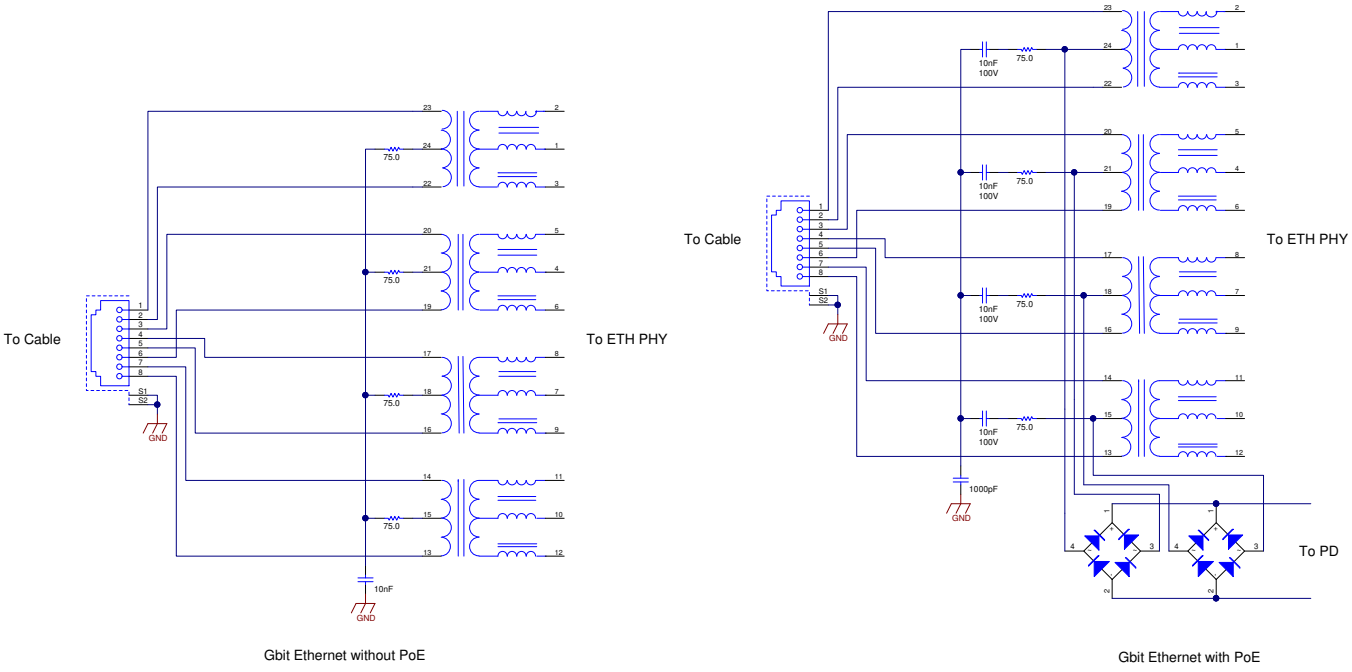
The details about this power solution will be discussed in the following sections.

2.4.1.1 Powered Device

Adding PoE to a gigabit Ethernet system requires some modifications. The schematic on the left side of 図 10 shows how the transformer is usually connected to the cable in a gigabit configuration. All of the middle taps of the transformers are connected to each other through a 75-Ω resistor and to ground (GND) by a capacitor. This circuit is typically called the Bob Smith termination. This circuit does not allow power to be added between the differential pair because it acts as a short.

To create the ability to inject power, adding one capacitor per middle tap interrupts the DC path. Because the DC path is no longer shorted, a DC voltage can be applied symmetrically between each differential pair. In total, it is possible to have up to four power lines. These lines go to the powered device (PD) controller over two rectifier bridges. By using a rectifier, the polarity, as well as the pairs used, does not matter.

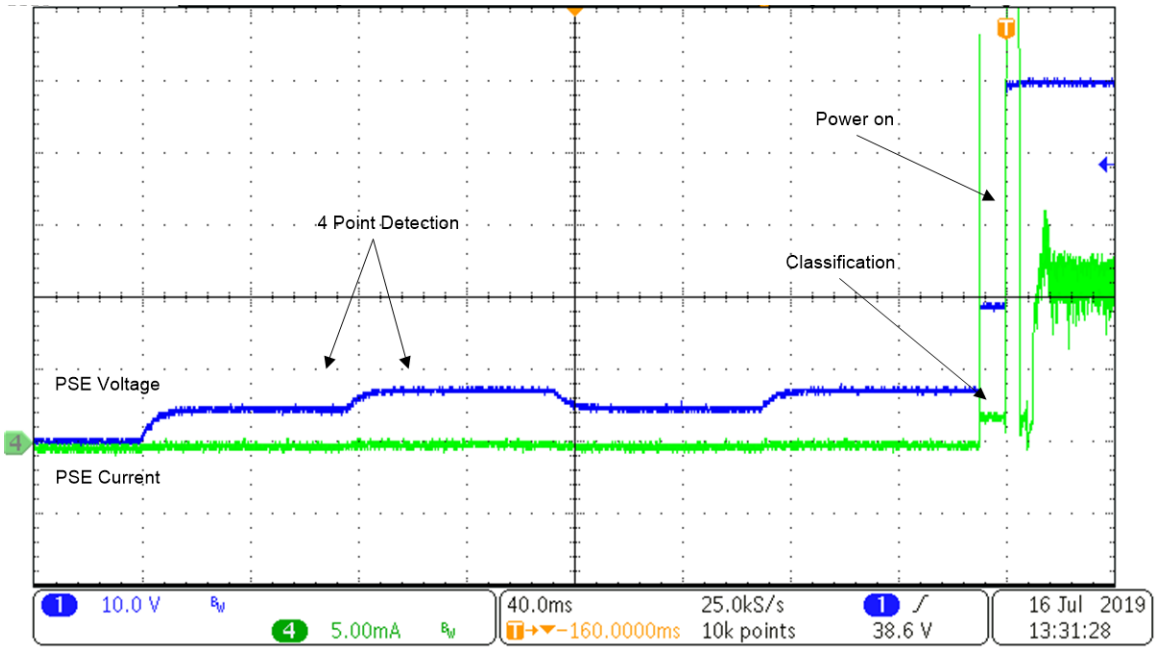
図 9. Ethernet Transformer Connection



The device delivering power, the power sourcing equipment (PSE), must ensure that a PoE-capable PD is connected before powering it so as not to damage it. There are a few passive PoE implementations on the market that just connect a power supply to the middle tap of a transformer without any detection. This works when used with a proper PoE PD but could damage anything else.

When connecting a PD to a PSE, the first step is detection by the PSE. During this step, a low voltage drop of 2.7 V and 10.1 V over the PD is used for sensing a signature resistor. 図 11 shows the complete procedure of an IEEE 802.3af-compliant class 0 PD. The detection of the signature resistance (in the range of 19 kΩ - 26.5 kΩ) occurs over four steps to make it robust.

図 10. PoE Detection and Classification

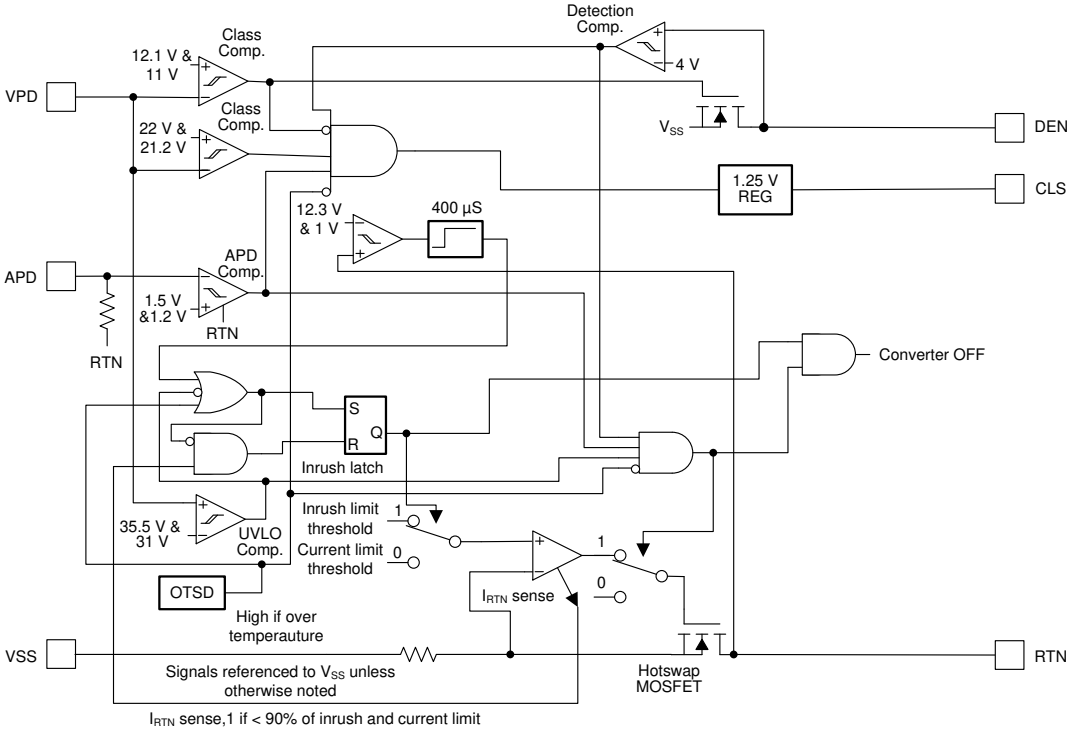


After correct detection of the signature, the classification starts. The PSE increases the voltage to a level of 14.5 V to 20.5 V. The PD then must draw a constant current to signal its power needs. A current of 0 mA is a valid classification here – meaning Class 0 or a non-implemented classification – which translates to 15.4 W of power coming from the PSE.

The example in 図 11 starts with a voltage between 5 V and 8 V. During this time, the signature is detected. After successful detection, the voltage increases to 19 V, and the PD draws a current of 2 mA. The PSE now knows that there is a class 0 device connected and will provide up to 15.4 W. The PSE turns on the full supply voltage, which can be between 37 V and 57 V.

In 図 12, the implementation of this part in the TPS23758 is shown. The rectifier coming from the RJ45 connector and data transformer is connected between VPD and VSS. During detection and classification, the hot swap MOSFET is open and no current can flow into the remaining circuit, so the IC can switch on either the detection resistor or the classification current sink. When the voltage rises to operating voltage, the internal hot swap MOSFET gets turned on, and the circuit connected between VPD and RTN can operate.

図 11. Block Diagram of the TPS23758 PD Part



The schematic in 図 13 shows how the PD must be configured. The resistor R20 is necessary for the detection phase. Typically a 24.9-kΩ resistor is placed to VPD. However, depending on the rectification diode that is used, it can be necessary to change this, especially when using Schottky diodes for lower voltage drop and so higher efficiency this resistor might be increased. Schottky diodes have a higher leakage current that can cause problems. TI recommends observing the leakage current over temperature to ensure that the detection resistance is in a valid range over the whole desired temperature.

Resistor R29 defines the current in the classification phase. Depending on the power class that is desired, this resistor must be selected. 表 2 gives an overview of the different classes that this design and an IC can be used for as well as the recommended current ranges. By default, this reference design has assembled a 649-Ω resistor and is therefore being detected as a class 0 powered device with up to 15.4 W from the PSE, meaning that the PD can draw up to 13 W.

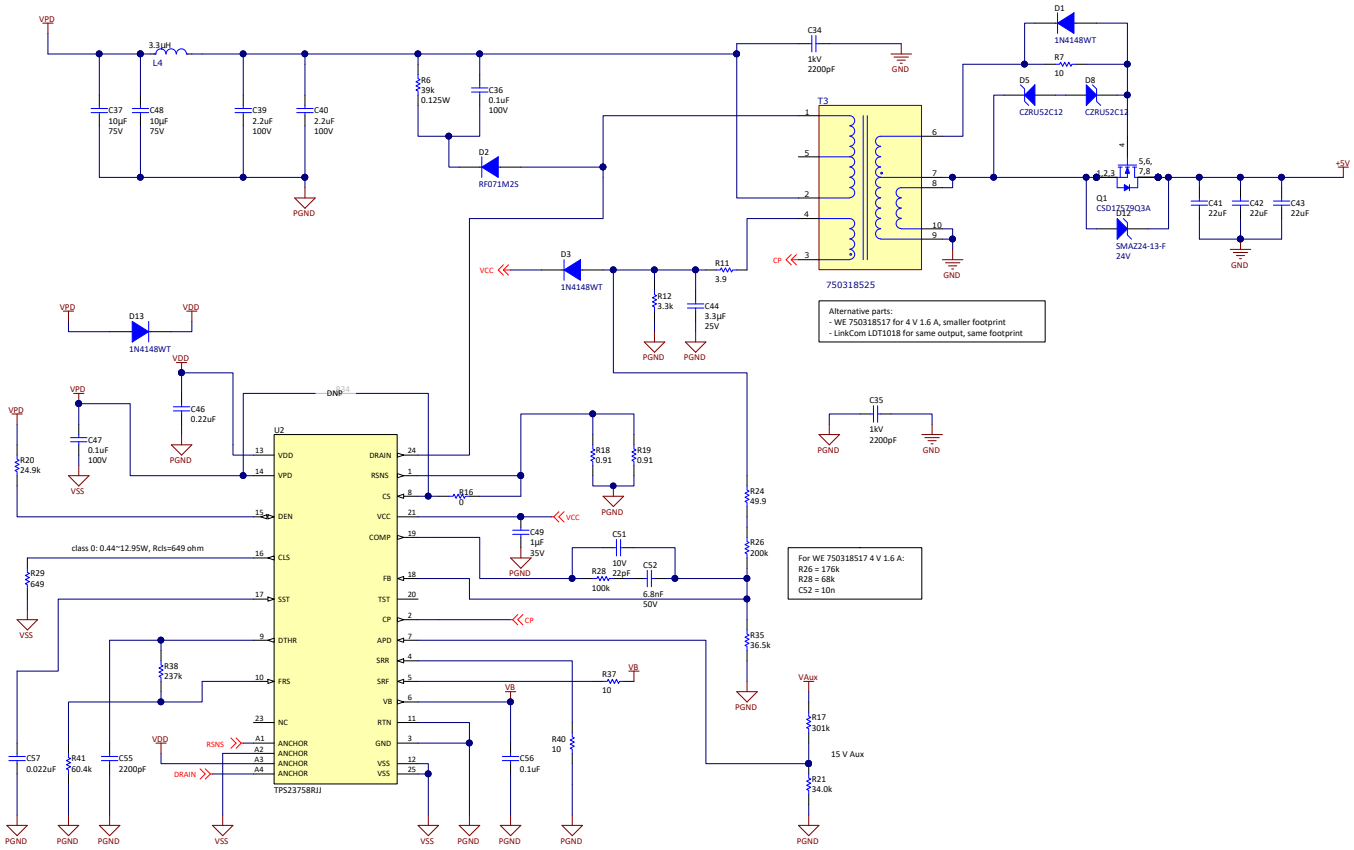
表 2. Classification Current and Resistor Selection

CLASS	CLASSIFICATION CURRENT ACCORDING TO 802.3af (mA)	RECOMMENDED CLS RESISTOR (Ω)	TPS23758 CLASSIFICATION CURRENT (mA)	MAXIMUM POWER FROM THE PSE
0	0 - 4	649	1.8 - 2.4	15.4
1	9 -12	121	9.9 - 11.3	4
2	17 - 20	68.1	17.6 - 19.4	7
3	26 - 30	45.3	26.5 - 29.3	15.4

2.4.1.2 Flyback

The next relevant functional block is the flyback, generating a regulated isolated voltage from the PSE voltage. When operating from PoE power, the PD controller passes through a voltage roughly in the range between 36 V and up to 57 V. When operating from the auxiliary 24-V input, a voltage range of 18 V up to 36 V is specified. This leads to an overall voltage range of 18 V to 57 V for the flyback converter to operate. When designing the transformer and the power stage, the whole voltage range must be considered. However, the output power must be reduced when operating from the auxiliary input to limit the power dissipation to a reasonable level.

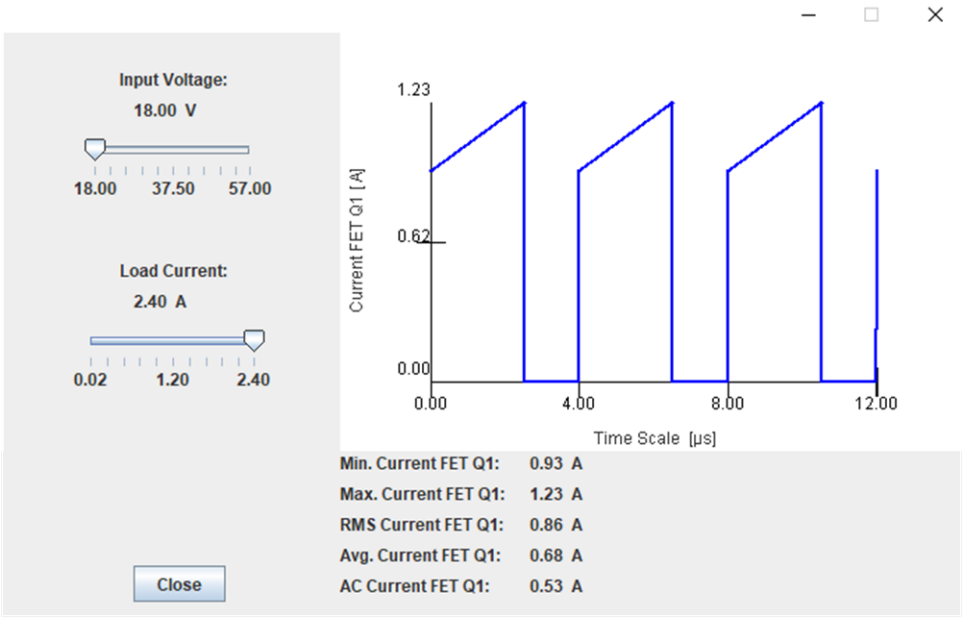
図 12. Schematic of the PD and Flyback



The transformer shown in the schematic has a turn ration of 6:1 primary to secondary and a primary inductance of 150 µH. Together with the desired voltage range output voltage and current, the primary switch current can be calculated. The switch current is at the highest level at maximum load current and lowest input voltage, so this worst case is used for designing the power stage.

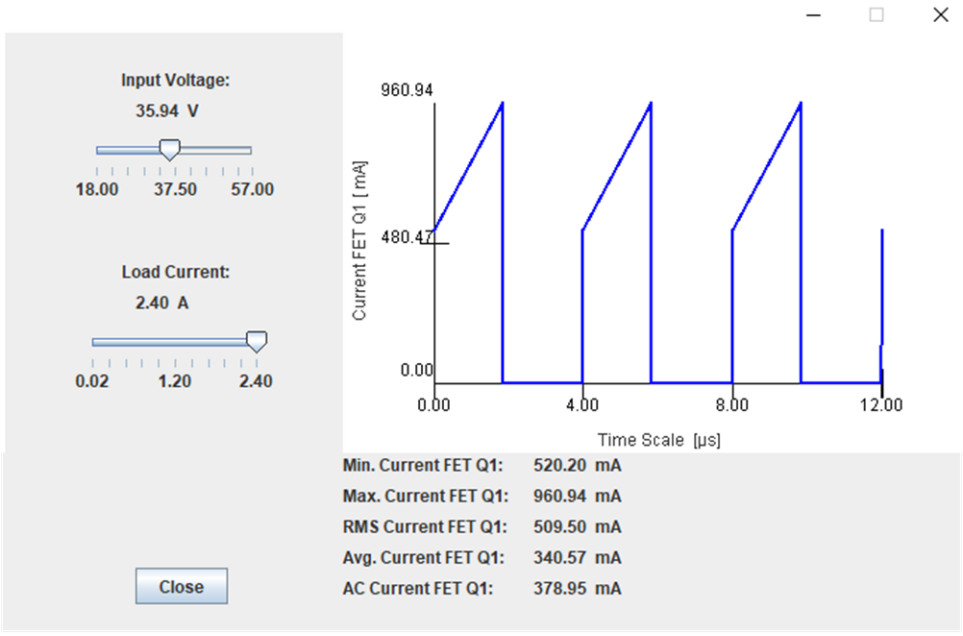
In 図 14, this is done for a 5-V output at 2.4 A at a 18-V input voltage. It can be seen in 図 13 that the peak current is at 1.23 A and the RMS current is at 0.86 A. Because the MOSFET of the flyback is integrated into the TPS23758 device, the designer has to take care not to overload it. The data sheet specifies a maximum peak current of 1.6 A, so this is acceptable. For estimating the static losses in the FET ($1.28\ \Omega \times 0.86^2\ A^2 = 0.95$ W) shows that already the power dissipation caused by the static losses is quite high for a small QFN IC with a thermal resistance of 34.7 K/W. It is not recommended to operate the device at these parameters, especially as the PCB size and therefore the area for heat dissipation is very limited.

図 13. Flyback for 5-V, 2.4-A Input Voltage Set to 18 V



Checking the same conditions at a higher input voltage of 36 V, as shown in 図 15, shows much better results. The peak current is as expected well within the allowed range. The RMS current is with 0.5 A much lower, yielding to a power dissipation of 0.3 W. This can be handled much better.

図 14. Flyback for 5-V, 2.4-A Input Voltage Set to 36 V



The current limit of the IC is configured with the resistors R18 and R19. The current limit is set to a peak current of 1.3 A to have some headroom: 0.6 V / 1.3 A = 0.46 Ω. To handle the power dissipation, two resistors are connected in parallel.

The feedback path of this regulator is realized by measuring the voltage of the auxiliary winding. This makes it necessary to have a good coupling between the auxiliary winding and the output voltage to see a good representation of the output voltage. Also, the turns ratio between auxiliary and output must be designed accordingly. The voltage divider R26 and R35 defines the voltage on the auxiliary winding and therefore the output voltage. In this design, the auxiliary voltage is set to ((200 kΩ / 36.5 kΩ) + 1) × 1.75 V = 11.3 V. This results in an output voltage of 11.3 V × 2.66/6 = 5.02 V. When designing for another output voltage, the designer must ensure that the auxiliary voltage is in a valid range and that the turns ratio meets the requirements.

For smaller output power, a smaller transformer can be used. This design is also tested with a 7-W transformer with smaller mechanical size. See 3.2.1.3 for the test results with a 4-V, 7-W solution. For applications requiring even less power, a transformer for 3 W can be designed, which is even smaller than the 7-W solution.

2.4.1.3 Sync Rectification

When using a diode rectification at the output of a primary-side regulated flyback, the output voltage changes depending on the load. At a very low load, the regulator operates in discontinuous conduction mode (DCM), and the diode rectifies the peak voltage at the output, resulting in a higher voltage. With an increasing load, the voltage drops, as the forward voltage of the diode is depending on the current. Moreover, the output voltage is temperature-dependent. All of these effects have a rather low impact on the voltage. However, this can be especially true at low output voltages, such as 5 V or 3.3 V, which are already too high. The power dissipation of the diode can be a reason to use a synchronous approach.

For low-output voltages, the synchronous rectification is a good approach to get a stable voltage over the full load range. This type of rectification forces the converter to always stay in continuous conduction mode (CCM) and therefore always operate at the same duty cycle independent of the load at the output.

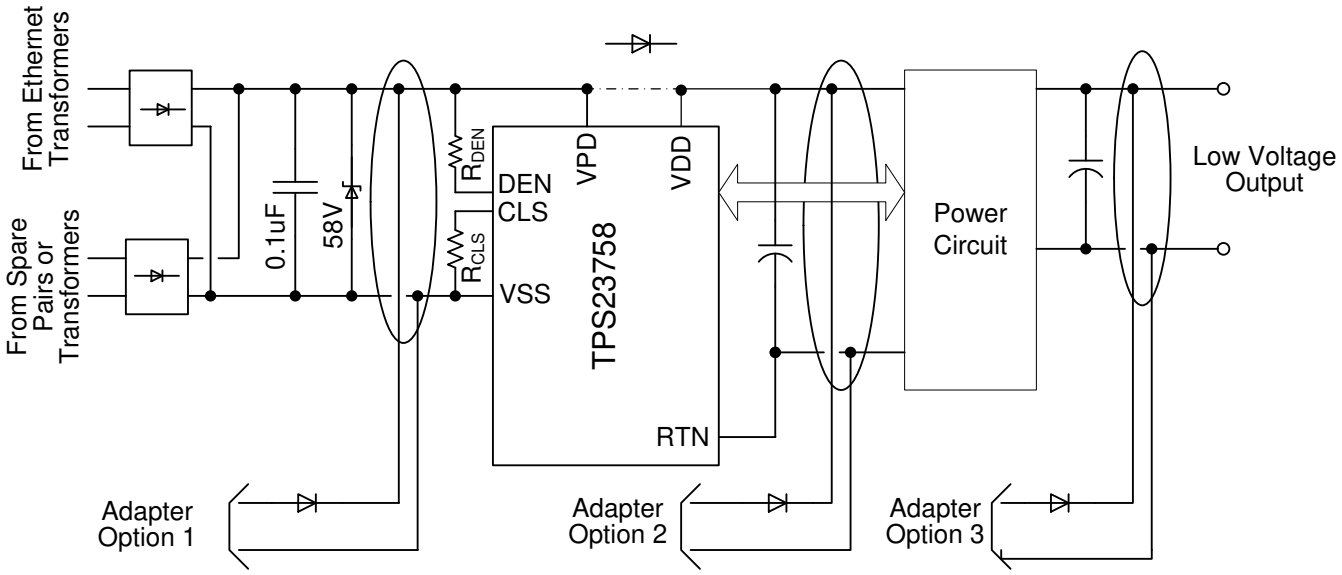
The MOSFET for rectification is driven by an additional winding on the transformer, and the gate drive can be implemented in a simple way. The gate-source voltage is limited by two Zener diodes, D5 and D8, to not exceed the maximum allowed voltages. The gate is charged through a resistor to control the slew rate and is turned off through a diode to turn off fast and reduce shoot through.

For selecting the MOSFET, a device with very low gate charge and that is slightly higher on resistance is a good choice, as most losses are caused by delayed turn on and off.

2.4.1.4 Auxiliary Power

Adding an option for external power can be done in different ways. 図 16 gives an overview of the different options that are possible.

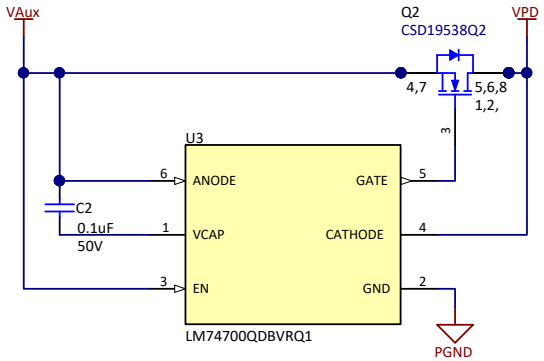
図 15. Adapter ORing Options



Implemented in this design is option 2, injecting the power right after the PD controller and before the flyback converter. Compared to option 1, option 2 allows a wider voltage range for the auxiliary input. Option 1 would limit the input voltage range to a voltage above 42 V. Option 3 would require an additional voltage regulator when realizing a 24-V input, as ORing is happening after the regulator.

To realize the powering option in the reference design, voltage must be injected between the VPD net and PGND. Decoupling the PoE voltage from the auxiliary voltage is done by using an ideal diode to minimize the voltage drop as well as power dissipation. 図 17 shows the schematic of the ideal diode. Compared to a standard or Schottky diode, the LM74700-Q1 has a regulated voltage drop of only 20 mV. Ensure that a MOSFET with proper voltage rating is used. The VPD voltage is used during PoE operation at a level of up to 57 V, whereas VAux can be zero or even at a reversed auxiliary power. This reference design uses a 100-V MOSFET here to have enough headroom.

図 16. Adapter ORing With Ideal Diode



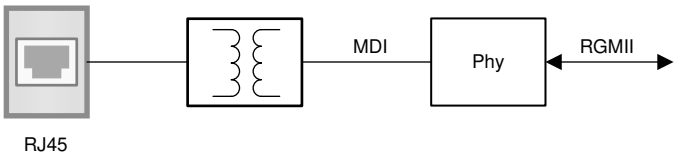
Ideal Diode for Aux Input

In addition to the diode, a resistor divider for signaling the PD controller, the presence of the auxiliary voltage is necessary. The voltage dividers R17 and R21 shown in 図 13 are designed to switch from PoE to auxiliary power at 15 V. In 3.3, the behavior of the adapter priority function is shown.

2.4.2 Ethernet Connection

The Ethernet PHY DP83867 builds the interface to the physical layer of the Ethernet connection. The overall dataflow is shown in 図 18. The task of the PHY is to translate the reduced gigabit media independent interface (RGMII) signals to a media dependent interface (MDI). This PHY supports 10/100/1000 Mbit/s Ethernet at a low power dissipation of typically 495 mW.

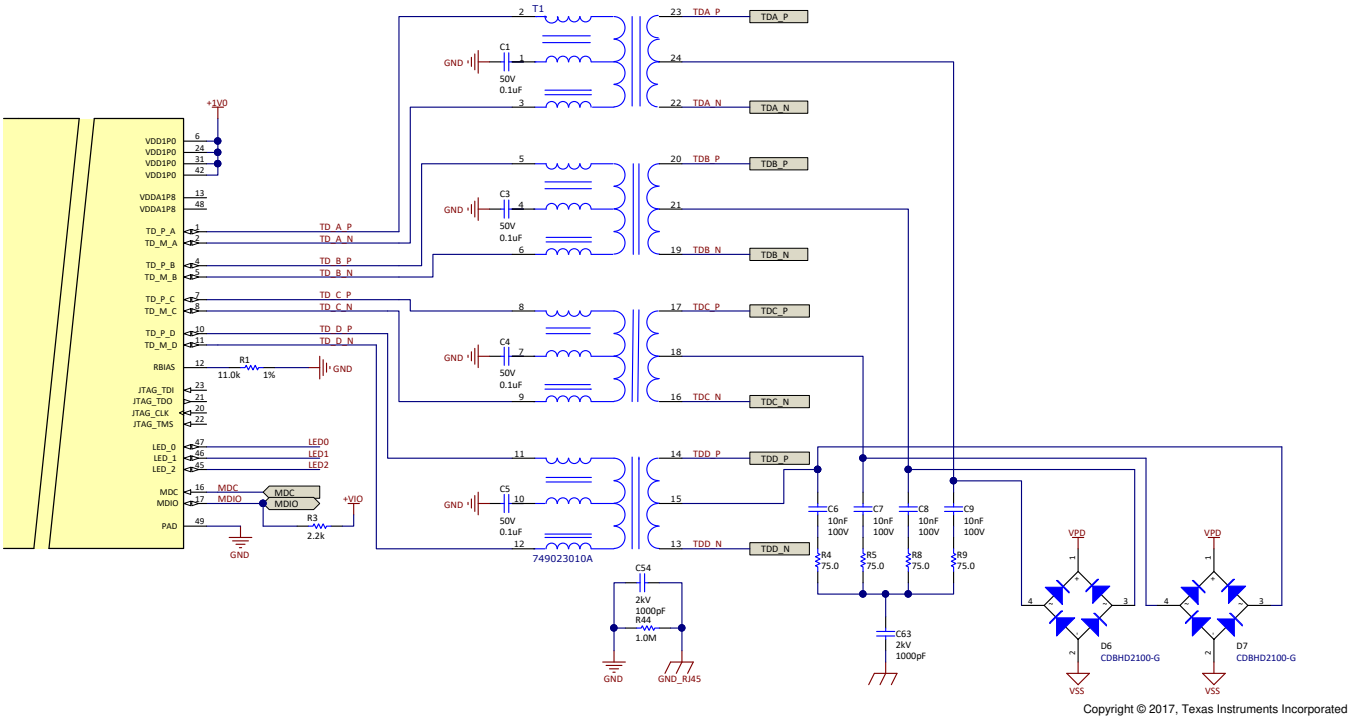
図 17. Data Path of the TIDA-010083



2.4.2.1 MDI Connection

The connection from the MDI of the PHY towards the network cable is DC isolated by using a transformer. For each pair, it is required to be isolated. As 1000-MBit/s Ethernet uses four pairs, four transformers are needed. Typically, integrated solutions with the four necessary transformers in one package are used. In space-constrained applications, it can be beneficial to have two packages with two transformers each.

図 18. Ethernet Transformer Connection



One device is used integrating four isolated channels. To implement PoE, it is important to have access to the middle tap of the transformer. In some cases, the channels are already tied together to minimize the footprint.

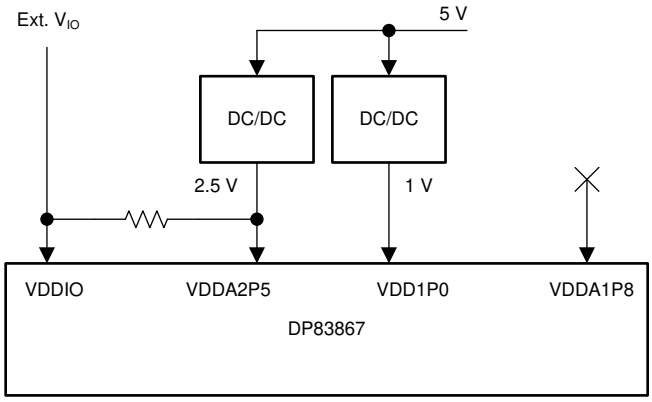
図 19 shows the connection in this reference design. On the left side, the PHYs MDI connection is shown going to the transformer. The middle tap on the PHY side must connect to the GND by using a capacitor. The middle tap of the other side is providing power to the PD controller and therefore must be connected to a diode bridge. Also, it is necessary to have a termination here. This Bob Smith termination uses a capacitor and a resistor to connect the middle taps together and to the GND. For electromagnetic interference (EMI) reasons, TI recommends connecting the GND of the cable side to the GND of the PHY through the RC network R44 and C54.

The MDI must be routed on the board as a differential pair with an impedance of 100 Ω, and the lines of each pair should have the same length. The pairs are independent to each other and do not need tight matching.

2.4.2.2 Power

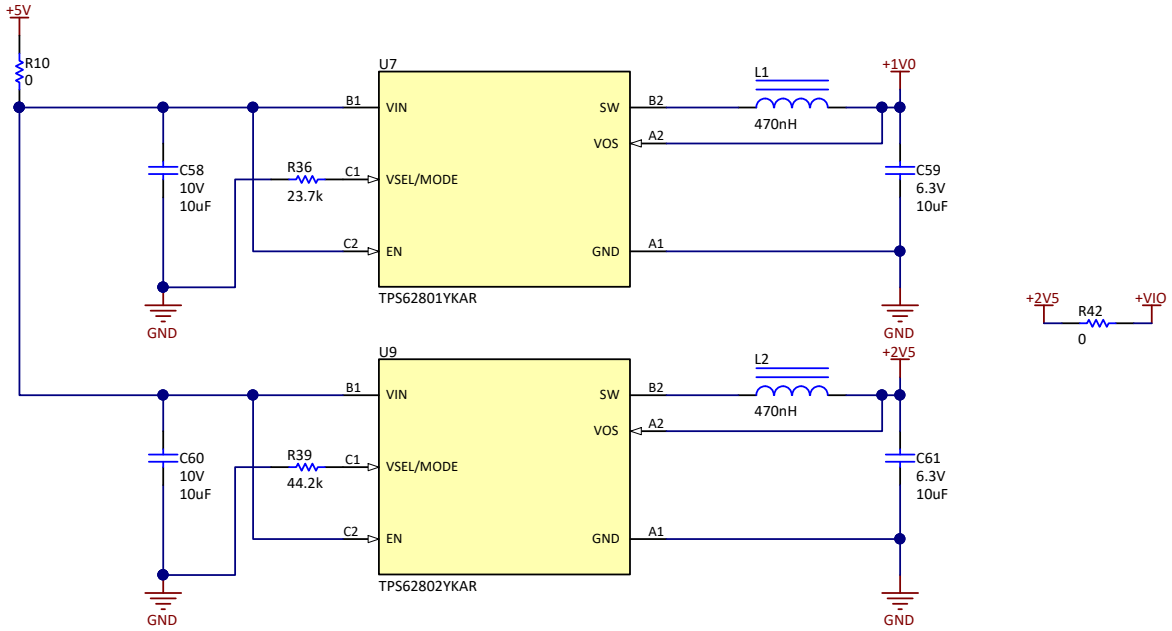
図 20 shows the power tree for the DP83867 Ethernet PHY. From the 5 V at the output of the PoE part, two additional voltages are generated to supply the Ethernet PHY.

図 19. Power Path for the DP83867



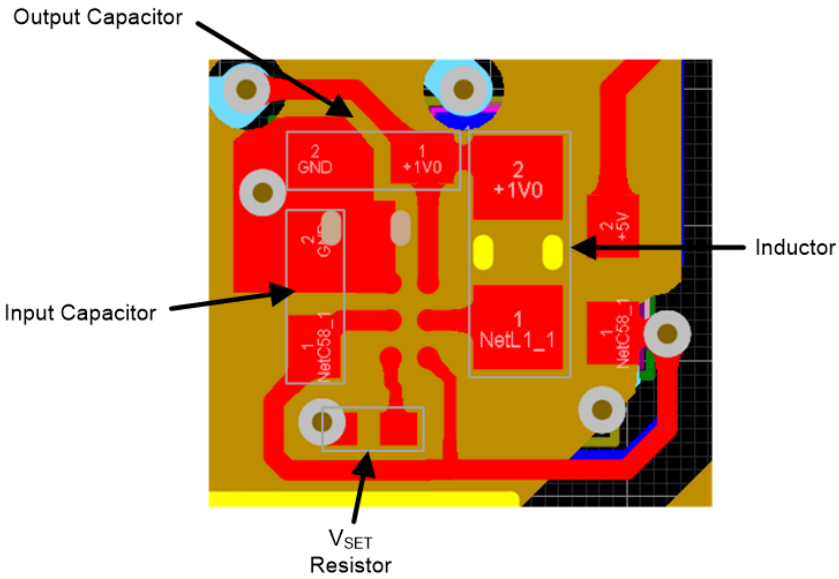
The PHY requires a 2.5-V and 1.0-V supply voltage. An optional 1.8-V rail exists that can be used to reduce the power dissipation of the PHY. However, in this reference design, this voltage is not used and is generated internally in the PHY. The IO voltage of the DP83867 can be either 1.8, 2.5, or 3.3 V. This design offers the option to either use the 2.5 V as IO voltage or an externally applied voltage. In an externally applied voltage, the resistor R42 must be removed.

図 20. Power Supply of the DP83867



In 図 21, the power supply using the TPS62801 and TPS62802 is shown. The input voltage can be disconnected by removing R10 during efficiency measurements and initial bring up. The resistor R42 is used for bridging the 2.5-V rail to the IO voltage. This voltage can be set for stand-alone testing, to supply the IO voltage to the connector, or for use on an external board. If any other IO voltage is to be used, this resistor must be removed.

図 21. TPS62801 Layout



Both regulators offer a very high switching frequency of 4 MHz and require only one resistor to set the output voltage. This enables a very small PCB footprint as shown in 図 22 for the power supply. The area shown in 図 21 is less than 4 × 4 mm² in size. Especially at this switching frequency, it is necessary to place the components as close as possible to minimize parasitic effects. The IC package is designed in a way that the critical GND, as well as the switching part, can be routed very short.

2.4.2.3 PHY

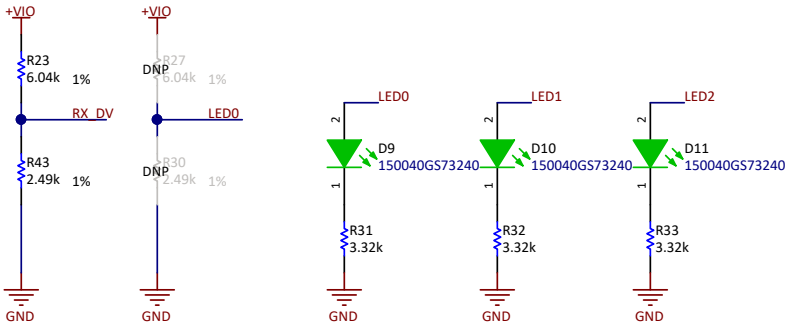
Besides power and the transformer connection, the PHY also requires additional configuration. In 図 23, the strapping configuration that is done on the board is shown. The PHY supports a four-level strapping, meaning for each configuration pin, four voltage levels are valid to define a parameter. A table in the datasheet of the DP83867 clarifies which parameter can be set on which pin. These pins are multiplexed with other functions, so following the release from reset, the strap level is read, and the pin switches its function, for example, to GPIO.

図 22. DP83867 Configuration Strapping

Straps:

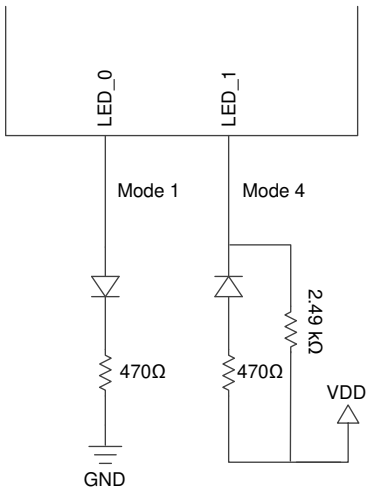
LED 0	0	Mirror En	Open
LED 1	0	ANEG SEL0	Open
LED 2	Dont care		Open
RX_CTRL	3	Auto Neg on	6.04k // 2.49k

Further strapping done on other board



The LED pins are also used as strap and depending on the level here, the connection of the LED has to be changed. 図 24shows how to connect the LEDs for different strap options.

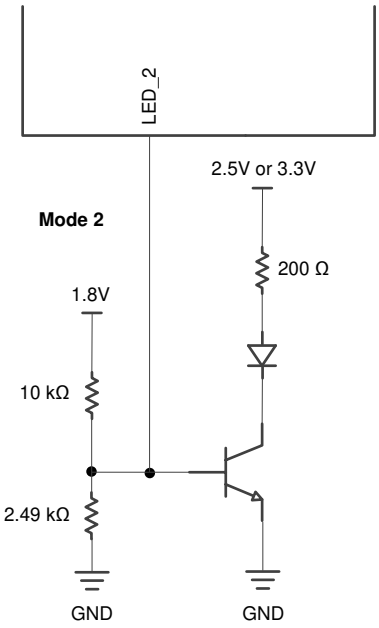
図 23. Example Strap Connection



Some of the configuration of the PHY can also be set by using MDIO, whereas the MDI address can only be set by using the strap options.

The connection of the LEDs is a bit special when using 1.8 V as IO voltage. 図 25 shows how to connect an LED in this case. As LEDs typically require more than 1.8 V to light up, an open-collector, level-shifting circuit must be built at the LED output, and a higher voltage must be used for the LED itself. This circuit can also be built using a MOSFET as long as the gate threshold voltage is low enough so that the FET switches on at 1.8 V.

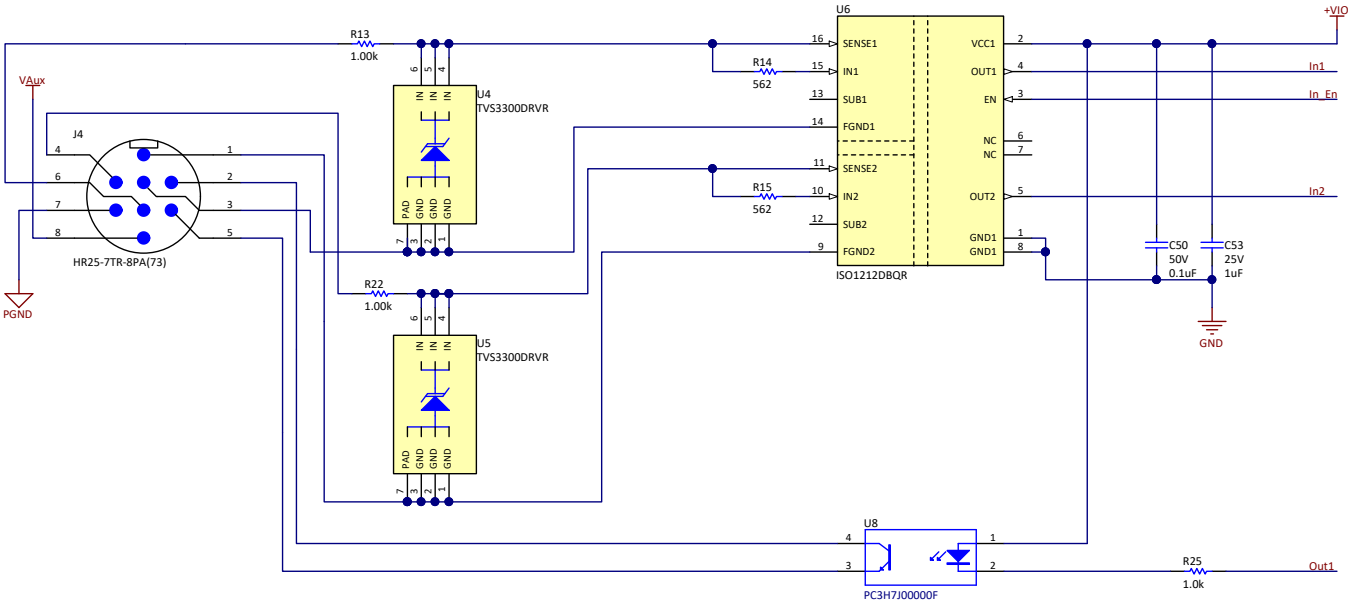
図 24. LED Options



2.4.3 Digital IO

The reference design includes two digital inputs as well as one digital output. Depending on how the PoE is realized, together with an additional auxiliary power it can be required to have an isolation for all other digital inputs and output of a system.

図 25. Digital Input and Output Schematic



Here a digital isolation of the IOs is implemented. This enables flexibility in how to use the inputs and outputs. 図 26 shows the implementation in the schematic. All digital channels are isolated to each other and can be used in an NPN or PNP configuration.

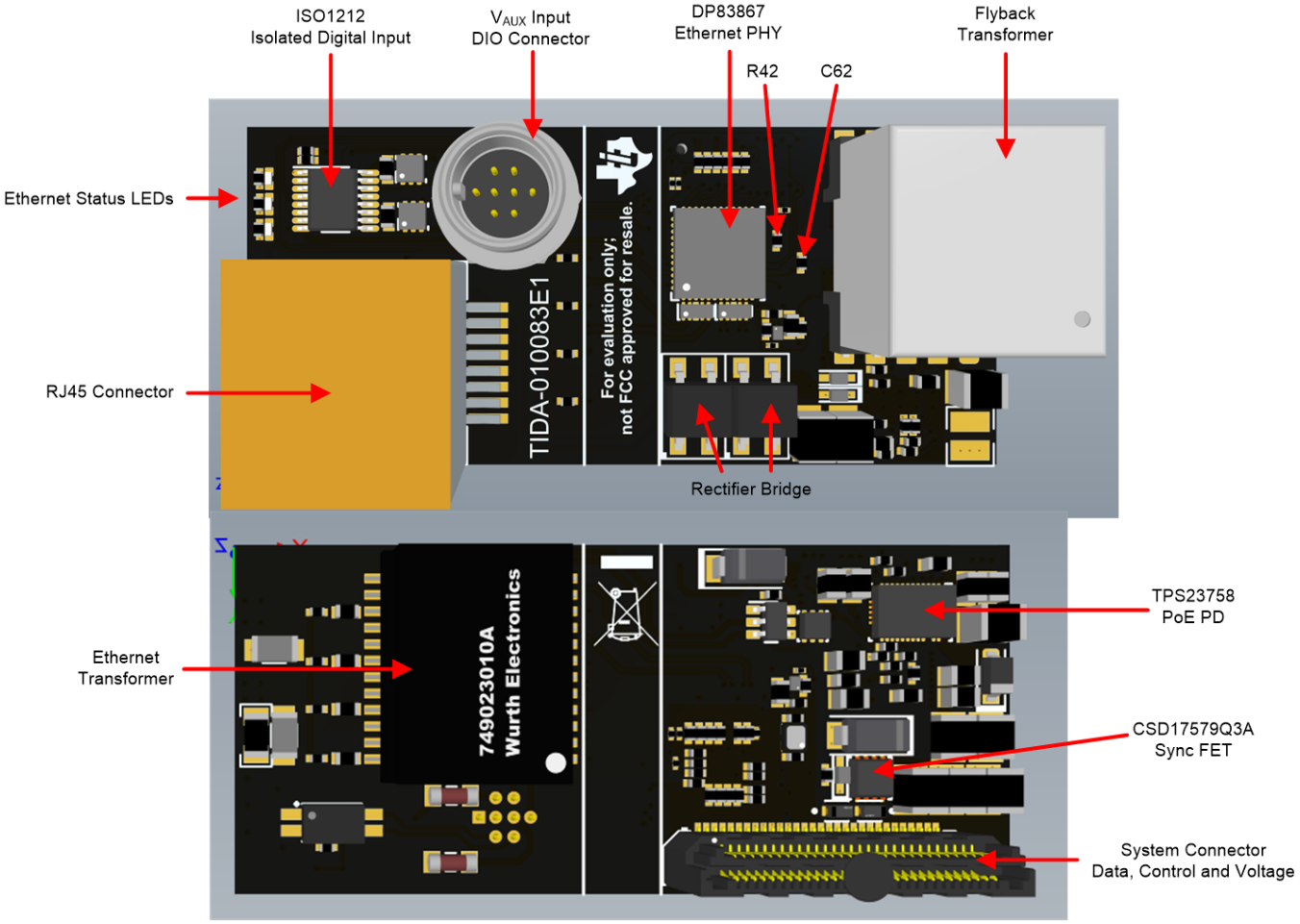
The digital inputs are realized with an ISO1212 that can be used for realizing type 1, 2, and 3 digital inputs and withstands ±60 V.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

This reference design can be evaluated alone or with an additional FPGA or a processor board with an RGMII interface. The IO voltage for RGMII, as well as the digital IOs, can either come from the design and be set to 2.5 V, or it can be applied externally after removing R42. The Ethernet PHY can either be clocked by the on-board crystal or by removing the crystal and assembling C62 from any external source. See 図 27 for an overview of the physical location of the main components and connectors.

図 26. Reference Design Overview (Top and Bottom View)

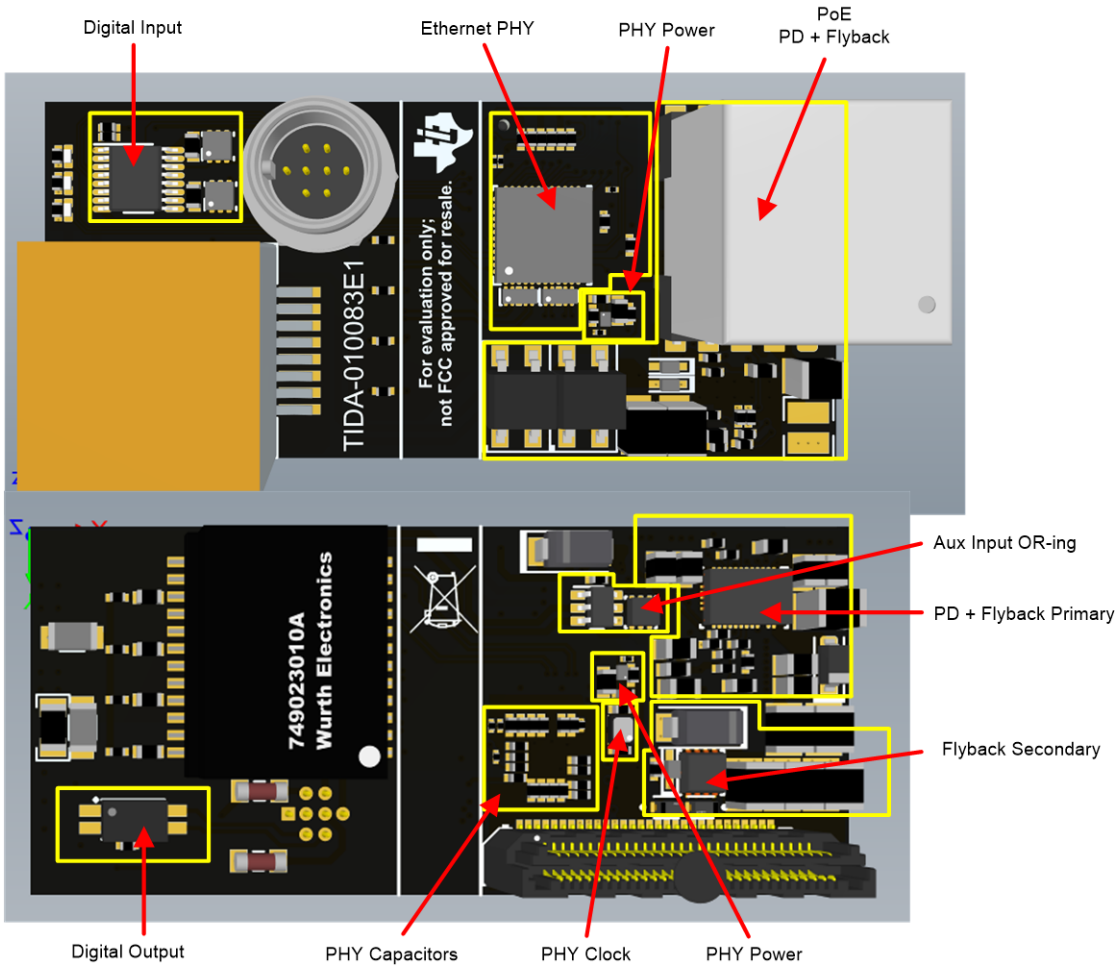


The system connector shown in 図 26 provides access to the RGMII signals and digital IO and provides 5 V at a maximum of 2.4 A of output power. For complete evaluation of the data connection, TI recommends using a custom adapter board with the correct impedance and length matching to have a proper signal integrity of the RGMII signals to connect to a MAC, either in FPGA or processor. For testing the MDI path including the RJ45 Ethernet transformer and PHY, the PHY can be placed into a reverse loopback mode. This enables remote testing of the connection and impact of PoE without the RGMII connection. See 3.5 for the test setup and results of this test.

For evaluating the power stage of the board, it is necessary to connect a load to the system connector and a power source to one of the inputs as described in 3.2.1. Three different transformers are tested as a part of this design. Two variants are designed for 5 V and 13 W, and one variant is designed for lower power applications with 4 V and 7 W.

In 図 28 an overview is shown where the different functional blocks of the system are located on the PCB.

図 27. Functional Blocks (Top and Bottom View)



3.2 Testing and Results

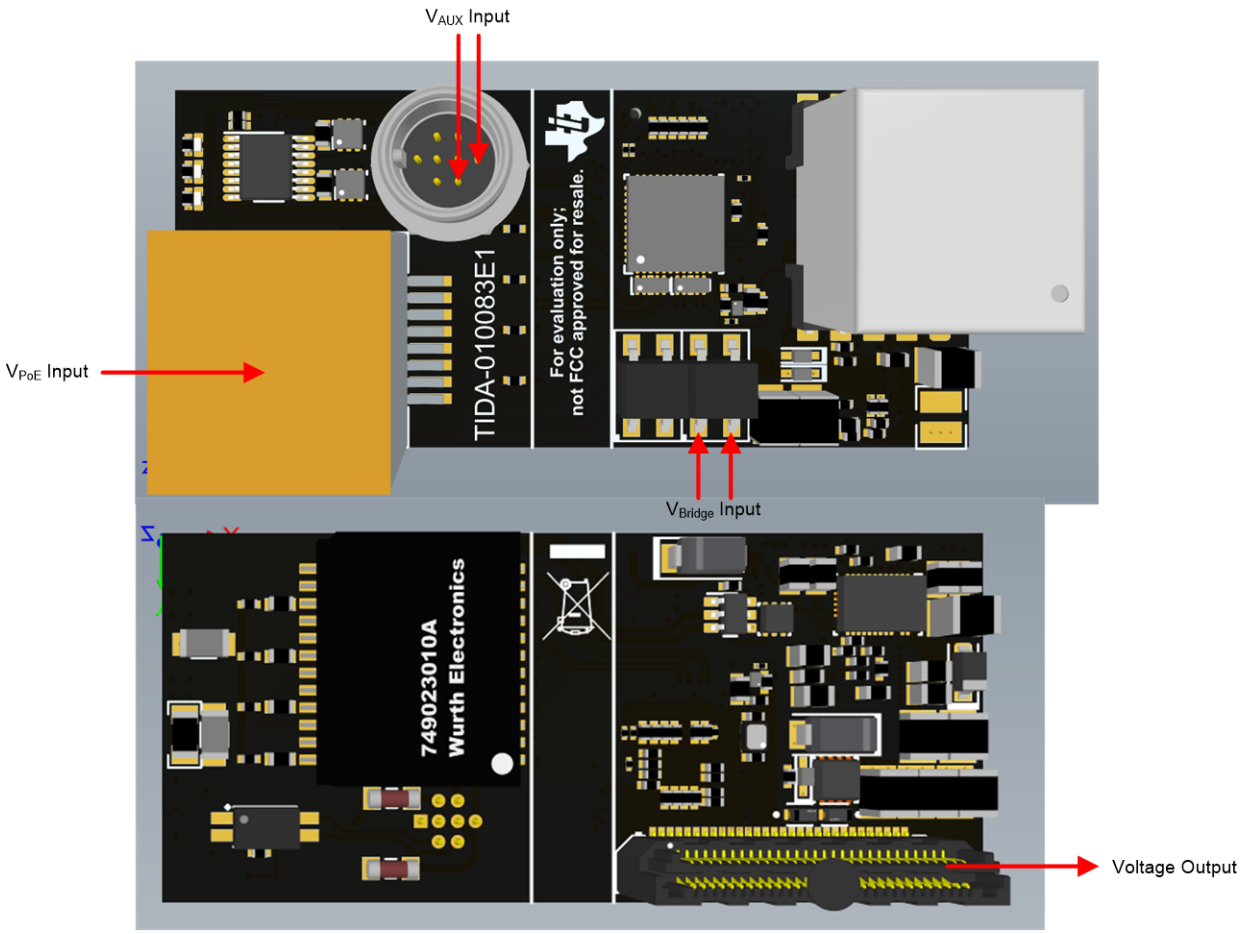
The following section contains measurement data of the isolated flyback converter, the PD controller, and the Ethernet PHY itself. Also included are thermal images showing the design at different load levels and transformer configurations. The test setup is explained in each section.

3.2.1 TPS23758 PoE Flyback

This section covers different tests that were done on the flyback part of the design. The efficiency and voltage drop is tested with different transformers and input voltages. Because there are different possibilities to power the flyback, these where tested separately. In 図 29, the different options for voltage input on the PCB are shown. Power comes through the RJ45 connector (shown as V_{PoE}) which is the usual way to power a PoE PD from the PSE. A second option is to power it through the V_{AUX} input, bypassing the PD part of the TPS23758 and powering the flyback converter directly. A third option is powering the part after the diode bridges (V_{Bridge}), bypassing the diodes but not the PD part. The different variants for powering have different path losses like voltage drop on the diode bridges and the pass FET for the PD. Though the efficiency depends on where the voltage is injected. The highest efficiency can be achieved using the V_{AUX} input that bypasses the PD part.

As the flyback is using primary side regulation, the voltage at the output can show a small current depended drop.

図 28. V_{AUX} Input for Efficiency Testing (Top and Bottom View)



3.2.1.1 TPS23758 Using LinkCom® LDT1018 Transformer

This sections covers all tests done with a LinkCom® LDT1018 transformer, designed for 13 W at 5 V. In 図 30 shows the efficiency and drop of the output voltage. For this test, the power comes through the V_{AUX} input, giving the highest efficiency. As it is not designed to be fully loaded at low input voltages, the curves for 18 V, 24 V, and 30 V are not measured up to 2.5 A.

The same tests are done with power over the RJ45 connector, V_{PoE}, shown in 図 31.

A third test is done powering after the diode bridges, V_{Bridge}, shown in 図 32.

図 29. Efficiency and Voltage When Powered Through V_{AUX}

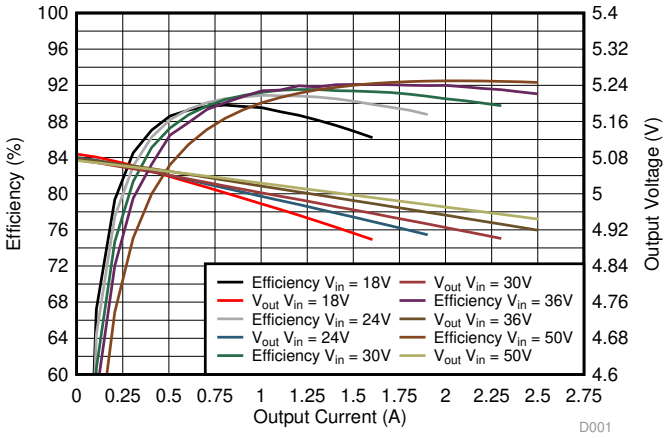


図 30. Efficiency and Voltage When Powered Through V_{PoE}

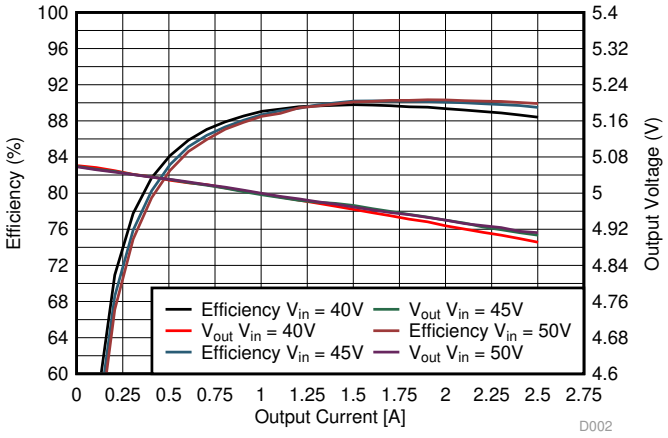
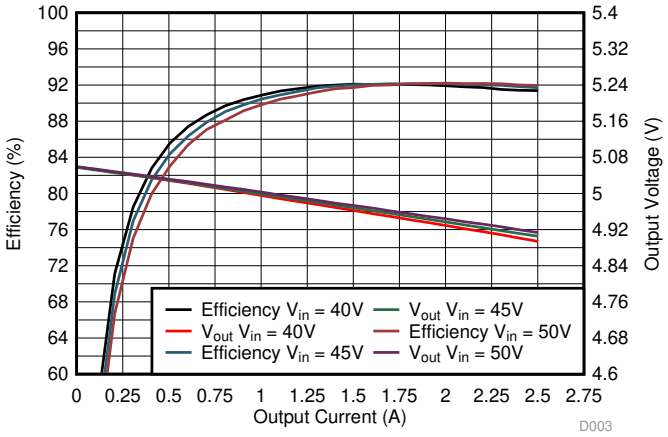


図 31. Efficiency and Voltage When Powered Through V_{Bridge}



3.2.1.2 TPS23758 Using Würth 750318525 Transformer

This section handles the same tests as before with a 750318525 transformer from Würth, designed for 13 W at 5 V.

図 32. Efficiency and Voltage When Powered Through V_{AUX}

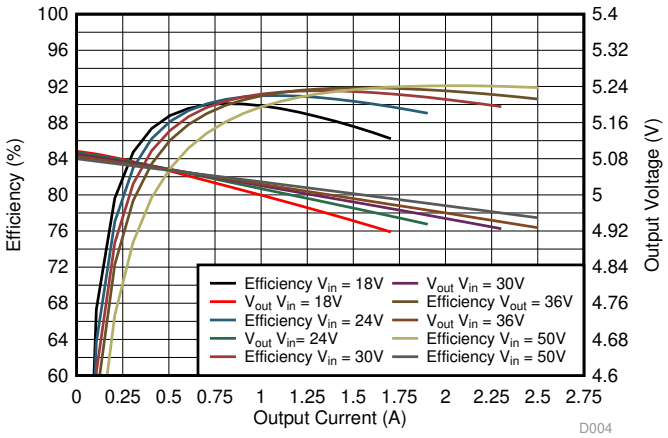


図 33. Efficiency and Voltage When Powered Through V_{PoE}

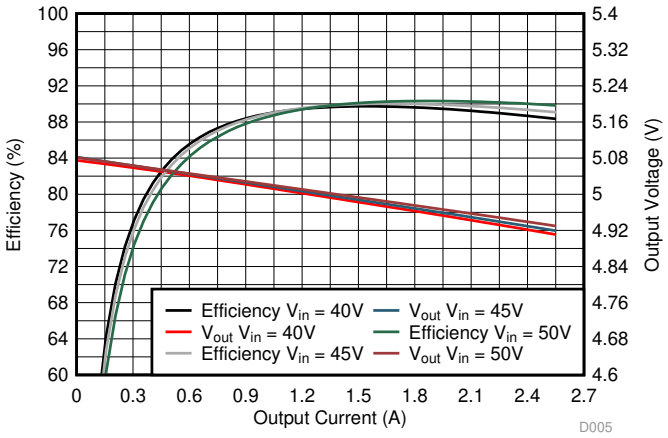


図 34. Efficiency and Voltage When Powered Through V_{Bridge}

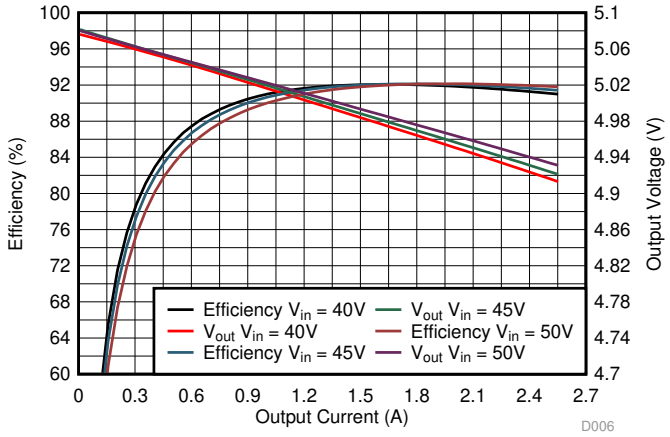


図 35. Loop Compensation With 750318525 Transformer

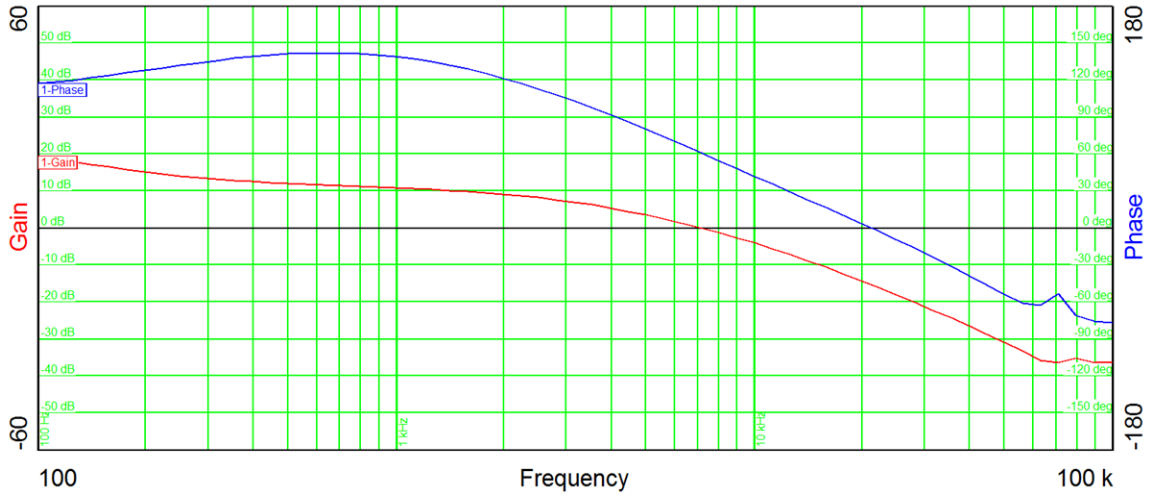


図 36 shows the frequency response of the regulation loop with the Würth 750318525 13-W transformer tested at a 2.4-A load with a 36-V input voltage. The value of C52 must be set to 6.8 nF and R28 to 100 kOhm for this as noted in the schematic.

図 36. Switch Node at Full Load at 36 V

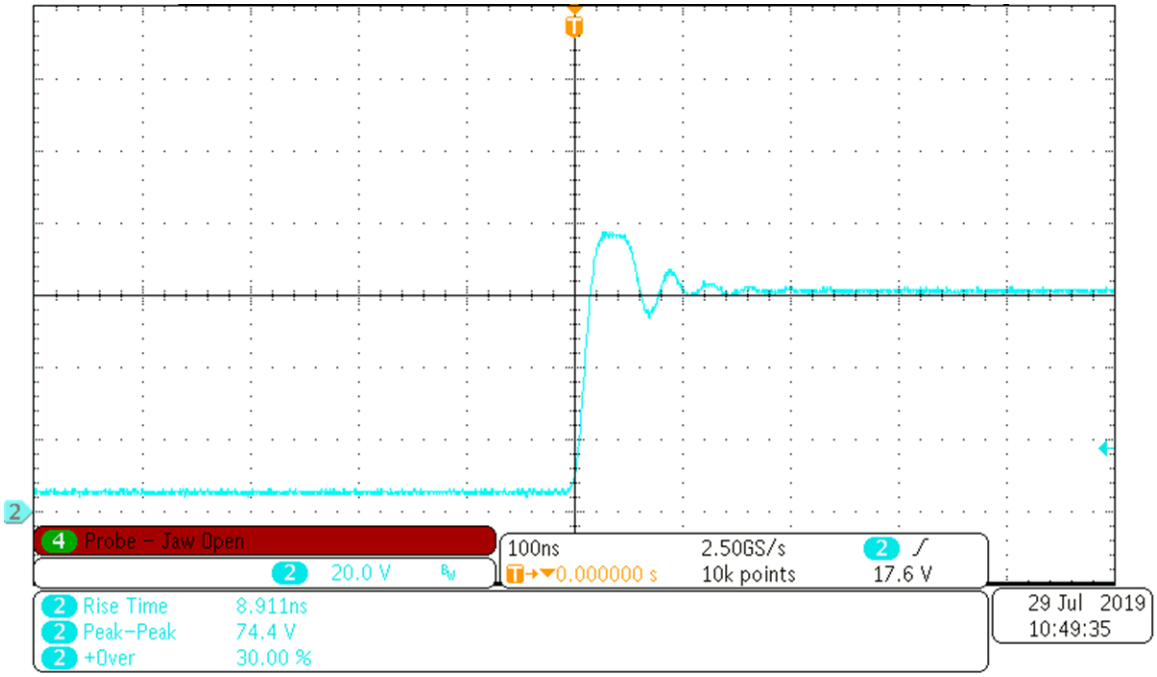


図 37 shows the switch node at an load current of 2.4 A and an input voltage of 36 V.

図 37. Switch Node at Full Load at 50 V

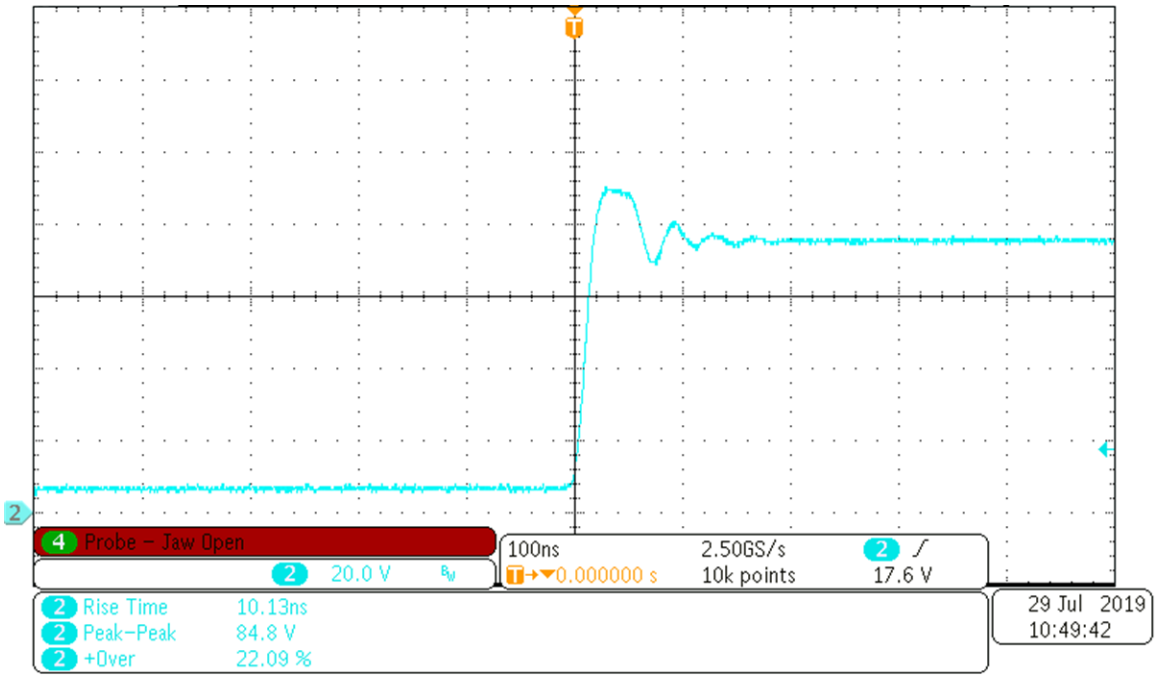


図 38 shows the switch node with same load as before at an input of 50 V.

図 38. Load Step 36-V Input Voltage

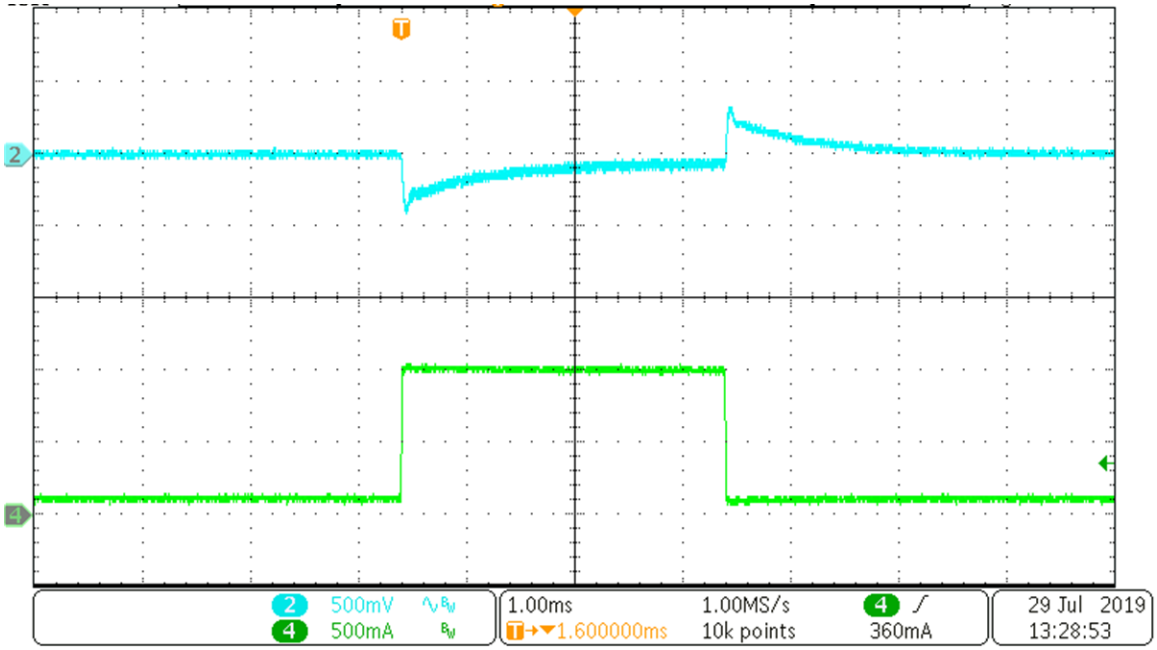


図 39. Load Step 50-V Input Voltage

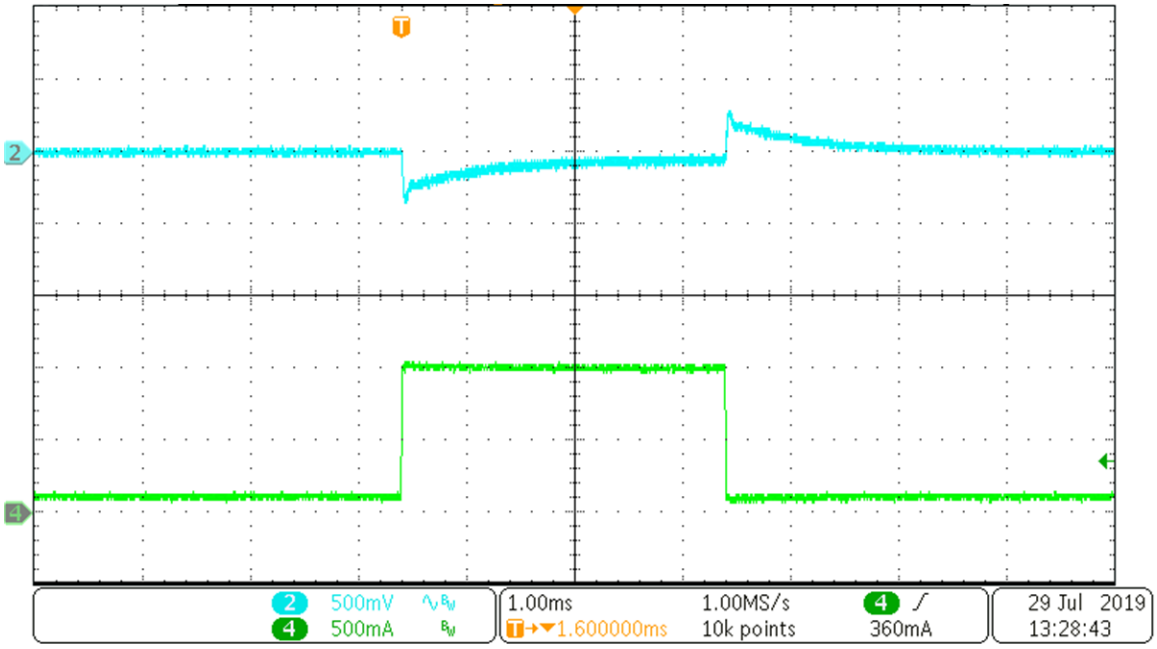


図 39 and 図 40 show the response to a fast load step from 0.1 A to 1 A at different input voltages. The reaction on the step confirms a fast and stable regulation.

3.2.1.3 TPS23758 Using Würth 750318517 Transformer

The same tests as performed previously are done with a Würth 750318517 transformer. This transformer has a smaller mechanical size and is designed for 7 W at an output voltage of 4 V.

図 40. Efficiency and Voltage When Powered Through V_{AUX}

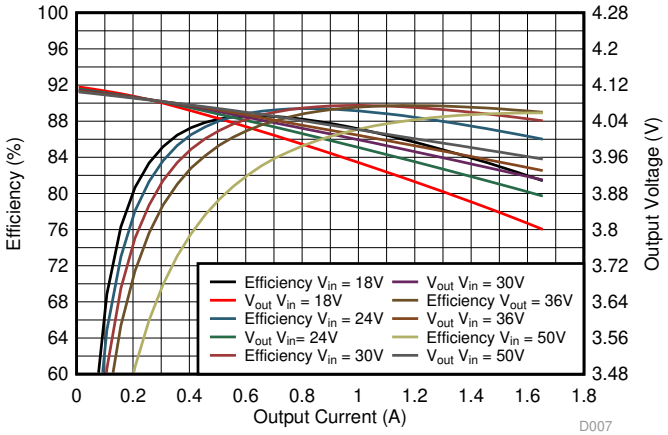


図 41. Efficiency and Voltage When Powered Through V_{PoE}

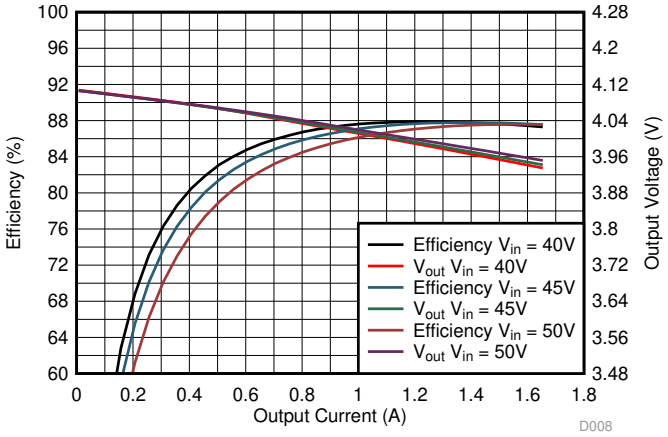


図 42. Efficiency and Voltage When Powered Through V_{Bridge}

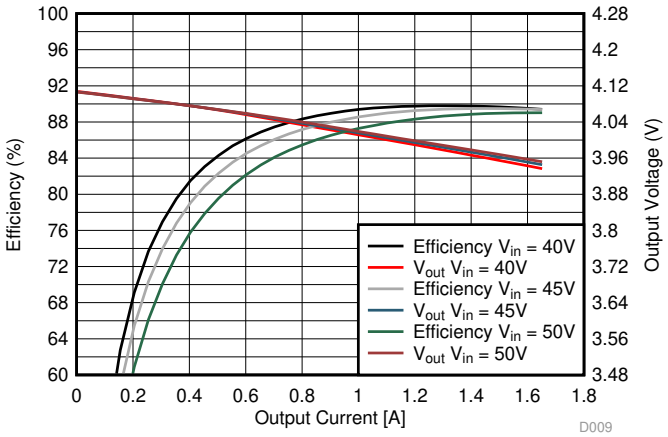


図 43. Loop Compensation With 7-W Transformer

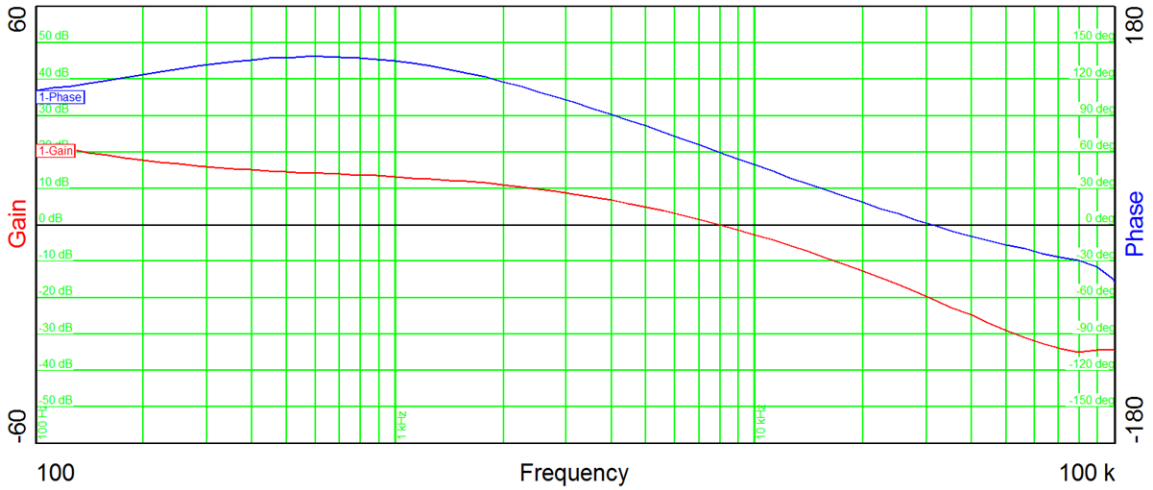


図 44 shows the frequency response of the regulation loop with the 7-W transformer tested at a 1.6-A load with a 18-V input voltage. The value of C52 must be set to 10 nF and R28 to 68 kOhm for this as noted in the schematic.

図 44. Switch Node at Full Load at 18 V

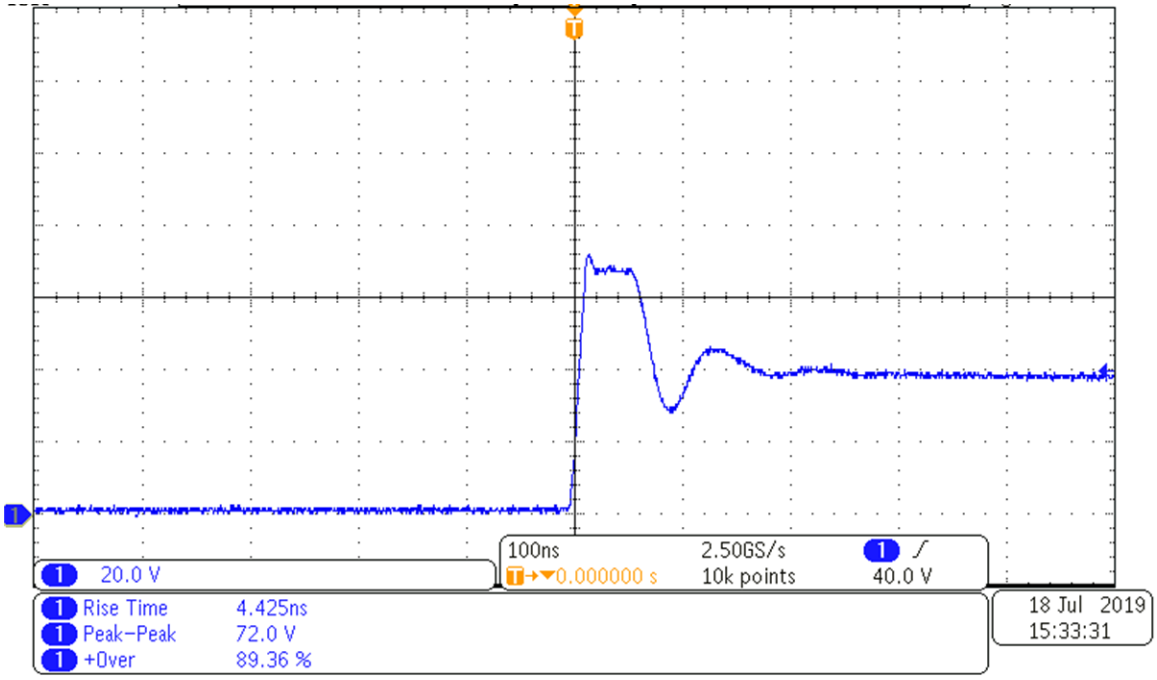
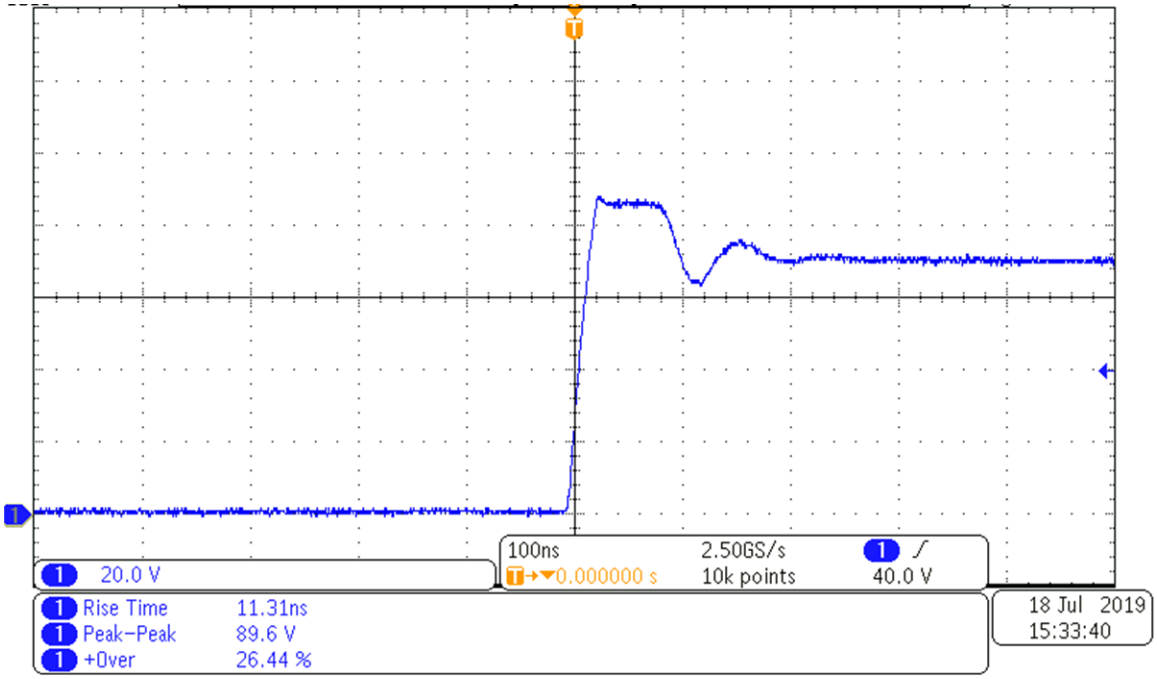


図 45 shows the switch node of the flyback at a 18-V input voltage as full load of 1.6 A.

図 45. Switch Node at Full Load at 50 V



In 図 46, the switch node with the 750318517 7-W transformer is shown at a 50-V supply voltage.

図 46. Load Step at 18-V Input

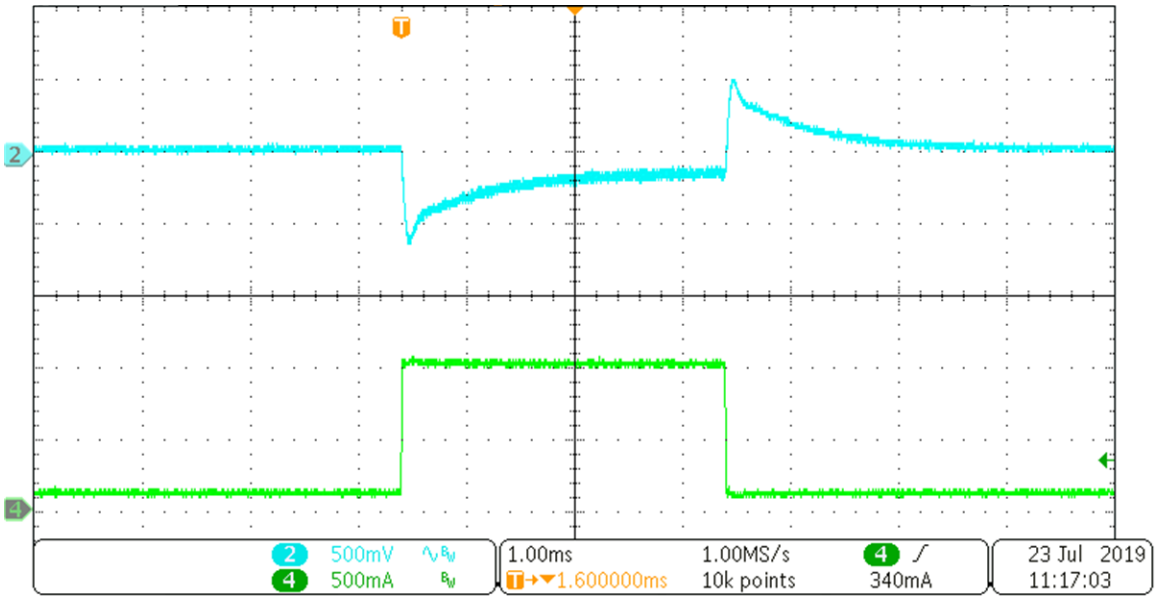


図 47. Load Step at 50-V Input

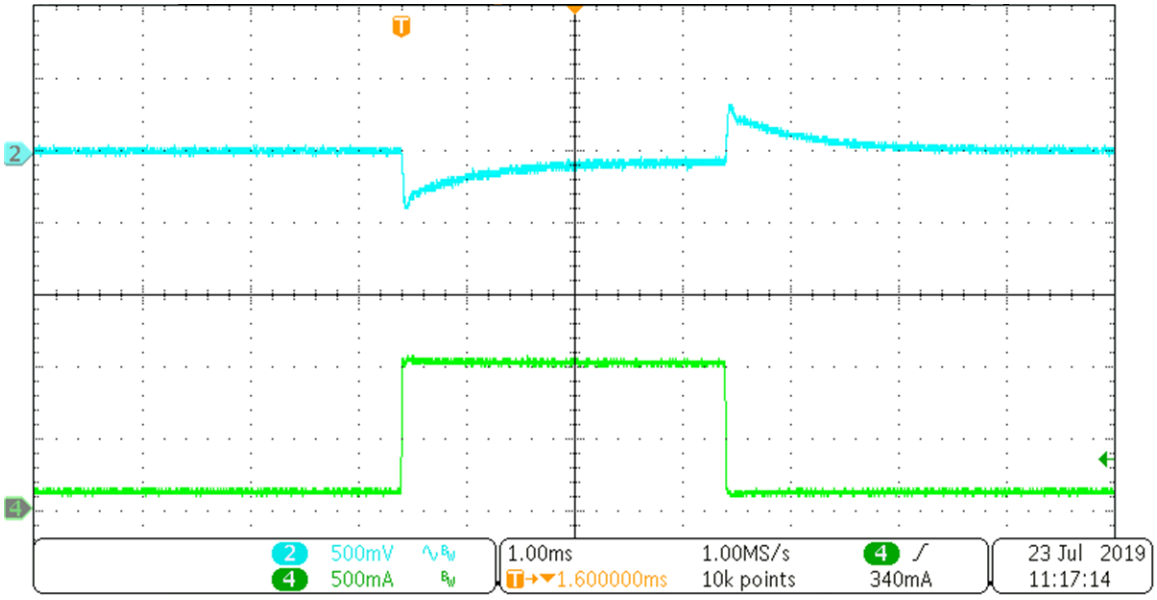


図 47 and 図 48 show the response to a fast load step from 0.1 A to 1 A at different input voltages. The reaction on the step confirms a fast and stable regulation.

3.2.2 TPS23758 PoE Powered Device - Detection and Classification

Depending on the voltage coming from the PSE, the PD must behave differently to do the correct signaling for detection and classification. To test the proper behavior, the PoE voltage is swept from 0 V to 50 V, and the input current is measured.

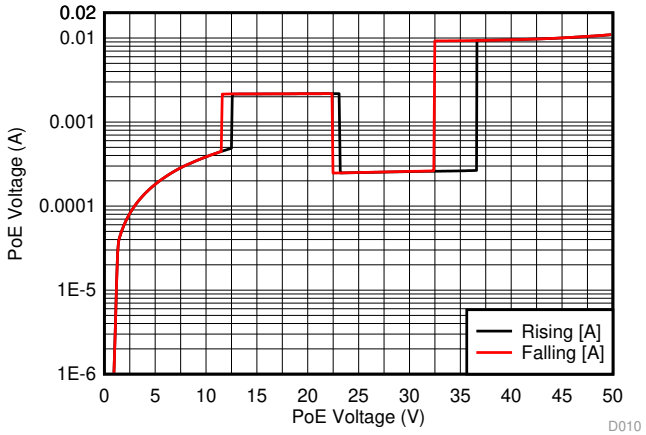
In the phase between 2.7 V and 10.1 V, the detection happens, and it must behave like a resistor of 19 kΩ and 26.5 kΩ.

Between 14.5 V and 20.5 V, the classification is happening and the current must be for a class 0 device between 0 mA and 4 mA.

Between 36 V and 42 V, the PD must turn on when the voltage is rising.

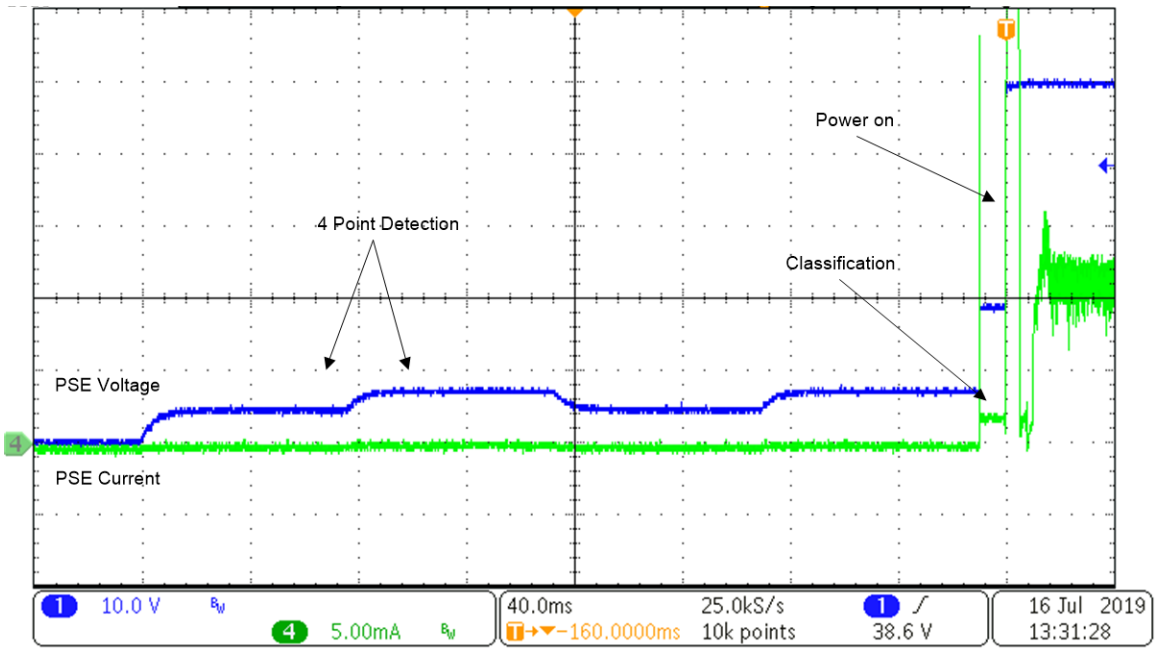
In 図 49, the results of sweeping the PoE voltage is shown. The different current levels, the turn on point, and the hysteresis can be seen.

図 48. PD Behavior Over Voltage



When connecting the PD to a PSE, the PSE senses the detection resistance followed by the classification current. 図 50 shows the scope plot of this process. The blue line shows the voltage which defines the state the PD is in. It starts with a detection phase, followed by the classification and then finally powers the device on.

図 49. PoE Detection and Classification



3.3 Auxiliary Power Priority

The TPS23758 allows a smooth transition from PoE power to auxiliary power.

図 50. PoE to Auxiliary Transition

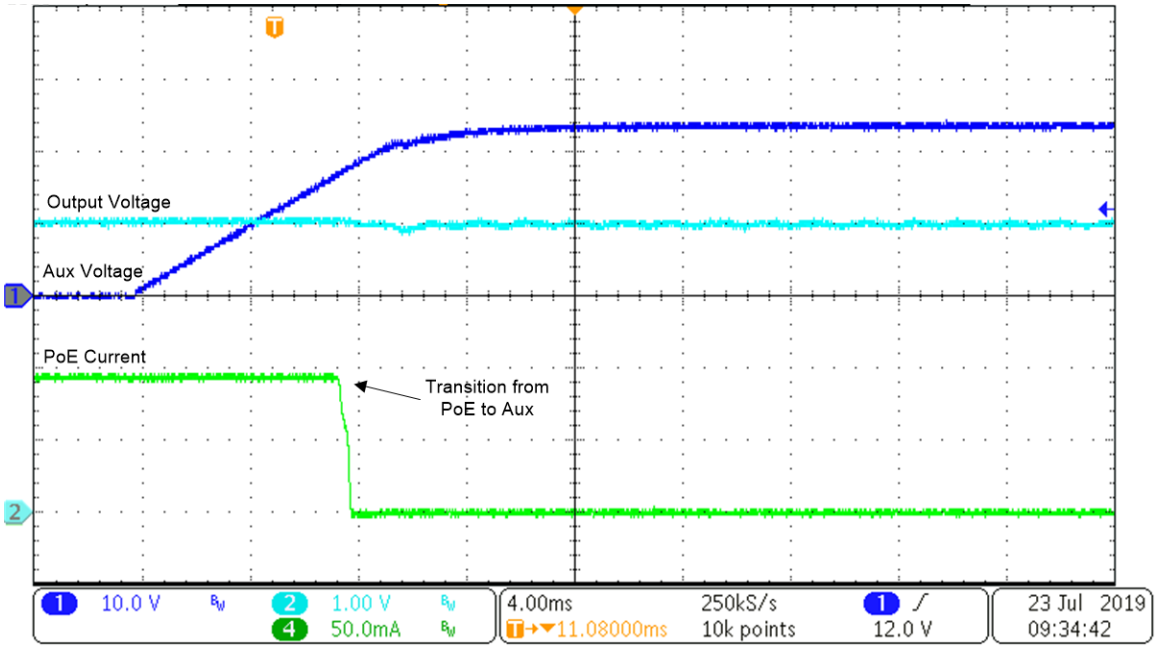


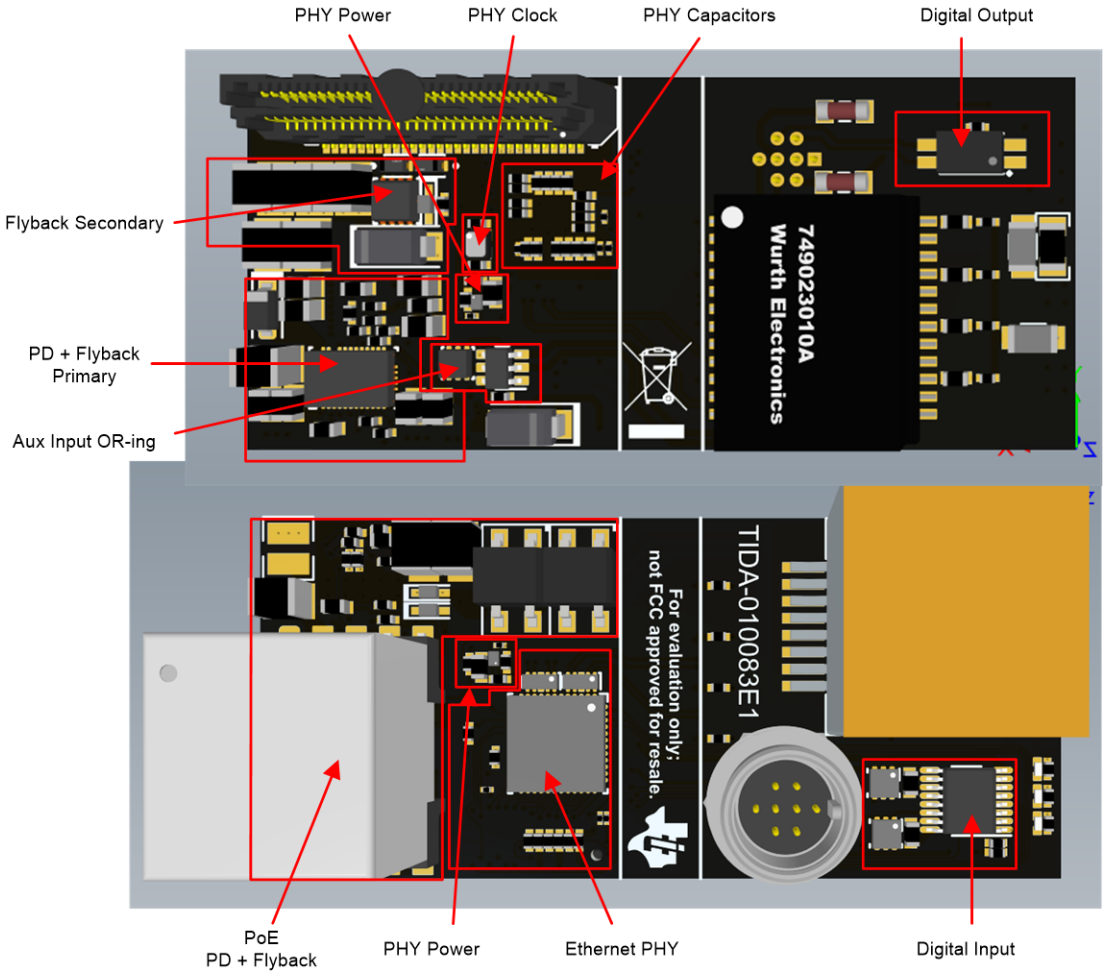
図 52 shows how the TPS23758 transitions from PoE power supply to auxiliary power. As soon as the auxiliary voltage is above a certain level, the PD switches off and the PoE current falls to zero. The necessary power is provided over the auxiliary power supply. The output voltage remains stable during the transition.

3.4 Thermal Performance

This sections shows the thermal performance of the reference design with two different configurations. One variant uses the previously mentioned 750318517 transformer tested up to 7 W, and the other variant uses one of the 13-W transformers.

The thermal images below are stitched together to show both sides of the PCB at once. 図 51 shows the functional blocks on the board in the same orientation as in the thermal images to understand the thermal behavior of the different subsystems.

図 51. Functional Blocks as Shown in Thermal Images



3.4.1 Output Configured for 7 W, 4 V

For this test, the reference design uses the Würth 750318517 transformer and is loaded with 1.6 A.

図 52. Thermal Image With 18-V Supply Voltage and 1.6-A Load

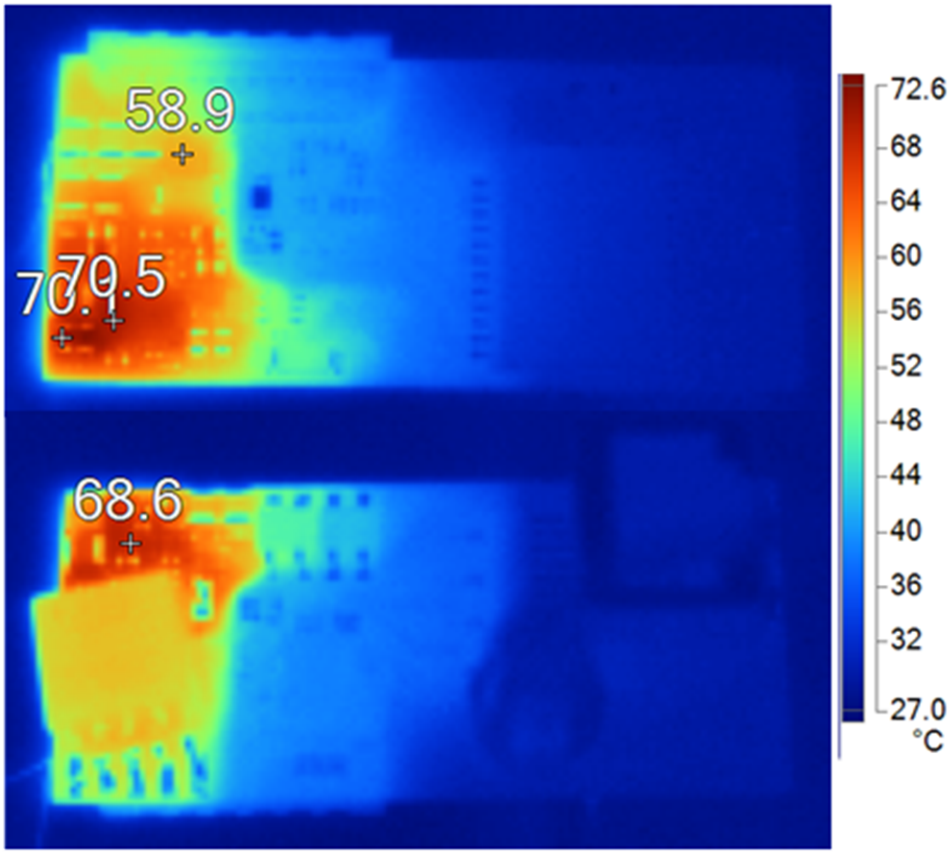


図 53 shows the design loaded with 1.6 A and an input voltage of 18 V. For this test, the design is powered through the V_{AUX} input. As this is the lowest designed input voltage, this results in the highest input and switching currents, as well as the highest duty cycle. The image shows that the highest temperature is at the TPS23758 and the shunt resistor for current measurement, so the most power is dissipated by the switch FET of the flyback regulator. The rectification FET on the secondary side does not dissipate that much power. Also, the ORing FET that is used at the V_{AUX} input does not heat up significantly.

図 53. Thermal Image With 36-V Supply Voltage and 1.6-A Load

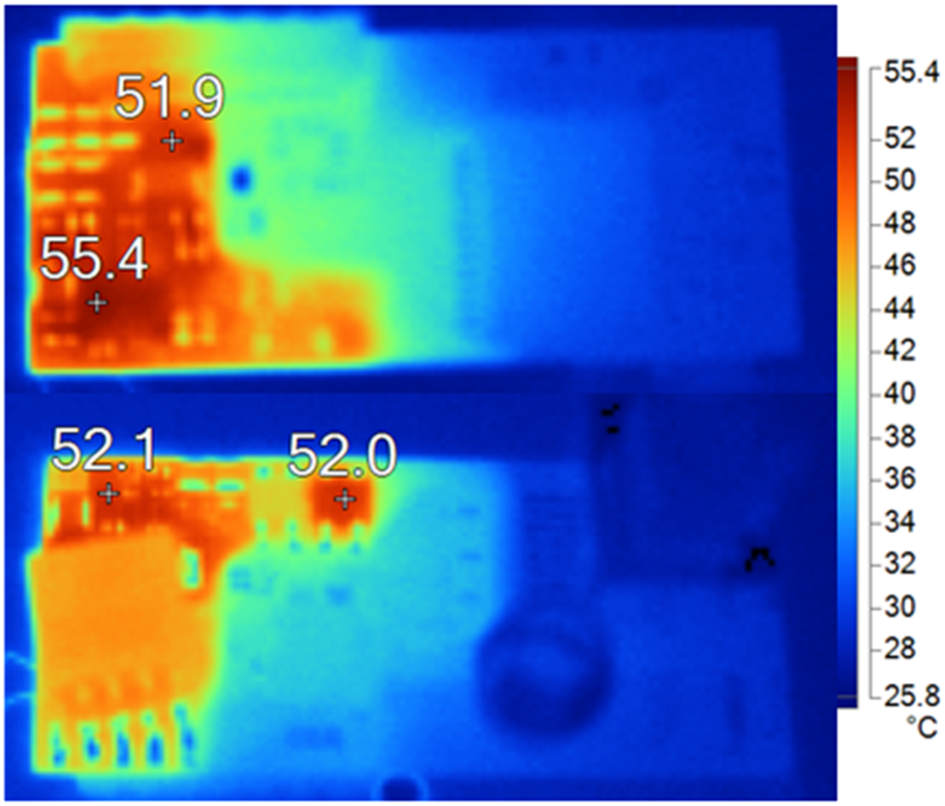


図 54. Thermal Image With 50-V Supply Voltage and 1.6-A Load

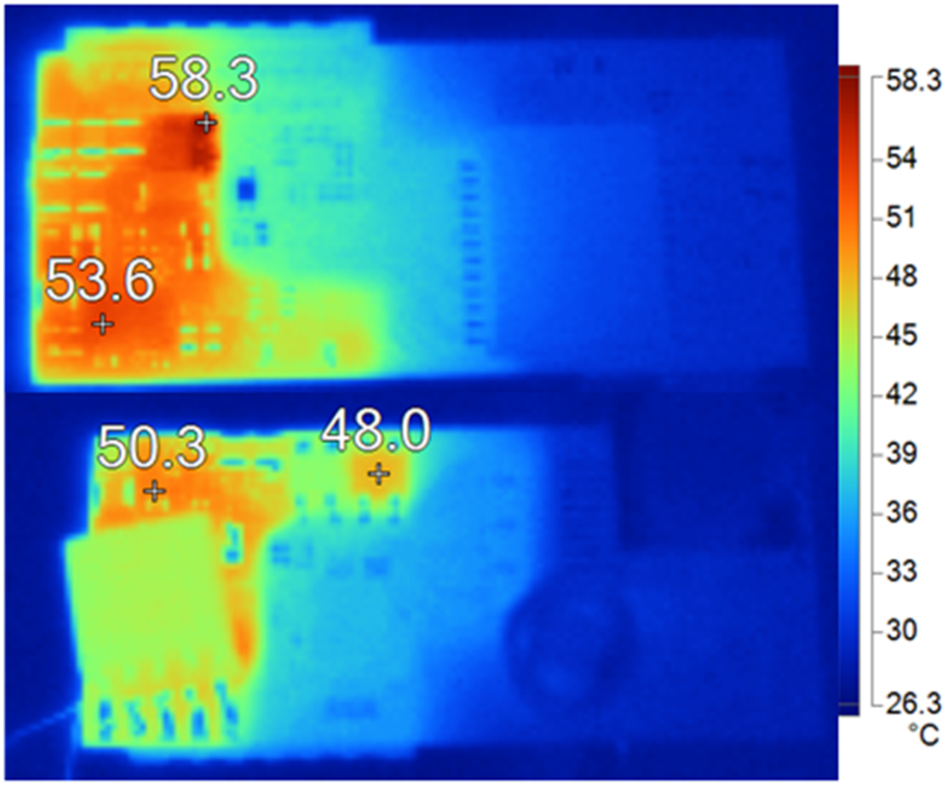


図 54 and 図 53 show the design powered through the V_{PoE} input at different voltage levels. In addition to the heat dissipated from the TPS23758, here also the diode bridge gets a significant heat source.

3.4.2 Output Configured for 13 W, 5 V

For this test, the reference design uses the Würth 750318525 transformer and is loaded with 2.4 A. 図 55 and 図 56 show the design powered through the V_{PoE} input at different voltage levels. In addition to the heat dissipated from the TPS23758, here also the diode bridge gets a significant heat source.

図 55. Thermal Image With 36-V Supply Voltage and 2.4-A Load

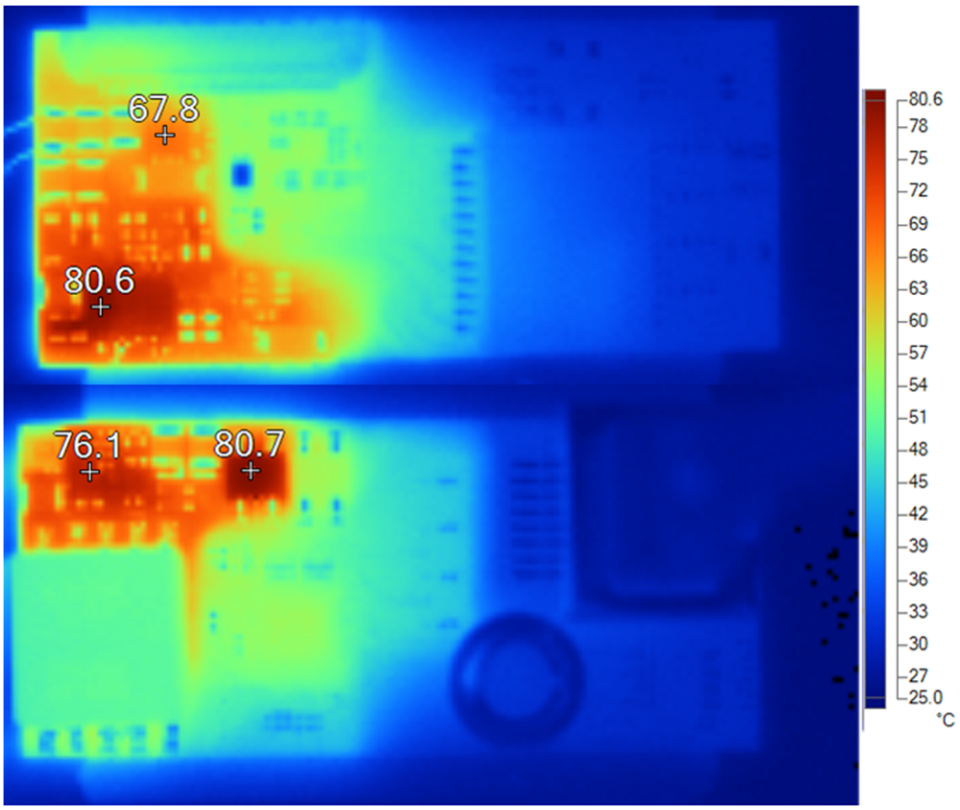


図 56. Thermal Image With 50-V Supply Voltage and 2.4-A Load

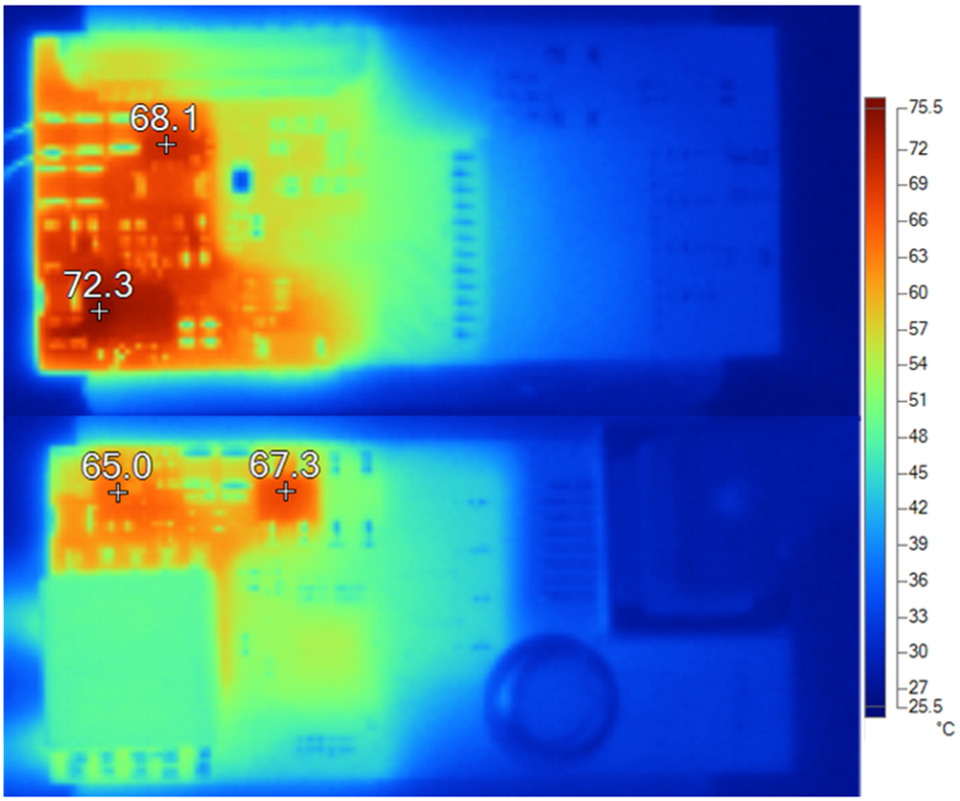


図 57. Thermal Image With 48-V Supply Voltage and 1-A Load

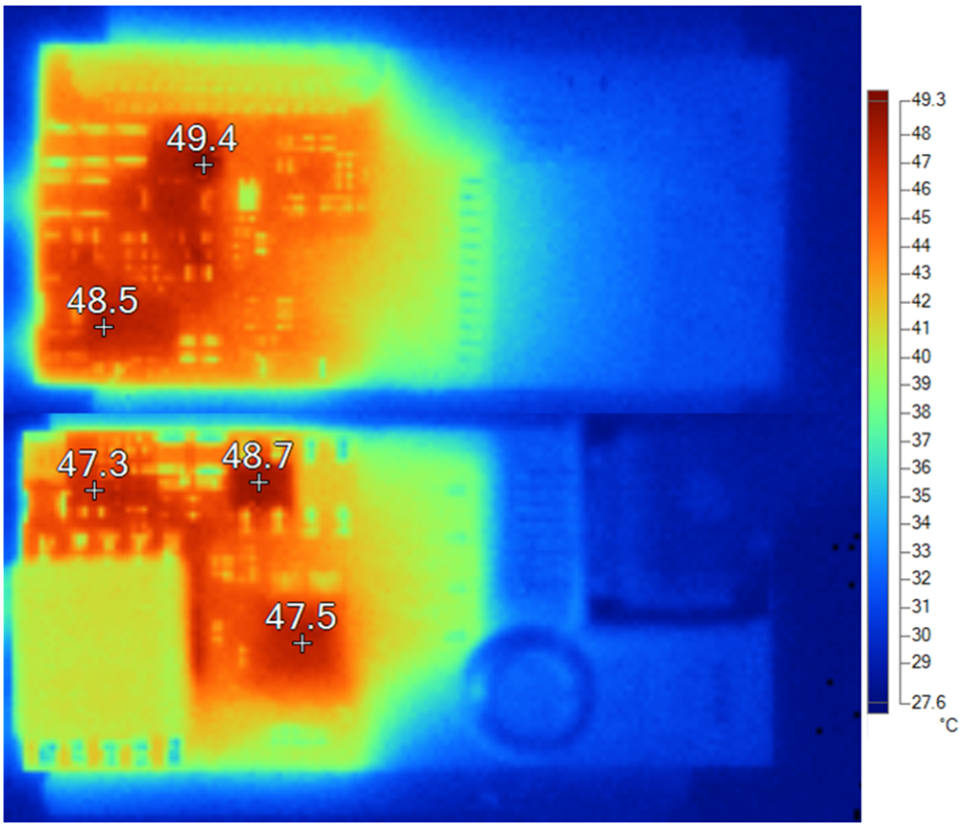


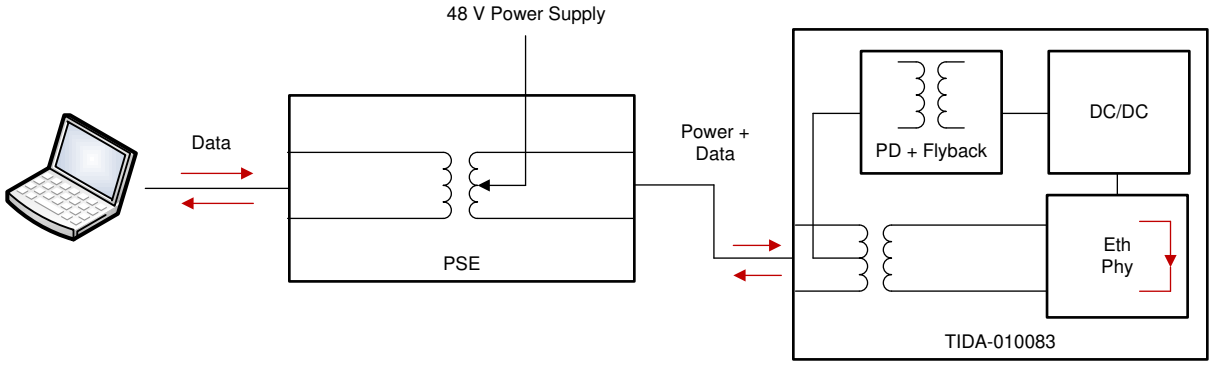
図 56 and 図 57 show the 13-W solution at full load and two different input voltages. In 図 58, the system is shown with a load of 1 A and a typical PoE voltage of 48 V.

Depending on the desired total system power, it might be necessary to have better cooling or reduction of the diode losses in the rectifier bridge by using an active rectification circuit. In larger applications, a larger cooling plane will help to reduce the temperature on the board. A thicker copper layer on the board will help to improve thermal transfer.

3.5 Data Interface

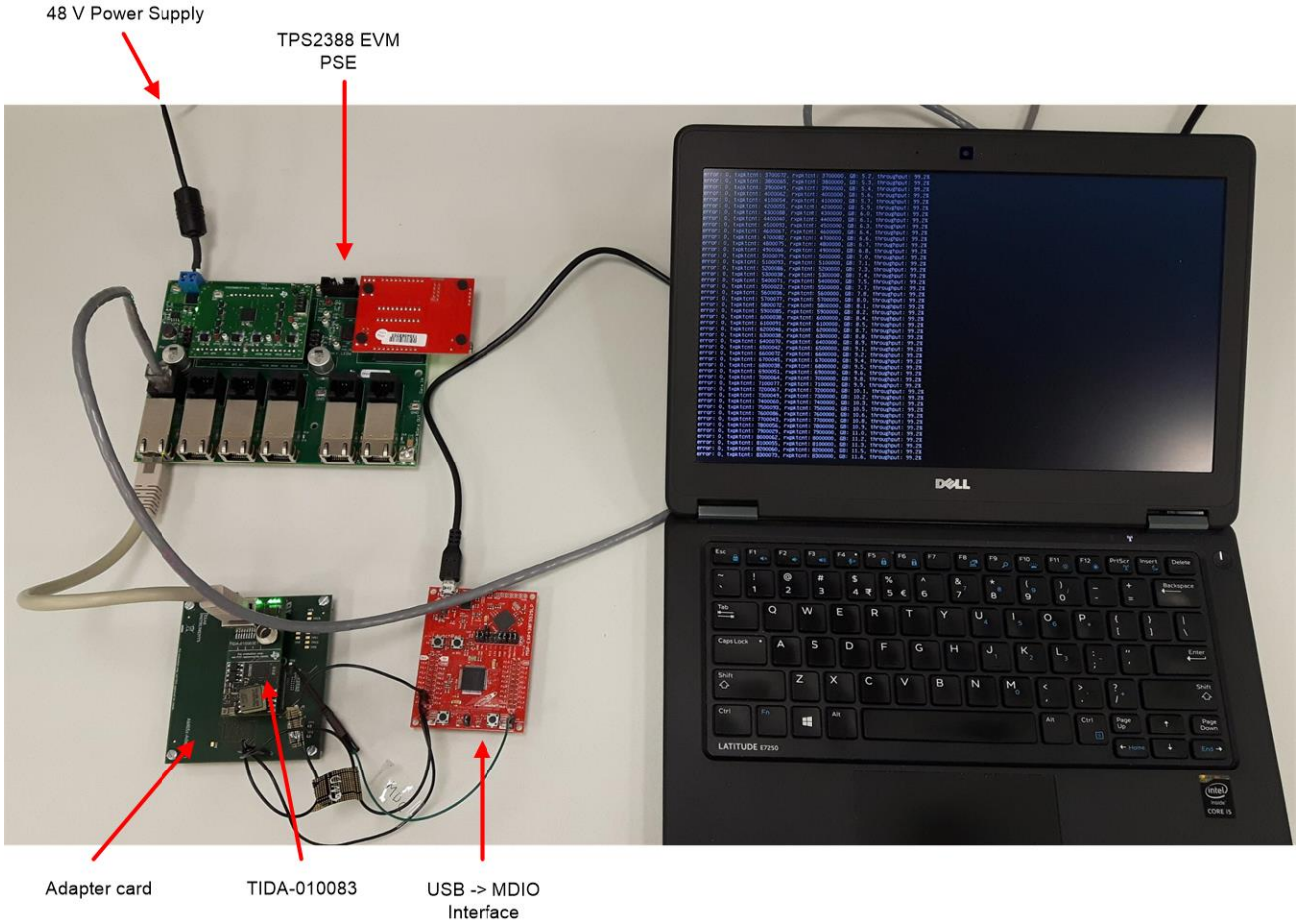
To test the MDI interface and by this the path from the RJ45 connector over the data transformer towards the PHY, the setup shown in 図 59 is used. The PHY is configured in reverse loopback, so it sends every frame that is received on the MDI interface back. When sending data to it from a PC, this PC should see every frame that is sent.

図 58. Setup for Testing the Data Transfer



The actual test setup is shown in 2.3 in addition to 図 58, a converter from MDIO to USB is used for configuring the PHY. Normally MDIO is used by a processor or FPGA to configure the PHY and read back status information. For debugging, the PHY is configured into reverse loopback by writing register 0x16 to 0x20. A PC running Linux is used for sending ethernet frames with a unique 64-bit sequence number and checking back if this is received. When an error on the transmission occurs, a frame will be dropped as the FCS will not match. The PC will then see a missing sequence number.

図 59. Running Data Test in Loopback Mode



This test is done with different PoE load conditions as shown in 表 3. For every test frame with a size of 1500 bytes + headers are used and at least 1 TB of test data is transmitted and received back.

表 3. Error Rates

TEST CONDITION	NUMBER OF ERRORS WITH 20-cm CAT 6 CABLE	NUMBER OF ERRORS WITH 150-m CAT 6 CABLE
No PoE	0	0
PoE 7-W transformer no load	0	0
PoE 7-W transformer 1.6-A load	0	0
PoE 13-W transformer no load	0	0
PoE 13-W transformer 2.4-A load	0	0

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010083.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010083.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010083.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010083.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010083.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010083.

5 Software Files

To download the software files, see the design files at TIDA-010083.

6 Related Documentation

1. Texas Instruments, *TPS23758 IEEE 802.3at PoE PD with No-Opto Sync Flyback DC-DC Controller Data Sheet*
2. Texas Instruments, *TPS23758EVM-080 Evaluation Module User's Guide*
3. Texas Instruments, *DP83867IR/CR High Immunity 10/100/1000 Ethernet Physical Layer Transceiver Data Sheet*
4. Texas Instruments, *DP83867EVM User's Guide*
5. Texas Instruments, *LM74700-Q1 Low IQ Reverse Polarity Protection Ideal Diode Controller Data Sheet*
6. Texas Instruments, *ISO121x Isolated 24-V to 60-V Digital Input Receivers for Digital Input Modules Data Sheet*
7. Texas Instruments, *Broken Wire Detection Using an Optical Switch Reference Design*
8. Texas Instruments, *TPS6280x 1.8-V to 5.5-V, 0.6A / 1-A, 2.3-µA IQ Step Down Converter 6-Pin, 0.35-mm Pitch WCSP Package Data Sheet*

6.1 商標

6.2 Third-Party Products Disclaimer

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7 About the Author

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