

デザイン・ガイド: TIDA-050017

3.3V 入力用の TEC ドライバのリファレンス・デザイン



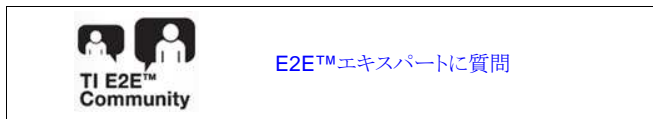
概要

このデザイン・ガイドでは、静止電流の小さい (11 μ A) 昇降圧コンバータ (TPS63802) をマイクロコントローラ MSP430FR2433 と組み合わせて熱電冷却 (TEC) ドライバを実装し、感受性の高いデバイスの温度を精密にレギュレートする方法を説明します。

一部の電子部品は、最良の性能を発揮し、動作寿命を延長するため、その温度を調整する必要があります。光学モジュールに使用されるレーザー・ダイオードなど特定のアプリケーションでは、0.1 $^{\circ}$ C 単位までの正確な温度制御が重要です。これらのアプリケーションでは、温度が 1 $^{\circ}$ C 変化するとレーザーの波長に 0.1nm のずれが生じます。TEC デバイスは、ペルチェ効果を使用して、このようなアプリケーションの温度を制御できます。TEC を通過する電流の方向を制御することで、加熱と冷却の両方の目的に使用可能です。

リソース

- TIDA-050017 デザイン・フォルダ
- TPS63802 プロダクト・フォルダ
- MSP430FR2433 プロダクト・フォルダ
- LM4041D プロダクト・フォルダ

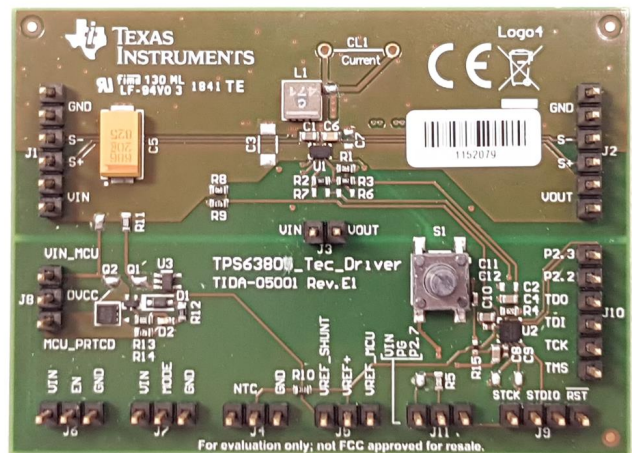
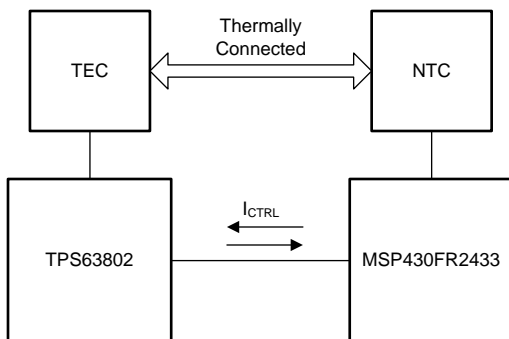


特長

- 低コストのソリューション
- ソリューション・サイズの小さい (30mm² 未満) 電力段 (TPS63802)
- 静止電流の小さい (11 μ A) 電力段 (TPS63802)
- デジタル PI 制御
- 0.1 $^{\circ}$ C 未満の精密な温度制御

アプリケーション

- レーザー・ダイオードの精密な温度制御
 - 光学モジュール
 - 長距離の海底用
 - 都市部データ・センターの相互接続
 - レーザー
- 電子機器パッケージの冷却





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1 System Description

The TPS63802 is a high-efficiency, high-output current (2 A) buck-boost converter available in a 3 mm x 2 mm QFN package. The device can seamlessly transition between buck, buck-boost, and boost modes without any unwanted toggling.

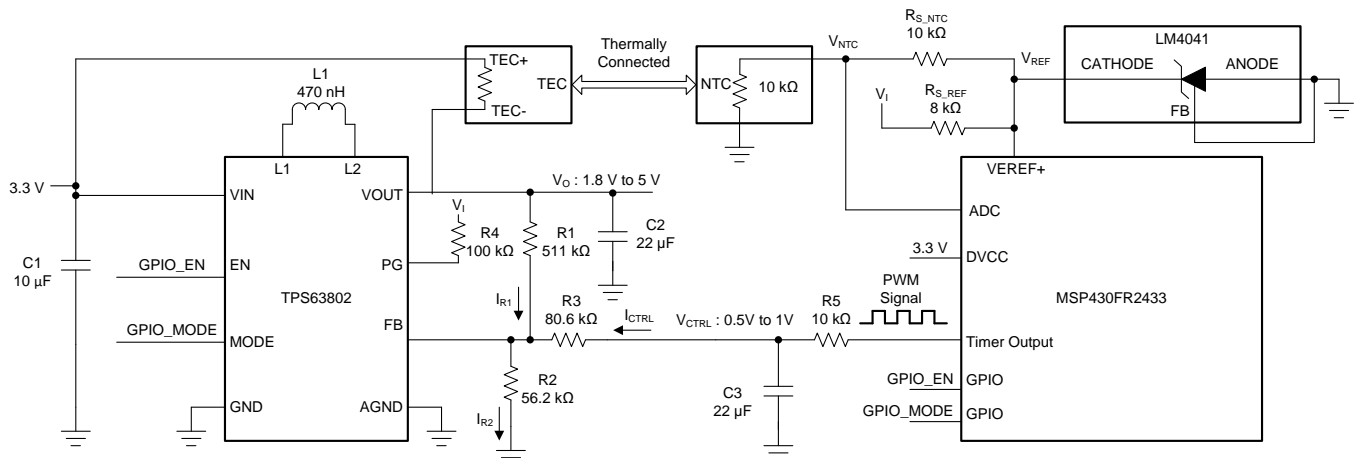
For this reference design, the TPS63802 is supplied by a regulated voltage rail of 3.3 V. The TEC element is connected between the VIN and VOUT pins of the TPS63802. Depending on the current required to flow through the TEC element, the output voltage of the TPS63802 can be varied from 1.8 V to 5 V, by injecting a control voltage V_{CTRL} , through a series resistance R_3 , into the FB pin.

The V_{CTRL} voltage can be generated either with a DAC or a low-pass filtered pulse width modulated (PWM) signal. This design uses the PWM signal option. The PWM signal is generated using one of TI's ultra low-power microcontrollers, MSP430FR2433, that is available in both a BGA and a 4 mm x 4 mm QFN package. The V_{CTRL} voltage can be varied by adjusting the duty cycle of the PWM signal. A Proportional – Integral (PI) control is programmed into the microcontroller unit (MCU) to regulate the temperature of the TEC element to the target value.

2 System Overview

2.1 Block Diagram

図 1. System Schematic



2.2 Design Considerations

The TPS63802 has a built in Power Save (PFM) mode where switching action is paused at low-load currents to achieve higher efficiency. This mode can be used to improve the efficiency when $V_i < V_o$. For conditions where $V_i > V_o$, the forced Pulse Width Modulation (PWM) mode, where the device continuously switches is used. This is because the V_o gets charged externally above its target, by V_i through the TEC element. The TPS63802 can regulate the V_o back to its target value by sinking negative current through the power FETs when the PWM mode is active.

2.2.1 Adjusting the Output Voltage of TPS63802

The TPS63802 regulates the voltage at the feedback pin (FB) pin to 0.5 V. The output voltage is set by 式 1, when the FB resistor divider network consists of only resistors R_1 and R_2 .

$$V_O = \frac{(R_1 + R_2)}{R_2} \times V_{FB}$$

where

- V_O = Output Voltage
 - R_1 = Upper resistor on feedback divider
 - R_2 = Lower resistor on feedback divider
 - V_{FB} = Feedback regulation voltage
- (1)

By adding a resistor R_3 with a control voltage V_{CTRL} to the FB pin, the output voltage can be changed dynamically depending on the current in the R_3 branch. The design equations stated here are for the case where the V_{CTRL} only sources current ($V_{CTRL_MIN} \geq V_{FB}$). For the case where the V_{CTRL} can both source and sink current ($V_{CTRL_MIN} < V_{FB} < V_{CTRL_MAX}$), please refer to the equations in [TIDUCA8](#). The current I_{R2} from FB to ground is constant as the FB voltage is regulated to 0.5 V. The current I_{R1} can be modulated by changing the current I_{CTRL} as $I_{R1} = I_{R2} - I_{CTRL}$. The modulation in I_{R1} is reflected in V_O as $V_O = I_{R1} \times R_1 + V_{FB}$.

To design the feedback divider network, a value of R_1 can be chosen according to the ranges given in [SLVSEU9A](#). The values of R_3 and R_2 can be obtained from 式 2 and 式 3, once the min and max value of the control voltage (V_{CTRL}) are chosen.

$$R_3 = \frac{V_{CTRL_MAX} - V_{CTRL_MIN}}{V_{O_MAX} - V_{O_MIN}} \times R_1$$
(2)

$$R_2 = \frac{V_{FB} \times R_1 \times R_3}{V_{O_MAX} \times R_3 - V_{FB} \times (R_1 + R_3) + V_{CTRL_MIN} \times R_1}$$

where

- R_3 = Resistor between control voltage and FB pin
 - V_{CTRL_MAX} = Maximum value of control voltage
 - V_{CTRL_MIN} = Minimum value of control voltage
 - V_{O_MAX} = Maximum value of output voltage
 - V_{O_MIN} = Minimum value of output voltage
- (3)

For example if R_1 is chosen as 511 k Ω , and V_{CTRL} varies between 0.5 V and 1 V, the calculated values of R_2 and R_3 necessary to vary V_O from 1.8 V to 5 V would be 56.2 k Ω and 80.6 k Ω respectively. The output voltage for a given value of control voltage can be calculated according to 式 4.

$$V_O = V_{FB} + \left(V_{FB} \times \left(\frac{1}{R_2} + \frac{1}{R_3} \right) - \frac{V_{CTRL}}{R_3} \right) \times R_1$$
(4)

2.2.2 Generating the PWM signal

The PWM signal of variable duty-cycle and frequency can be generated using one of the timers of the MCU. For example, the MSP430FR2433 timer can be configured to be in the *Up* mode, where it counts from 0 to the value specified in the `TAXCCR0` register.

The duty-cycle of the PWM signal is adjusted in each cycle, based on the output from the PI controller by setting the `TAXCCR1` register. The timer output pin itself can be used as the PWM source by setting it in one of the Output Modes like *Reset/Set*. Alternatively, a GPIO pin can be used for the PWM signal using the interrupts generated from the timer, if the port pin corresponding to the timer output needs to be simultaneously used by another peripheral of the MCU.

The PWM signal can be sent to a first order low pass filter to generate the V_{CTRL} signal. The corner frequency of the filter should be chosen based on the desired transient response and steady state temperature accuracy required.

2.2.3 Digital PI Controller

The temperature of the TEC element can be sensed by using an NTC element in a simple voltage divider configuration by adding a series resistance R_{S_NTC} with an accurate voltage source V_{REF} , as shown in [図 1](#). A lookup table of temperature versus resistance of the NTC element can be written into the MCU memory. Once the target temperature is input to the MCU, the corresponding NTC resistance (R_{NTC_TARGET}) is obtained from this lookup table. The voltage across the NTC at the target temperature can be calculated using the values of R_{NTC_TARGET} , V_{REF} and R_{S_NTC} . This voltage is used as the reference voltage (V_{NTC_TARGET}) of the PI controller.

An ADC is used to sample the voltage (V_{NTC}) of the NTC element. If the MCU used has an accurate internal reference voltage, the ADC reference and the NTC resistor divider network source (V_{REF}) can be supplied from this reference itself. If the internal reference is not accurate enough, an external reference such as shunt regulator (LM4041D) is required to reach the right temperature set point. When using the LM4041D, a series resistance R_{S_REF} is connected between the supply and the cathode pin. The value of R_{S_REF} must be set properly taking into account the current needed to supply the NTC resistor divider network and the minimum cathode bias current. The LM4041D has reference voltage of 1.233 V between the cathode and feedback pin. R_{S_REF} was chosen to be 8 k Ω in this design to have a total available current of 314 μ A ($(V_I - V_{REF}) / R_{S_REF}$).

The error of the PI controller is the difference between the reference (V_{NTC_TARGET}) and the measured NTC voltage (V_{NTC}). The output U , of the PI controller given in [式 5](#) is the sum of the individual outputs of the Proportional and Integral parts.

$$U = K_p \times E_R + K_i \times (E_R - E_{R_PREV}) \times dt$$

where

- U = Controller output
 - K_p = Gain of proportional part of the controller
 - K_i = Gain of integral part of the controller
 - E_R = Error in present cycle
 - E_{R_PREV} = Error in previous cycle
 - dt = Time between two ADC samples
- (5)

The gains K_p and K_i of the controller need to be tuned based on the thermal environment of the application. The integral part of the error, when using rectangular integration, is the difference between the present error (E_R) and the previously calculated error (E_{R_PREV}) multiplied by the time (dt) between two ADC samples.

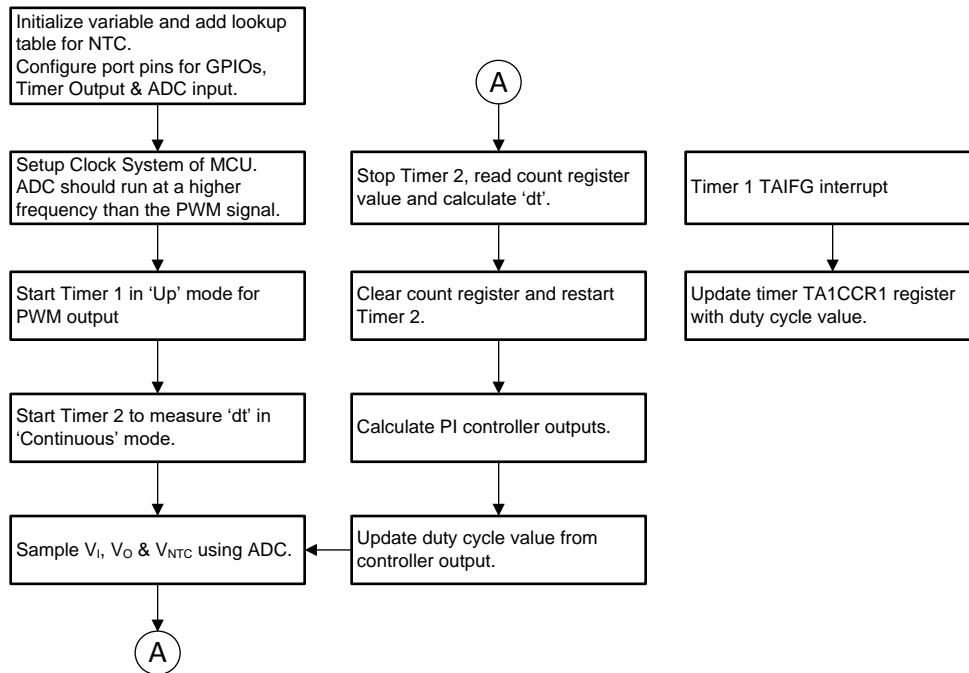
The dt value required for the calculation can be obtained using one of the MCU timers. When using the MSP430FR2433, the timer can be configured to run in the *Continuous* mode. As soon as the ADC completes the conversion of the V_{NTC} voltage, the timer can be stopped and the contents of the timer counter register TAXR be read out. The dt value can then be calculated based on the timer frequency and the number of counts. The TAXR register can then be cleared and the timer is restarted.

The output of the PI controller is used to update the duty cycle of the PWM signal. The duty cycle of the PWM signal should be limited to a range corresponding to V_{CTRL_MIN} and V_{CTRL_MAX} . If the duty cycle is at one of the limits, the integral of the error should be clamped to prevent saturation of the integrator.

2.2.4 Program Flow Chart

The firmware implementation of the digital PI controller on the MSP430FR2433, corresponding to the design schematics found at [TIDA-050017](#) is shown in [図 2](#).

図 2. Program Flow Chart

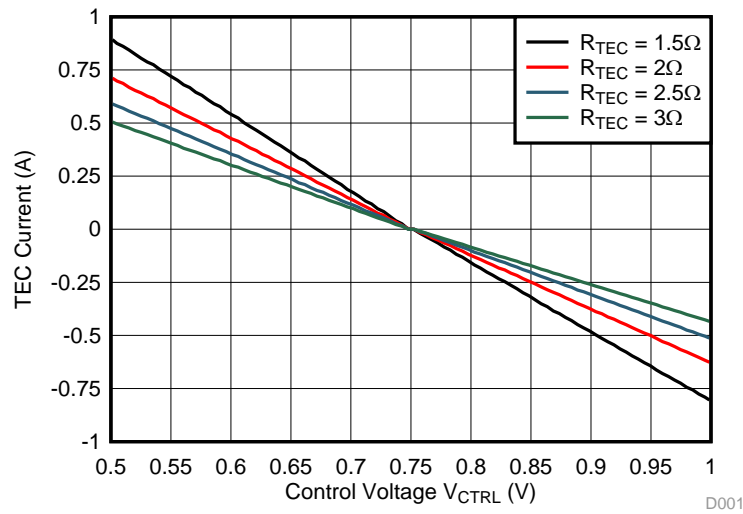


3 Test Results

The TEC current vs Control Voltage (V_{CTRL}), (図 3) and efficiency measurements (図 4 to 図 6), were obtained using a real resistor instead of a TEC element. This was because the resistance of a TEC element drifts much more with temperature when compared with a resistor. This temperature variation of the TEC resistance should be considered when calculating the maximum possible TEC currents. The efficiency of TPS63802 in PFM mode (図 4) is better than in PWM mode (図 5) at lower load currents (< 200 mA) due to the lower switching losses. Higher values of TEC resistance can increase efficiency, but at a cost of a lower maximum TEC current.

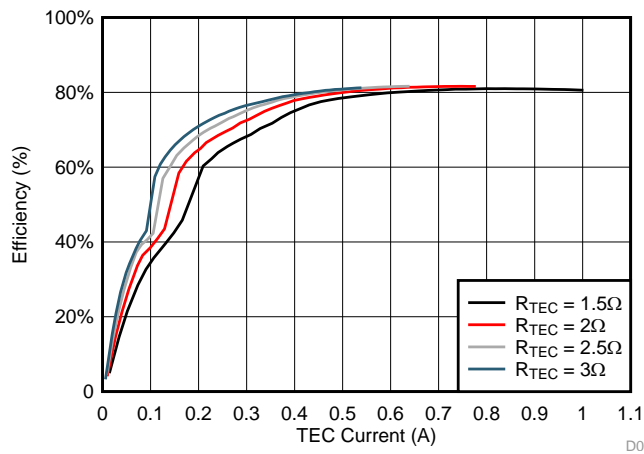
To show the high temperature accuracy achievable with this design, the steady state temperature error over time plot in 図 7, was measured using the values of $R_5 = 10 \text{ k}\Omega$ and $C_3 = 22 \text{ }\mu\text{F}$ for the low pass filter. For this measurement, the LM4041D shunt regulator was used to drive the NTC resistor divider network and also to provide the external voltage reference to the ADC.

図 3. TEC Current versus Control Voltage (V_{CTRL})



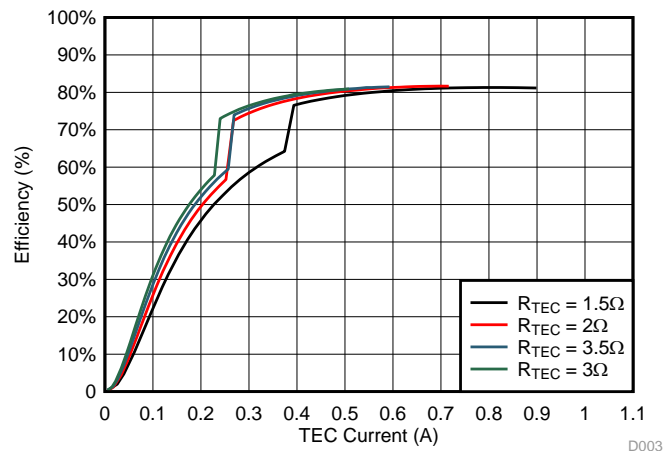
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図 4. TPS63802 Efficiency for $V_O > V_I$ (PFM)



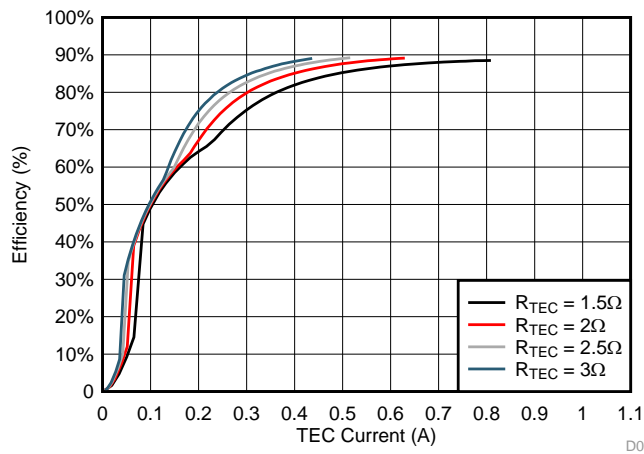
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図 5. TPS63802 Efficiency for $V_O > V_I$ (PWM)



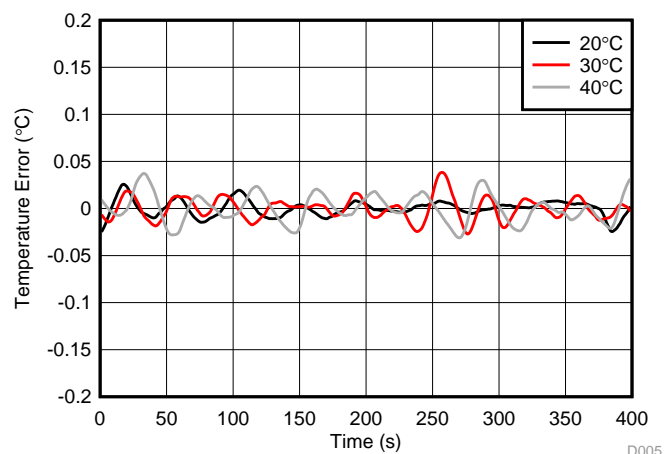
D003

図 6. TPS63802 Efficiency for $V_O < V_I$



D004

図 7. Steadystate Temperature Error of Design



D005

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-050017](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-050017](#).

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-050017](#).

4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-050017](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-050017](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-050017](#).

5 Software Files

To download the software files, see the design files at [TIDA-050017](#).

6 Related Documentation

1. Texas Instruments, [5 V low-power TEC driver reference design](#)
2. Texas Instruments, [MSP430FR4xx and MSP430FR2xx family user's guide](#)

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7 About the Author

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